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Performance Comparison of Different Circuit Using DCVSL and Static CMOS Technique

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Abstract: The basic requirement of any Integrated Circuit is high speed and low power processing of the data signals to perform the desired execution. The minimization of feature size plays an important role in increasing the performance of integrated circuits. But the feature minimization inversely affects the percentage of leakage current when compared to the total current requirement of the circuit. So in this research we design single bit magnitude comparator & 3 input EXOR gate using conventional CMOS logic style as well as DCVSL style and then compared the output of both designs with some parameters. These parameters are power dissipation, delay and number of transistors used in the respective designs, and then concluded that which design yields best results. In CMOS circuits, as the technology scales down to nano scale, the sub-threshold leakage current increases with the decrease in the threshold voltage. So we need a technique to tackle the power dissipation problem in CMOS circuits do the analysis keeping parameters such as power consumption, delay, voltage & transistor count. First, there is the analysis between power consumption & delay, keeping the voltage constant at 1.8V. We here can see that circuit of the DCSVL structures produces better results in terms of power consumption by lowering its value. The circuit designed using DCVS Logic style is an attempt to further reduce the power dissipation with minimum delay.

Keywords: CMOS, 1-bit Magnitude comparator, EXOR gate, DCVSL, delay, transistor count, power dissipation.

1. INTRODUCTION

The single bit magnitude comparator has been designed using different techniques which result in varying power dissipation, delay at 180nm technology used in Tanner EDA tool. Some of the characteristics and performance will vary significantly when we use different logic styles and thus the selection of logic style is most important for the performance of device. These designs are compared by performing simulation and obtaining result in Tanner EDA tool at 180 nm technology mode. Low power and High speed are the design trade-offs in VLSI industry. Until recently performance has been synonymous with speed. Emergence of portable computing devices are enhancing the importance of low power design methodologies. In pass transistor logic, the transistors are used as voltage controlled switches to implement the logic. The PTL logic is Bidirectional. There is no static power dissipation in PTL gates. Comparators are the basic building blocks in digital computer systems. Arithmetic operations are widely used in most digital computer systems. Comparison is a fundamental arithmetic operation and is the base for arithmetic operations such as multiplication and the basic adder cell can be modified to function as subtractor by adding another Xor gate and can be used for division. Therefore, 1-bit comparator cell is the most important and basic block of an arithmetic unit of a system. Xor gate is designed using DCVSL technique because these can produce both complementary and true outputs using single gate architecture.

2. SINGLE BIT MAGNITUDE COMPARATOR

A 1-bit comparator compares two binary numbers applied at input and concluded that the number is either equal to or greater than or less than the another number. The first input A & second input are bits. If bit A is not equal to bit B then either input A is greater than input B for A =1 and B= 0 or A is less than input B for A= 0 and B =1. At this stage, the comparison process ceases. Both of two input number are equal, i.e. when bits A=B. The figure below shows the block diagram of a magnitude comparator, it produces 3 outputs as L (A<B), E (A=B) and G (A>B) as shown in Fig 1.

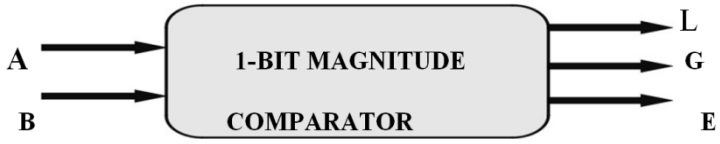

Fig1: Single bit magnitude comparator.

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Table 1: Truth table of 1 bit magnitude comparator.

Sr. No.	INPUT		OUTPUTS		
	A	B	A>B	A<B	A=B
1	0	0	0	0	1
2	0	1	0	1	0
3	1	0	1	0	0
4	1	1	0	0	1

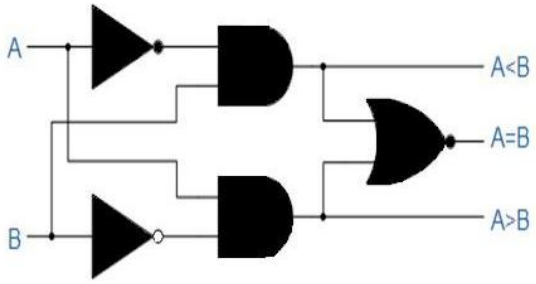

Fig.2 : Magnitude comparator using logic gates

This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. Consider the simple 1-bit comparator above. The operation of magnitude comparator is depicted in the truth table I. Here we notice two distinct features about the comparator from the above truth table. Firstly, the circuit does not distinguish between either two "0" or two "1"'s as an output A = B is produced when they are both equal, either A = B = "0" or A = B = "1". Secondly, the output condition for A = B resembles that of a commonly available logic gate, the Exclusive-NOR or Ex-NOR function (equivalence) on each of the n-bits giving: Q = A Exor B.

3. EXCLUSIVE OR GATE

The Exclusive-OR logic function is a very useful circuit that can be used in many different types of computational circuits.

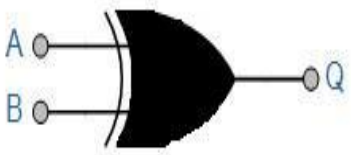

Fig 3: Symbol of EX-OR Gate

There are two other types of digital logic gates which although they are not a basic gate in their own right as they are constructed by combining together other logic gates, their output Boolean function is important enough to be considered as complete logic gates. These two "hybrid" logic gates are called the Exclusive-OR (Ex-OR) Gate. If however, an logic output "1" is obtained when ONLY A = "1" or when ONLY B = "1" but NOT both together at the same time, giving the binary inputs of "01" or "10", then the output will be "1". This type of gate is known as an Exclusive-OR function or more commonly an Ex-Or function for short. This is because its boolean expression excludes the "OR BOTH" case of Q = "1" when both A and B = "1".

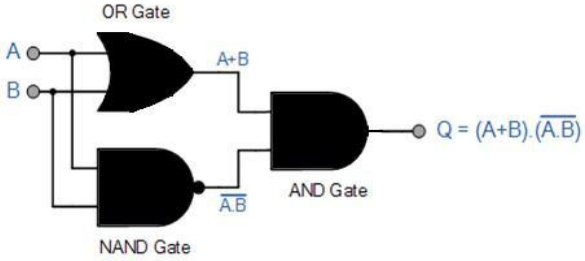

Fig. 4 : EXOR Gate Equivalent circuit

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In other words the output of an Exclusive-OR gate ONLY goes "HIGH" when its two input terminals are at "DIFFERENT" logic levels with respect to each other. An odd number of logic "1's" on its inputs gives logic "1" at the output. These two inputs can be at logic level "1" or at logic level "0" giving us the Boolean expression of: Q = $A.\bar{B} + \bar{A}.B$.

Table II: Truth table of 3 input EXOR Gate'

Sr. No.	INPUTS			OUTPUT
	A	B	C	Out
1	0	0	0	0
2	0	0	1	1
3	0	1	0	1
4	0	1	1	0
5	1	0	0	1
6	1	0	1	0
7	1	1	0	0
8	1	1	1	1
Any ODD Number of Inputs gives Q				

Now the single bit magnitude comparator & Exclusive OR gate is designed using two logic styles:

(i) Conventional CMOS logic style

(ii) DCVS Logic style

4. CONVENTIONAL CMOS LOGIC STYLE

Today's computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. Fig 5 (a) represents circuit of CMOS Inverter. It consists of one NMOS & one PMOS transistor. If input A=0 (i.e. logic low) then both of the gates are at zero potential & PMOS is ON that provide low impedance path from supply voltage to output (Y). Therefore output (Y) approaches to high level of VDD. If input A=1 (logic high) then both gates are at higher potential but NMOS is ON & provide low impedance path between ground & output (Y). Therefore, output (Y) approaches to the low level of 0V.

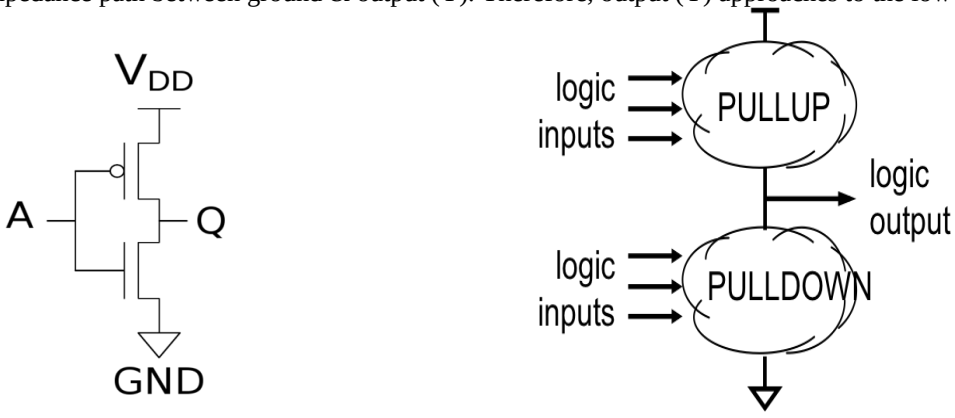

Fig 5: (a) Circuit of CMOS Inverter (b) Logic Network of CMOS Style

5. DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC:

A DCVS Logic is based on 2:1 Multiplexer which is used as an important element in many various circuit designs such as implementation of memory circuits and FPGA. It is valuable in situations where price is a factor and for modularity. A 2:1 Multiplexer is considered to be the basic building block of the "switch logic". "Switch Logic" basically proposes that logic circuits are implemented not as logic gate but as combination of switches. Multiplexers are used to create a single line from two or more digital signals, by engaging them there at changed times.

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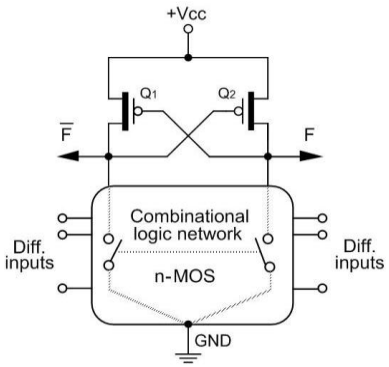

Fig 6 : Schematic of DCVSL logic style.

5.1 ADVANTAGES:

- No static power dissipation
- Differential signals improve noise immunity

5.2 DISADVANTAGES:

- Need 2x NMOS
- Need to wire flag and complement

6. SINGLE BIT MAGNITUDE COMPARATOR USING CMOS LOGIC STYLE

1-bit magnitude comparator circuit is simulated at 180nm technology using Tanner EDA tool, by using static CMOS logic style. This circuit consists of various n-MOS & p-MOS transistors. A magnitude comparator is a combinational circuit that compares two numbers, A and B, and then determines their relative magnitudes. A > B, A = B, A < B. To determine if A is greater than or less than B, we inspect the relative magnitudes of significant digits. If the two digits are equal, we compare the next lower significant pair of digits.

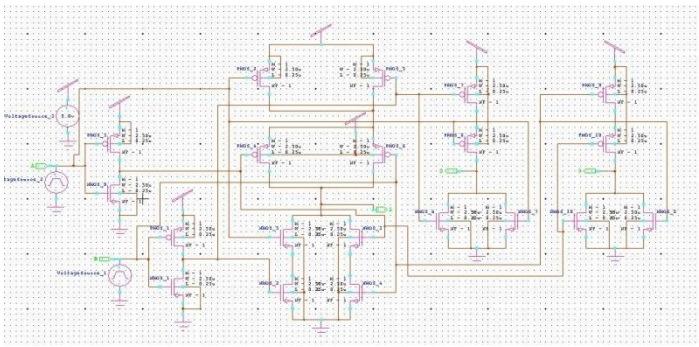

Fig 7: Single bit comparator using CMOS logic style.

The simulated waveform for the circuit designed is as follows.

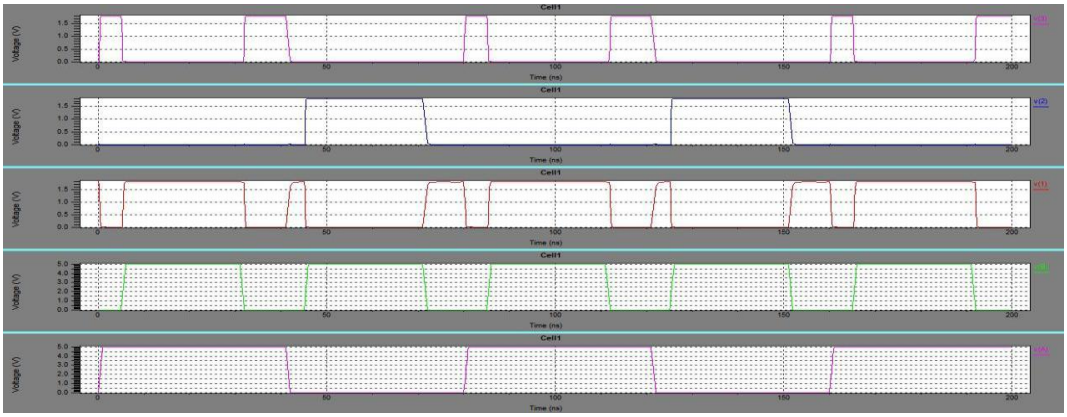

Fig 8: Output waveform of magnitude comparators using CMOS Logic style

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7. SINGLE BIT MAGNITUDE COMPARATOR USING DCVS LOGIC

Static DCVSL is a differential method which requires both true and complementary signals to be routed to gates. Two complementary n-MOSFET switching trees are constructed to a pair of cross-coupled p-MOSFET transistors. Depending on the differential inputs one of the outputs is pulled down by the corresponding n-MOSFET network.

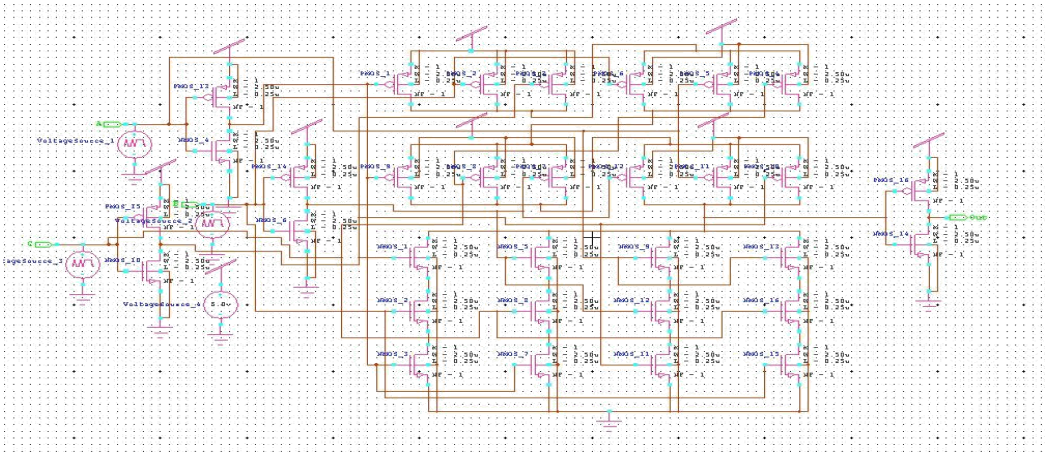

Fig 9: Schematic of magnitude comparator using DCVSL Logic style.

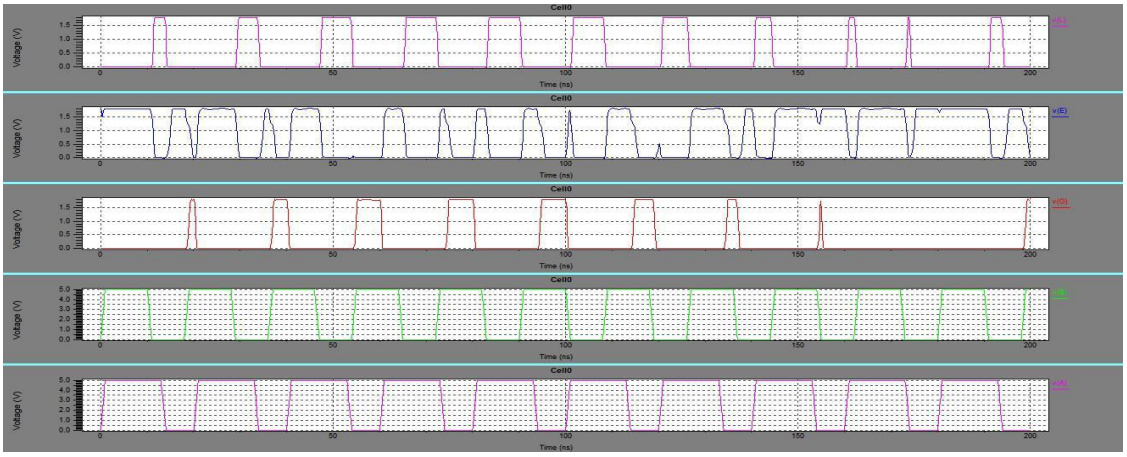

Fig 10: Output waveform of magnitude comparators using DCVS Logic style.

8. EXOR GATE (3-INPUT) USING CMOS LOGIC STYLE:

EXOR Gate is most used gate after NAND gate and nor gate and is directly used in other circuits.

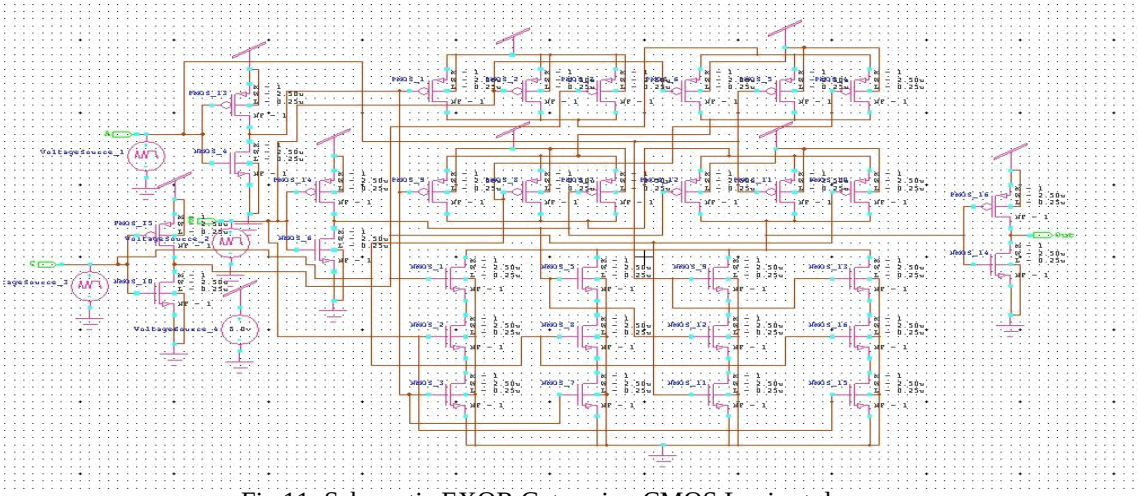

Fig 11: Schematic EXOR Gate using CMOS Logic style.

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Consider input bits as 10 then referring to truth table in the output side, 1 should be obtained in A>B & rest of the output will be obtained as 0. After performing simulation the output waveform (Fig 12) shows the same result as in truth table for the applied input bits. The simulated waveform for the circuit designed is as follows.

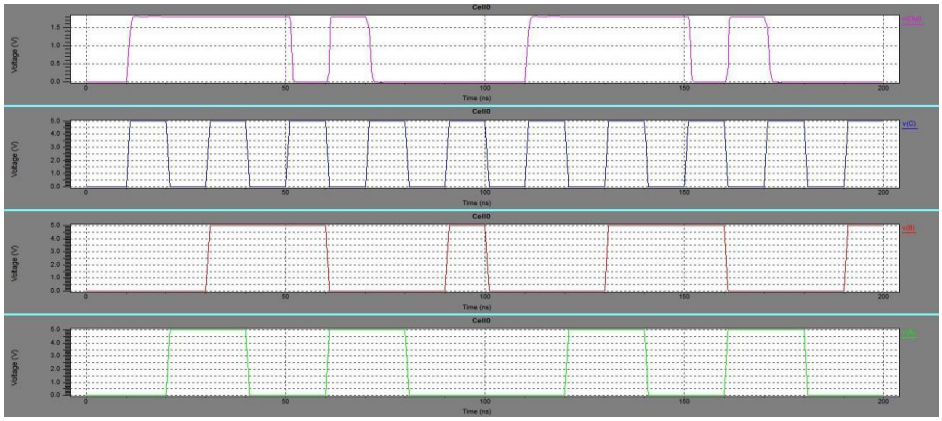

Fig 12: Output waveform of EXOR Gate using CMOS Logic style.

9. EXOR GATE (3 INPUT) USING DCVS LOGIC STYLE

Static DCVSL is a differential method which requires both true and complementary signals to be routed to gates. Two complementary n-MOSFET switching trees are constructed to a pair of cross-coupled p-MOSFET transistors. Depending on the differential inputs one of the outputs is pulled down by the corresponding n-MOSFET network. The differential output is then latched by the cross-coupled p-MOSFET transistors

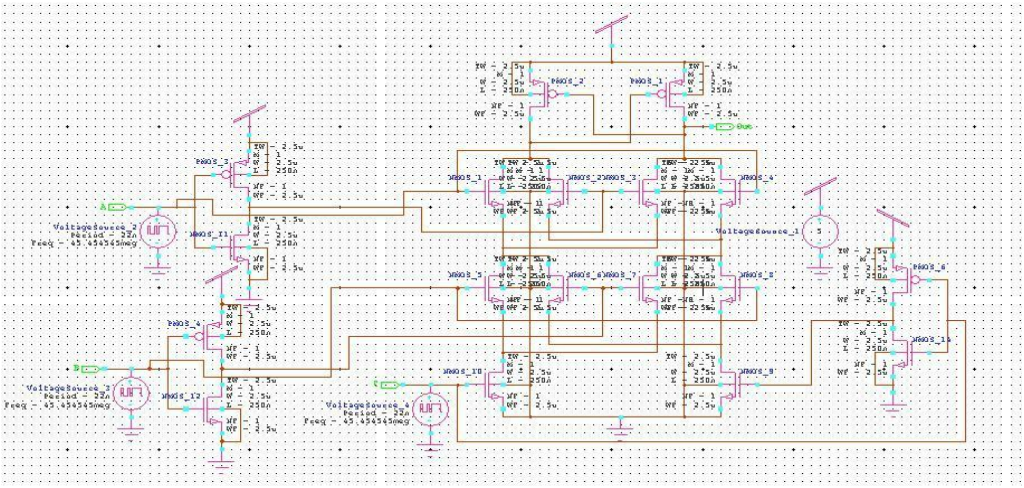

Fig 13: Schematic of EXOR Gate using DCVS Logic style.

The simulated waveform for the circuit designed is as follows.

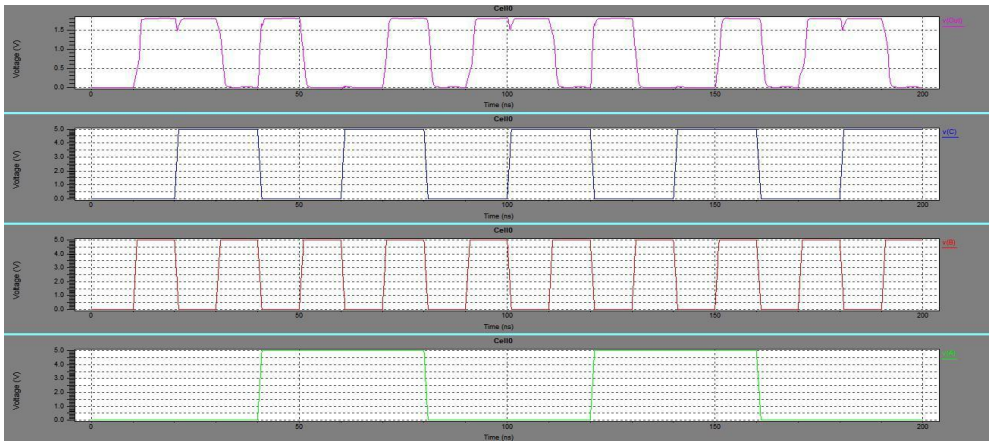

Fig 14 : Output waveform of magnitude comparators using DCVS Logic style.

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9. SIMULATION RESULTS

Sr. No	Input voltage	Circuit Design	Technology	Delay	Power dissipation	Transistor count
1.	1.8v	comparator	Cmos logic	$4.4869e^{-008}$	$1.476638e^{-005}$	24 [12p+12n]
			Dcvs logic	$2.4839e^{-009}$	$1.943302e^{-006}$	26 [8p+18n]
2.	1.8v	Exor gate	Cmos logic	$1.0280e^{-008}$	$2.976007e^{-005}$	32 [16p+16n]
			Dcvs logic	$7.5141e^{-009}$	$2.421221e^{-005}$	18 [5p+13n]

10. CONCLUSION

For low-leakage and high-speed circuit, the important two factors are speed and power. However, the main trade-off is that; when someone goes for speed, the power is degraded. And when the power consumption is improved, the delay is more in that case. Therefore, we go for the power delay product, which best determines the efficient circuit combining the two parameters, keeping other factors such as voltage and transistor count. Also find a technique which results in reduction of both power dissipation and delay, also number of transistors used while designing the circuit. In calculation of the Power Delay Product (PDP) for all of these EXOR & magnitude comparator circuits, it is found out that the proposed circuits of all of them are having less value than the conventional one and static DCVSL adder is having the least among them. A comparison is done with the parameters number of transistors, which shows that the area is least for the static DCVSL comparator than the rest and the number of transistors is least for the Static DCVSL than the conventional CMOS.

11. FUTURE SCOPE

In future a better technology can be used to implement the circuits like dynamic DCVS Logic style and modified DCVS Logic style so that power dissipation, propagation delay & number of transistors used in the circuit can be reduced more. This research contributes to better understanding of power efficient circuits. This work showed that the total transistors used will be saved in the DCVS Logic style.

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