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Design and Implementation of PID Controller using HDL on FPGA

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Abstract— This paper concentrates on the work done on controller using Field Programmable Gate Array (FPGA) technology. FPGA based realization offers high speed, complex functionality, consume less power, and provides parallel Processing. Proportional-Integral-Derivative (PID) controllers are universal control structure and have widely used in Automation systems. A PID is widely used in feedback control of industrial processes on the market in 1939 and has remained the most widely used controller in process control until today. The work is done on PID Controller and working status of PID Controller is shown through its one of application i.e. a line follower Car which is used in industry for parcels and stuffs transports. For such an PID to obtained an pre-defined output a Car is created which may called as a application of PID Controller. The car is composed by three cards DE0-Nano main card, SCD(Smart Car Daughter card) daughter card, and sensor daughter card. The SDC daughter card includes the lamp, buzzer, motor driver DRV8833, IR receiver, ADC chip LT2308, and TMD (Terasic Mini Digital) expansion header. The sensor daughter card includes seven Photo Interrupters used to track dark line (s) on a white background. Proportional-integral-derivative (PID) controller is a vastly used control algorithm for many real-time control applications and among many types of PID controller, FPGA based PID controller is one of the effective one. FPGA can offer parallel processing, more speed and easy to implement. In this paper, we focused our works designing PID controller with its application by Field Programmable Gate Arrays (FPGAs) with some parameter change so that the cost will be minimized and accuracy will be maximized.

Keywords: P1D, HDL, FPGA, Control system.

I. INTRODUCTION

Proportional-Integral-Derivative (PID) controllers are universal control structure and have widely used in Automation systems, they are usually implemented either in hardware using analog components or in software using Computer-based systems. PID controller can be understood as a controller that takes the present, the past, and the future of the error into consideration. A PID is widely used in feedback control of industrial processes and has remained the most widely used controller in process control until today. The work is done on PID Controller and working status of PID Controller is shown through its one of application i.e. a line follower Car which is used in industry for parcels and stuffs transports. A proportional– integral–derivative controller (PID controller) is a method of the control loop feedback. This method is composing of three controllers [1]: 1. Proportional controller (PC) 2. Integral controller (IC) 3. Derivative Controller (DC). Along with PID it contain a kit which comes with the following contents: A car body, 4-pack AA size batteries, IR Remote control, USB Mini-B cable,5V Power Supply, DC Adapter Cable ,Quick Start Guide. The PID controller is implemented in C++ code running on the Altera NIOS II Processor. The program is stored on the FPGA on-chip memory. Proportional Integral Derivative (PID) based scheme is widely preferred in industries because of their simple structure and ease of realization. Project is to design a PID controller with its application which I have created a cute line follower Car and implement it on FPGA using hardware description language. PID controller along with PWM module is used for speed control of DC motor and current – voltage control of DC –DC converter. Proportional-Integral-Derivative (PID) controller are still dominating in the motion control systems in the industry due to the well acquaintance of the operating personnel with PID controllers.

III. LITERATURE REVIEW

The main aim of this paper [1] is to design PID control PWM module using Field Programmable Gate Array (FPGA) technology. FPGA based realization offers high speed, complex functionality, consume less power, and provides parallel processing. In this paper, we have implemented PID control PWM module on programmable logic design software Quartus II and verified on DE0 Nano Board (Cyclone IV FPGA family of company Altera). Signal Tap II analyzer and RTL viewer are used for analyzing and debugging the design. For Proper timing constraint and clock

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arrangement, Time Quest analyzer is used. The simulation and hardware results shows that implementation with FPGA has some advantages such as flexible design, high reliability and high speed. Proportional-Integral-Derivative (PID) controllers [2] are universal control structure and have widely used in Automation systems, they are usually implemented either in hardware using analog components or in software using Computer-based systems. In this paper, we focused our works designing on building a multi-channel PID controller by Field Programmable Gate Arrays (FPGAs). To overcome the hardware complexity by the use of more processors for multi channel, using single PID controller for multi channel .Multi channel can be implemented by the use of FPGA.when the error is more it can differentiate and produce the constant output, when signal is low when compared to reference signal it can integrate it.FPGA can offer parallel processing, more speed.

The main objective of this paper [3] is to present the steps of how to program a PID controller in a FPGA, and in that way to control a DC motor using Pulse Width Modulation. Also we want to give some ideas to people interested in program embedded controllers in hardware. During the project use some tools to help us to visualize the behavior of the controller on the computer screen through rs232 communication and LabView chart to plot, and LCD display for visualize the Set Point, gains and the current value PID (Proportional – Integral - Derivative) controllers are the most widely used closed loop controllers due to their simplicity, robustness, effectiveness and applicability for much kind of systems [4] . With the rapid development of technology, implementation of PID controller has gone several steps fromUsing analog components in hardware to using some software based program to execute PID instructions digitally in some processor-based systems. And also, these developments have brought an alternative solution to implement PID instructions in Programmable Logic Devices (PLD). Field Programmable Logic Array (FPGA) is the most advanced members of PLDs. This paper [4] presents the digital PID algorithm on FPGA. The controller algorithm is developed using VHDL and implemented using Altera DE0 Nano Board. As the controlled system, five axis robot arm is selected, which have five dc motor and four potentiometer to determine the positions of motors. The results show that digital PID controller and also multi-feedback control systems can be implemented successively using FPGA devices.

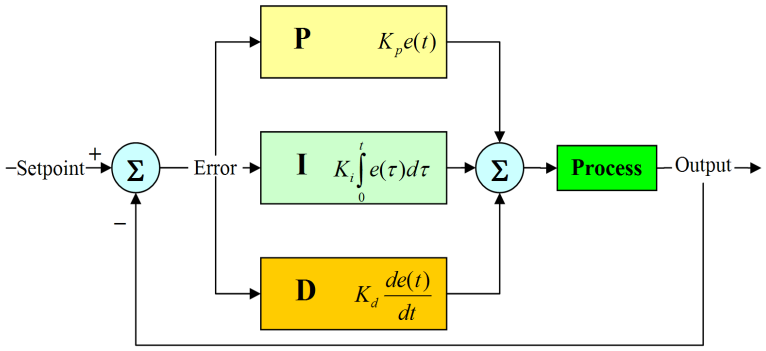
This paper presents [5] a novel technique for implementation of an efficient FPGA based digital Proportional-Integral-Derivative (PID) controller for the motion control of a permanent magnet DC motor. The implementation technique circumnavigates the problem of interfacing analog and digital systems in real-time. The controller is used in a speed control loop. This paper [6] explains a method for the design of Intelligent PID controller based on Very large scale integrated circuits (VLSI). In PID controller parameters are tuned with particle swarm optimization (PSO) algorithm. The error is identified and the PSO algorithm controls the system with many iteration of different parameters.

This paper [7] presents the implementation of a proportional-integral-Derivative (PID) controller for motion control of a DC motor based on FPGA. This implementation technique used to avoid the problems which create during analog and digital interfacing system in real-time.the controller used in speed controller loop. The hardware implementation has been done on a Xilinx Spartan 3 FPGA chip and generates the PWM signal as an input of motor driver for controlling. The out of optically encoded data is decoded and give it to PID control loop. Proposed implementation is present through the VHDL algorithm

IV. PID CONTROLLER

The PID algorithm consists of three modes proportional, integral and derivative mode.
PID algorithm consists of three basic coefficients:

- Proportional: For Proportional p(t) = Kp*e(t)
- Integral: For integral i(t) = Ki*∫e(t)dt
- Derivative: For derivative d(t) = Kd* de(t)/dt



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The PID Controller is implement in the Main.cpp.In this demonstration, only P and D are used. The PID code looks like the following. The **error** input obtained from proportional and derivative of PID will be used to generate new **output** value. The output value will be used to generate the **turn** value which is used to generate **Left-Speed** and **Right-Speed** for the two motors on the A-Cute Car. In this demonstration, kp is 1.0 and kd is where kp is roportionality constant and kd is derivative constant 8.0. (ki is 0.0). The PID controller is implemented in C++ code running on the Altera NIOS II Processor. The program is stored on the FPGA on-chip memory. The LTC2308 IP is used to read eight digitized value from the LTC2308 ADC chip through high speed SPI bus. The eight digitized values include one digitized value for the input power voltage and seven sensor values from the sensor board which contains seven Photo Interrupters used to track dark line(s) on a white background. The PWM IP is used to control the rotation speed and direction of DC motor. Each motor is controlled by a PWM controller. The 1K waveform IP is used to generate 1M frequency to drive the buzzer and the associated GPIO is used to control the beep sounds on or off switch.Left and right lamps are directly controlled by GPIO IP .The IR receiver is used to decode the recevied IR signal which is tramsmiited from the Terasic remoted controller.

V. SYSTEM BLOCK DIAGRAM

The first board to be introduced is the main controller called Terasic DE0-Nano Board. This board uses the Altera Cyclone IV FPGA chip as the main control board. It is responsible for the entire Acute car control system. The second is the A-Cute driver board. It was designed and developed by Terasic SCD (Smart Car Daughter) Card. It is responsible for converting the battery power and driving the motor. The third is to introduce A-Cute Sensor Module Board. It is placed at the front of the car. It is used for sensing the ground black line, enabling the car to follow the black line in a forward direction.

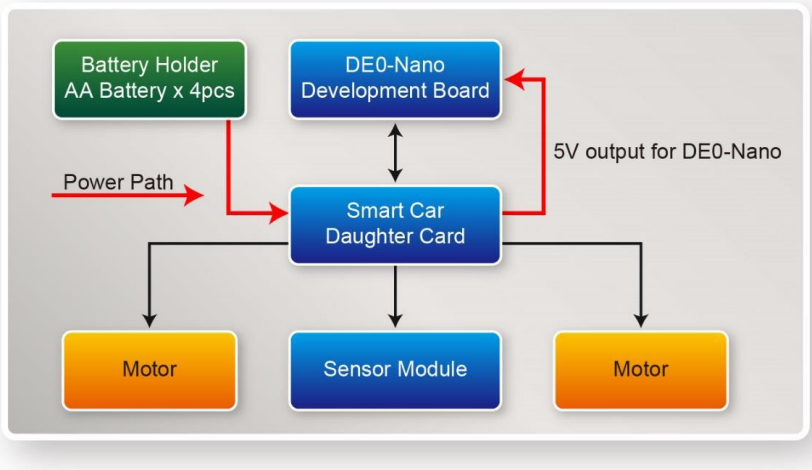

Figure: Block Diagram of System

VI. SCD (Smart Car Daughter) CARD

Smart Car Daughter was developed for the two wheels of the car, the infrared sensing, and motor drive control board. It can be connected to any GPIO Port on the Terasic board. This allows users to easily control the DC Motor, achieving automatic control purposes. The main functions of the board:
1. Power System: Buck-Boost DC/DC Converter, 5V/2A output for Control Board Power supply.
2. Motor Driver: Can drive two Brushless DC Motors.
3. ADC: 8-channel for IR Sensor input and Battery power meter.
4. LED: Two white LED for illumination.
5. Buzzer: You can play some sound.

The main functions of Smart Car Daughter Card:
Power System: Buck-Boost DC/DC Converter, 5V/2A output for Control Board Power supply.
Motor Driver: Can drive two Brushless DC Motors.
ADC: 8-channel for IR Sensor input and Battery power meter.
LED: Two white LED for illumination.
Buzzer: You can play some sound.
TMD (Terasic Mini Digital) expansion header: Can use Bluetooth Daughter (BTS-TMD) for the expansion of remote control.

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VII. IR RECEIVER CONTROLLER

The IR Receiver IP receiving the input IR signal. When valid IR signal is received, the received IR scan code is stored in hardware FIFO and IRQ is asserted. To start receiving IR scan code, the main program should call the member function ***Enable*** to enable interrupt handling. To disable interrupt handing, main program can call the member function ***Disable***.

VIII. SENSOR MODULE

Sensor Module contains Seven IR Sensors. Each IR Sensors consist of one IR Transmitter and one IR Receiver. Single IR Sensors can detect both black and white surface. When IR receiver receives rays it send 1 and when it does not receive any rays it sends 0. IR Sensors are attach in such a way that the transmitter and receiver both can see the surface of ground so they can see the black and white surface. It is placed at the front of the car.It is used for sensing the ground black line, enabling the car to follow the black line in a forward direction.When IR Sensor is on the black surface none of IR ray will transmitted by transmitter.
Reason: Black surface will absorb the IR Rays so the receiver will receive 0 and it will continue its work .If IR Sensor is on the white surface IR ray will be detect by transmitter and it transmit 1 to the receiver.

IX. MOTOR

A-Car body is composed of acrylic, with two geared motor groups, and 66mm diameter rubber wheels. The third wheel (a training wheel) is attached to the front of the body**.** The PWM controller generate required duty cycle to control motor rotation speed. The member function SetSpeed with an input parameter fSpeed is designed to control motor speed and direction.fSpeed value range is -100.0~100.0. Positive value presents forward rotary, and negative value presents backward rotary. 100 represent maximal speed for forward rotary, and -100 represents maximal speed for backward rotary. The SetSpeed function translate the input parameter fSpeed to required PMW parameters for the PWM controller. The translate formula also depends on the input voltage level which is used to drive the DC motor. The member function SetInputPower is designed for users to input the current input power voltage level. After setting motor speed, calling member function Start can start motor rotation. To stop motor rotation, developer can use the member function Stop. The member function SetSpeed is designed to setup car movement speed and direction. The member function Start is designed to start car moving, and the member function Stop is designed to stop car moving.

X. DE0-NANO BOARD

The DE0-Nano board introduces a compact-sized FPGA development platform suited for to a wide range of portable design projects ,such as robots and mobile projects. The DE0-Nano is ideal for use with embedded soft processors—it features a powerful Altera Cyclone IV FPGA (with 22,320 logic elements), 32 MB of SDRAM, 2 Kb EEPROM, and a 16 Mb serial configuration memory device. For connecting to real-world sensors the DE0-Nano includes a National Semiconductor 8-channel 12-bit A/D converter, and it also features an Analog Devices 13-bit, 3-axis accelerometer device. The DE0-Nano board includes a built-in USB Blaster for FPGA programming, and the board can be powered either from this USB port or by an external power source. The board includes expansion headers that can be used to attach various Terasic daughter cards or other devices, such as motors and actuators. Inputs and outputs include 2 pushbuttons, 8 user LEDs and a set of 4 dip-switches**.**

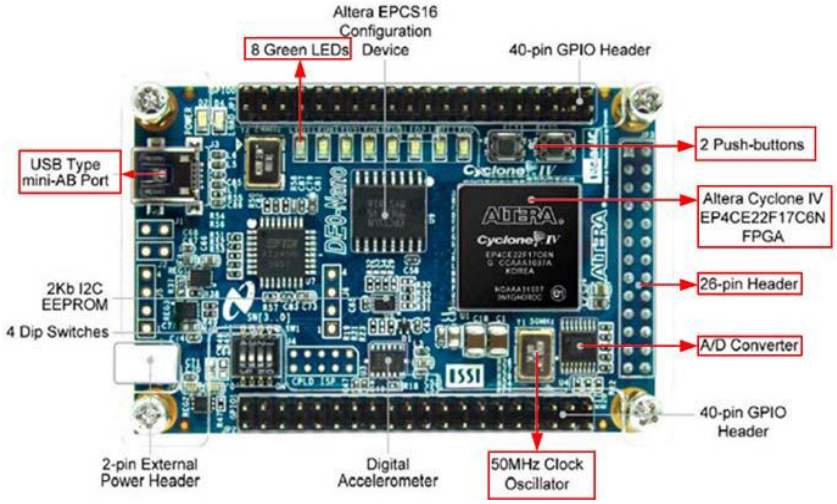

Figure The DE0-NanoBoardPCB and component diagram(top view)

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The Block Diagram Of DE0 Nano Board:

Figure shows the block diagram of the DE0-Nanoboard. To provide maximum flexibility for the user, all connections are made through the Cyclone IVFPGA device. Thus, the user can configure the FPGA to implement any system design. The DE0-Nano board contains a Cyclone IV E FPGA which can be programmed using JTAG programming. This allows users to configure the FPGA with a specified design using Quartus II software.

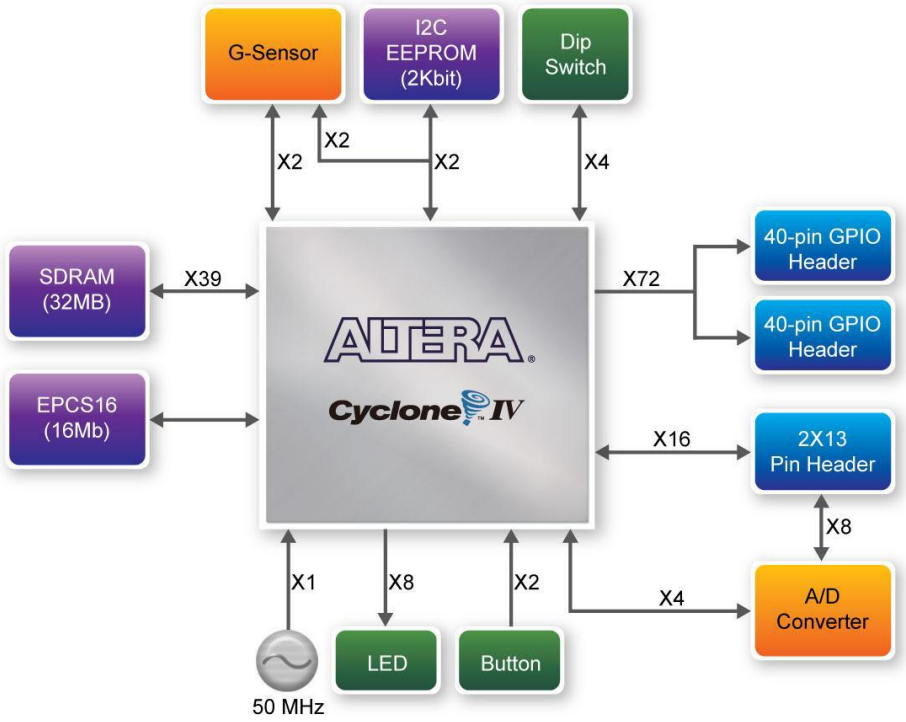

Figure:Block Diagram of DE0 Nano Board

The DE0-Nano board contains an Altera EPCS16 serial configuration device. This device provides non-volatile storage of the configuration bit-stream, so that the information is retained even when the power supply to the DE0-Nano board is turned off. When the board's power is turned on, the configuration data in the EPCS16 device is automatically loaded into the Cyclone IV E FPGA. There are 8 green user-controllable LEDs on the DE0-Nano board. The eight LEDs, which are presented it, allow users to display status and debugging information. Each LED is driven directly by the Cyclone IV E FPGA. Each LED is driven directly by a pin on the Cyclone IV E FPGA. The DE0-Nanoboard contains a 4 dipswitches. A DIP switch provides, to the FPGA, a high logic level when it is in the DOWN position, and a low logic level when in the UPPER position. The board features a Synchronous Dynamic Random Access Memory (SDRAM) device providing 32MB with a 16-bit data lines connected to the FPGA. The chip uses 3.3V LVCMOS signalling. Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) is a low voltage class of CMOS technology integrated circuits. The DE0-Nano contains a 2Kbit Electrically Erasable PROM (EEPROM). The EEPROM is configured through a 2-wire I2C serial interface. The DE0-Nanocontains an ADC128S022 lower power, eight-channel CMOS 12-bit analog-to-digital converter.This A-to-D provides conversion throughput rates of 50 ksps to 200 ksps. It can be configured to accept up to eight input signals at inputs IN0 through IN7.

The key features of DE0-NanoBoard are :

- Featured device

  Altera Cyclone® IV EP4CE22F17C6N FPGA

  153 maximum FPGA I/O pins

- Memory devices

  32MB SDRAM

  2Kb I2C EEPROM

- General user input/output

  8 green LEDs

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2 debounced pushbuttons

4-position DIP switch

- A/D Converter

NS ADC128S022, 8-Channel

12-bit A/D Converter

50 Ksps to 200 Ksps

XI. FPGA DEVLOPMENT BOARD

For digital implementation microcontrollers are used, but FPGA has flexibility, increasingly better power efficiency and decreasing prices. The application range of FPGA based designs increases every day. This is mainly due to the flexibility and capability to perform parallel tasks. The industry is adopting massively the core-based design methodology for system integration using FPGAs, which leads to the appearance of the System-on-Programmable-Chip (SoPC) platforms. With the help of FPGA we can able to develop a circuit in digital form that involves high division of complexity. Due to this, FPGA technology is utilized so that to build up a digital circuit so to get an efficient, flexible and fast control system. In FPGA, there is no fixed hardware structure, so it is defined by user.

Altera Quartus II design software

The Altera Quartus II design software provides a complete, multiplatform design environment that easily adapts to your specific design needs. It is a comprehensive environment for System-On-a-Programmable-Chip (SOPC) design. The Quartus II software includes solutions for all phases of FPGA and CPLD design

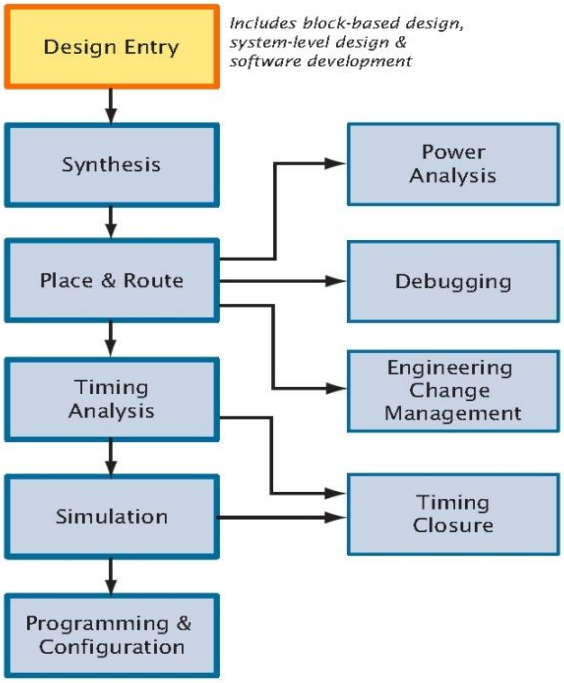

Figure 1. Quartus II Design Flow

In addition, the Quartus II software allows you to use the Quartus II graphical user interface and command-line interface for each phase of the design flow. You can use one of these interfaces for the entire flow, or you can use different options at different phases.

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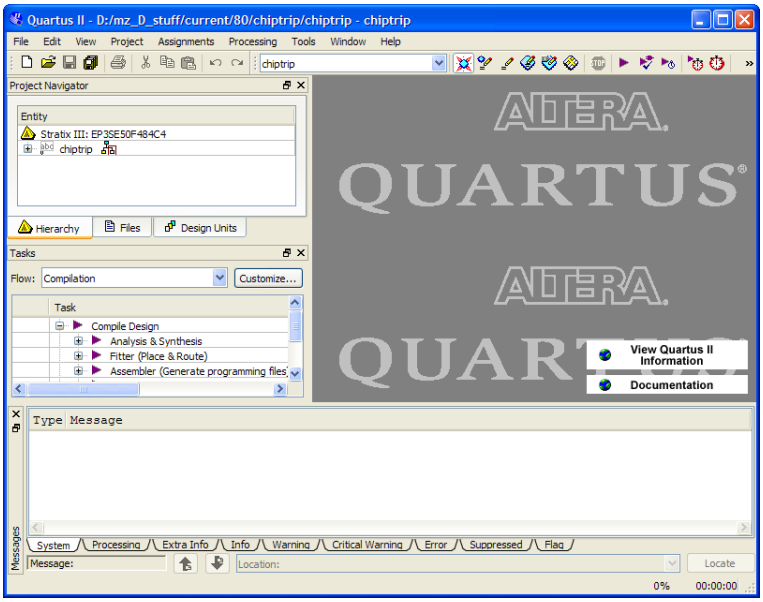

Figure 2 Quartus II Graphical User Interface

XII. RESULT

Based on PID Controller a line follower car is created which is application of PID Controller. To verify the output it is simpler with the help of line follower car because if the line follower Car is working in a proper way then one can say that the design and implementation of PID Controller is successfully done which is the theme of my project. The line follower car is composed by three cards DE0-Nano main card, SCD(Smart Car Daughter card) daughter card, and sensor daughter card.

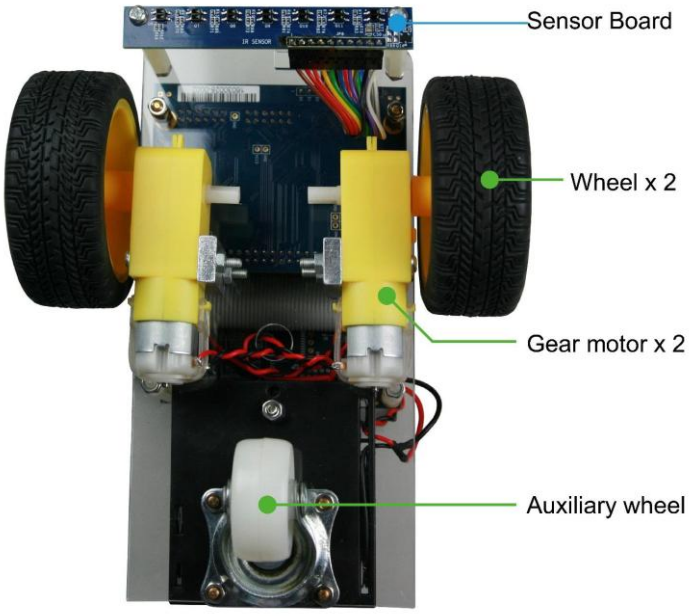

Figure The bottom view of A line follower Car

The project is built by Quartus. Use Quartus to open the Quartusproject file DE0_NANO_SMART_CAR.qpf and click the menu item “Processing Start Compilation” will start the compile process. When compilation is completed, an output file DE0_NANO_SMART_CAR.sof will be generated under the output files folder.

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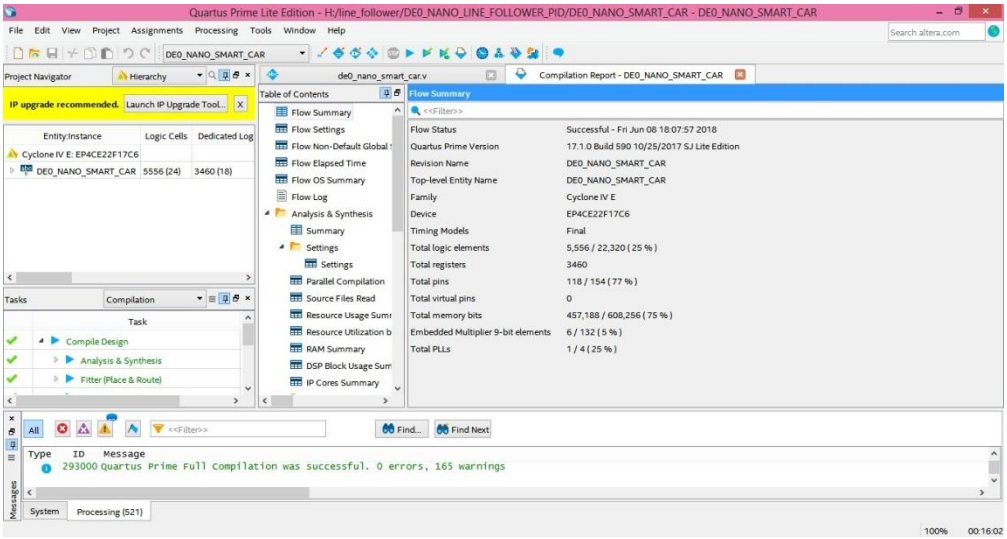

Once have successfully compiled a project with the Quartus II software, We can program or configure an Altera device. The Assembler module of the Quartus II Compiler generates programming files that the Quartus II Programmer can use to program or configure a device with Altera programming hardware. We can also use a stand-alone version of the Quartus II Programmer to program and configure devices

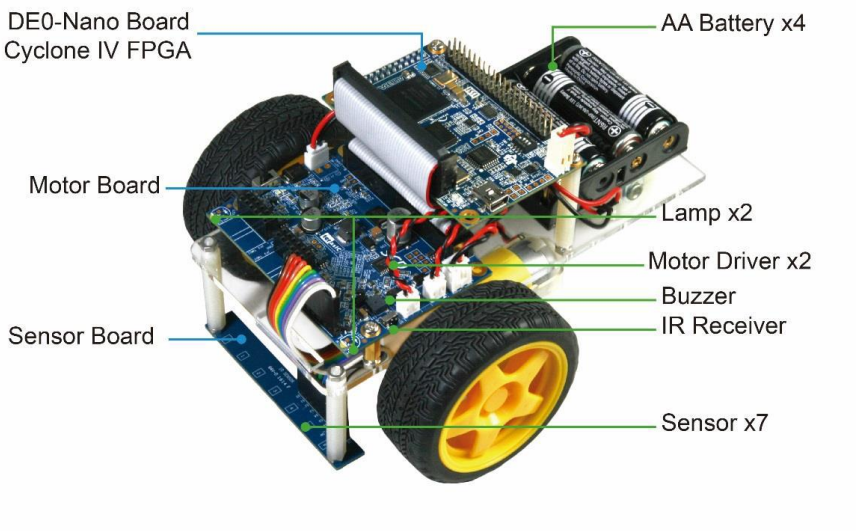

Figure Top View of A line follower Car

The final model of a line follower Car is as shown in figure. Now the Car is ready to perform its operations it can now run on a black surface without any distortion. The application area of line follower Car is it is used in industry for parcels and stuffs transports from one place to another place.

VIII. CONCLUSIONS

Here I can conclude that the design and implementation of PID Controller is successfully done because, To show the proper and actual working of an PID controller it is important to show it with an certain example. So I created a line follower Car based on PID controller which is helpful in industry as they are carrying the parcels or materials from one place to another place using the crane system . The Car is working in Proper way so that I can say that the design and implementation of PID Controller is successful. Based on the PID Controller the Car is constructed so that it is simpler to derived and verified the output of PID Controller .Though there are many control systems are available, PID is the best and mostly used robust control system. The line follower Car's applications start from basic domestic uses to industrial uses. The present condition in industry is line follower Car is carrying the parcels or materials one place to another place using the crane system .

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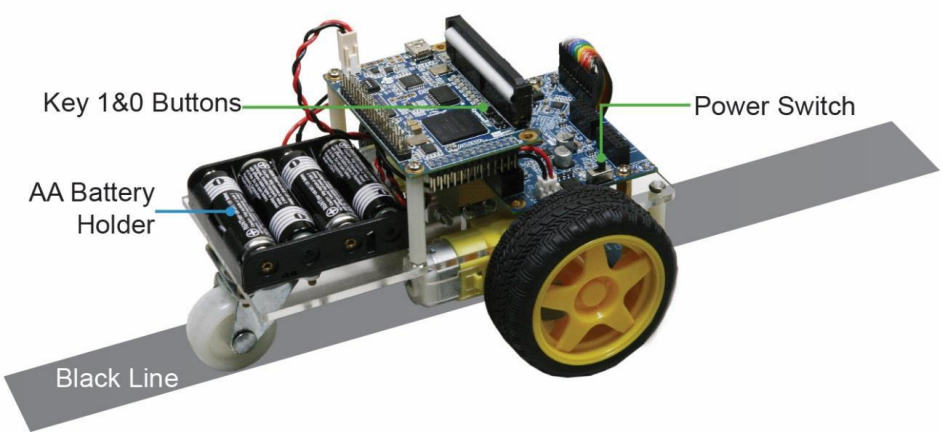

Figure A line follower Car on a Black surface.

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