IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 7, Issue 5, May 2018

Optimization of a Ground Bounce Noise Reduction in NAND Logic Gate in 90nm Technology

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Abstract: In this paper, a varied range of adder circuits are designed in which NAND Gate, are designed using MOSFET in 90nm Technology length. Then, they are simulated using HSPICE and the performance parameters of NAND Gate such as average power, Leakage current and ground bounce is improved. A dual switch mode low power technique is applied on NAND Gate to improve all parameters.

Keywords: NAND, Dual Switch-Mode, 90nm.

1. INTRODUCTION

The way toward scaling advancements to nano-meter administration has brought about a quick increment in spillage power scattering (static and dynamic power dispersal). Diminishing the static power scattering has turned out to be critical amid times of inertia to create outline procedures. Without exchanging off execution the power lessening must be accomplished which makes it harder to diminish spillage amid (ordinary) task at runtime .In sleep or standby mode to decrease the spillage power there are a few procedures that are utilized. Surely understood strategy is Power gating system where a sleep transistor is included between virtual ground (circuit ground) and genuine ground rail. In the sleep mode to remove the spillage way, the gadget is killed. This procedure gives a considerable diminishment in spillage at a negligible effect on execution. It has been demonstrated that the Power Gating system utilizes high Vth sleep transistors. At the point when the square isn't exchanging high sleep transistors are cut off VDD from a circuit piece. An essential plan parameter is size of the sleep transistor and this strategy is otherwise called MTCMOS (Multi-Threshold CMOS). To accomplish long haul spillage power diminishment a remotely exchanged power supply is an extremely essential type of power gating. Inside power gating is more reasonable to stop the piece for little interims of time. Power can be controlled by power gating controllers and to give power to the hardware CMOS switches are used.The power gated yields square releases gradually. Subsequently voltage levels of the yield square invest more energy in limit voltage level (Vth), and in this manner it prompts bigger short out current in the circuit. NMOS footer switches can likewise be utilized as sleep transistors in the plan of power gating system. The sleep transistors can be embedded to part the chip's power organize into a perpetual power arrange associated with the power supply and a virtual power organize that drives the cells and can be killed. By utilizing of cell-or group based (or fine grain) approach or a circulated coarse-grained approach Power Gating can be actualized.

2. NAND LOGIC GATE AND IMPLEMENTATION TECHNIQUES:

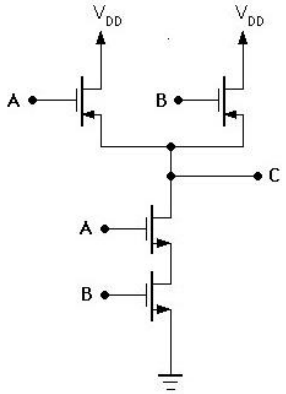

Figure 1: NAND Gate

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Figure 1 shows basic circuit for NAND gate. InTri-mode-controlled MTCMOS technique to implement the intermediate PARK mode for ground bouncing noise suppression from SLEEP to Active mode .A .high-Vth PMOS sleep transistor (called Parker) is connected in parallel with the footer [18] .as shown in" Fig 2"

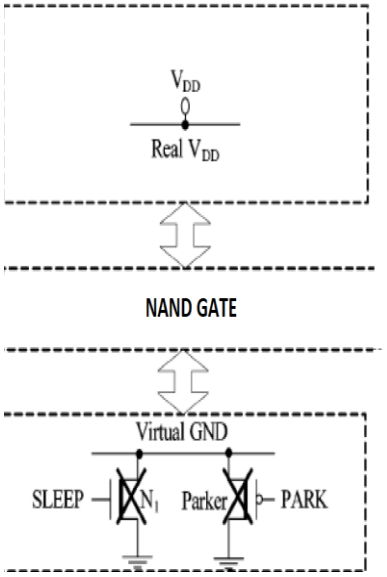

Figure 2 NAND Based On Tri-mode- Controlled MTCMOS Technique

In the SLEEP mode, all the transistors i.e Sleep transistors and Parkr transistor are turned off which reduced the sub threshold leakage currents. In the PARK mode, the Parkr and header are turned on. The footer is at cut-off mode. In ACTIVE mode, the header and footer are turned on. The MTCMOS circuit operates with high speed .The SLEEP mode is the preferable mode of operation for minimization the leakage power consumption. PARK mode is an intermediate mode during SLEEP to ACTIVE mode to suppress the ground bouncing noise .The virtual power line is charged from intermediate voltage level V mid (0V < V mid < VDD) towards ~VDD and The virtual ground line is discharged from V mid toward the threshold voltage of the Parkr. At the end of the intermediate transition period to complete the circuit activation process footer transistor is turned on. During the transition from PARK mode to the ACTIVE mode, the virtual ground line is discharged from Vtp to ~Vgnd. Two-step wake-up process reduce the range of voltage swing on the virtual ground line which will reduced ground bouncing noise To reduce the transition delay from the SLEEP to the PARK mode, a low-Vth Parkr can be used, as shown in "Fig.4.5(b)".Tri-mode-controlled MTCMOS with high- Vth Parkr transistor (TTH) and the Tri-mode-controlled MTCMOS with low-Vth Park transistor (TTL) of the Tri-mode-controlled technique is use for ground bouncing noise reduction.

Dual-Switch MTCMOS Technique:

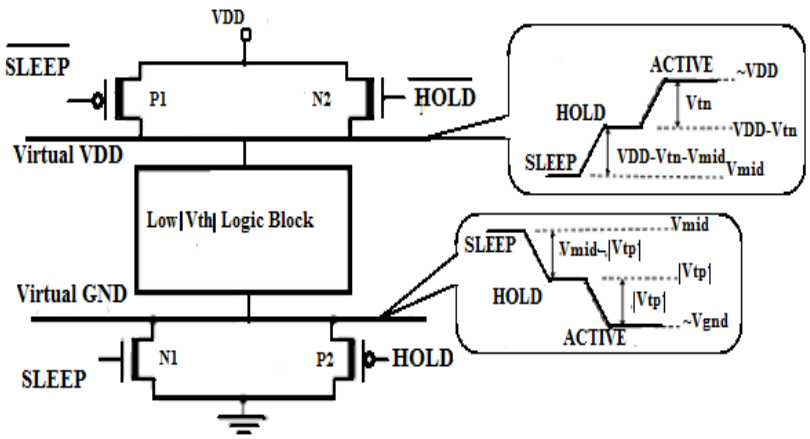

Figure 3 Dual-Switch MTCMOS Technique

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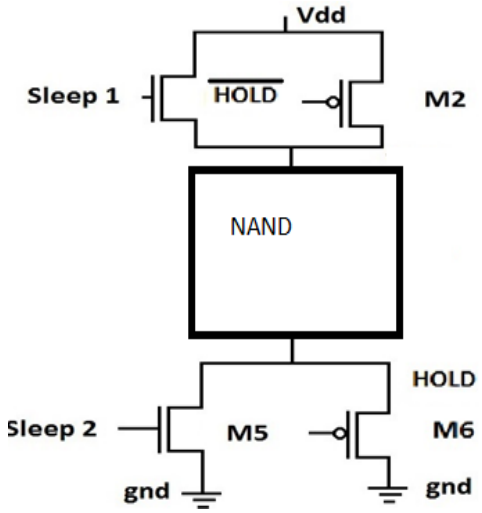

Figure 4NAND with Dual switch technique MOS

In dual switch technique (fig 4), an intermediate HOLD mode is introduced to suppress the ground bouncing noise, similar to Tri mode [4]. It is an alternative method to suppress the ground bounce in gated- &ground structure As shown in "Fig. 3" A high-Vth NMOS transistor is connected in parallel to the header sleep transistor connected in between real power line and virtual power line similarly high-Vth PMOS Transistor is connected in parallel to the footer sleep transistor which is connected in between the real ground and the virtual ground line. In an intermediate HOLD P2 and N2 high Vth transistor turned on and the header (P1) and the footer (N1) are maintained at cut-off mode. In the SLEEP mode, all the transistors i.e Sleep transistors (P1, N1) and Parkr transistor (P2, N2) are turned off which reduced the sub-threshold leakage currents. The voltages maintained at virtual power and ground lines are approximately equal to (Vmid). Before the activation of the circuit, The circuit transitions to the intermediate HOLD mode i.e from the SLEEP mode to the HOLD mode. VDD- Vtn-Vtp voltage is produced between the virtual lines. And from the HOLD mode to the ACTIVE mode transition P1 and N1 are activated. The virtual power line and ground line is charged and discharged to ~VDD and ~Vgnd. HOLD mode reduces the voltage swing range which reduces the amplitude of Ground bouncing noise.

3. SIMULATION RESULTS

Results are obtained on synopsys HSPICE software and models of MosFET from PTM website, i.e. Predictive Technology Model**.** The Adder is implemented on 90nm Technology of MosFET using conventional CMOS technique on Sleep technique, tri-mode and dual-mode technique.

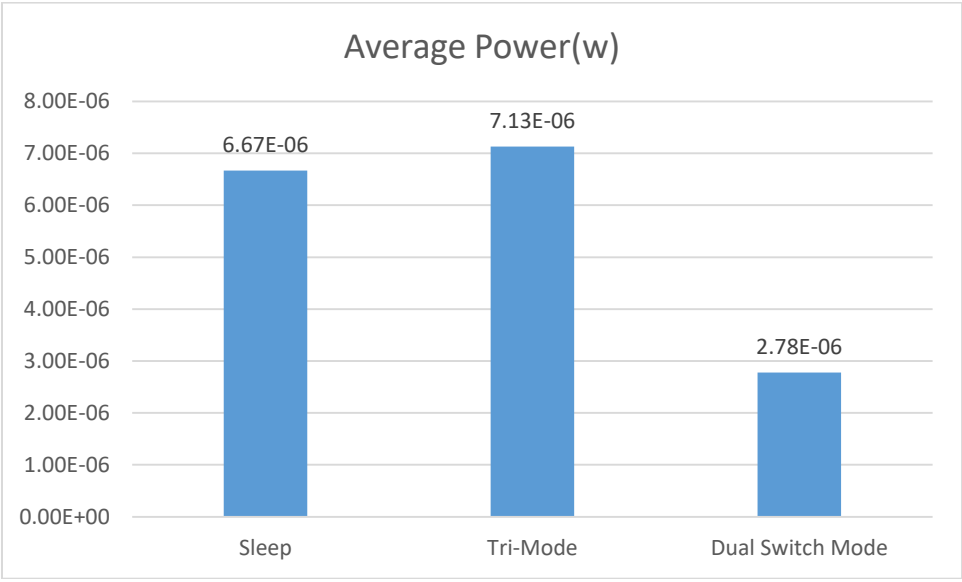

Figure 4.4Average Power

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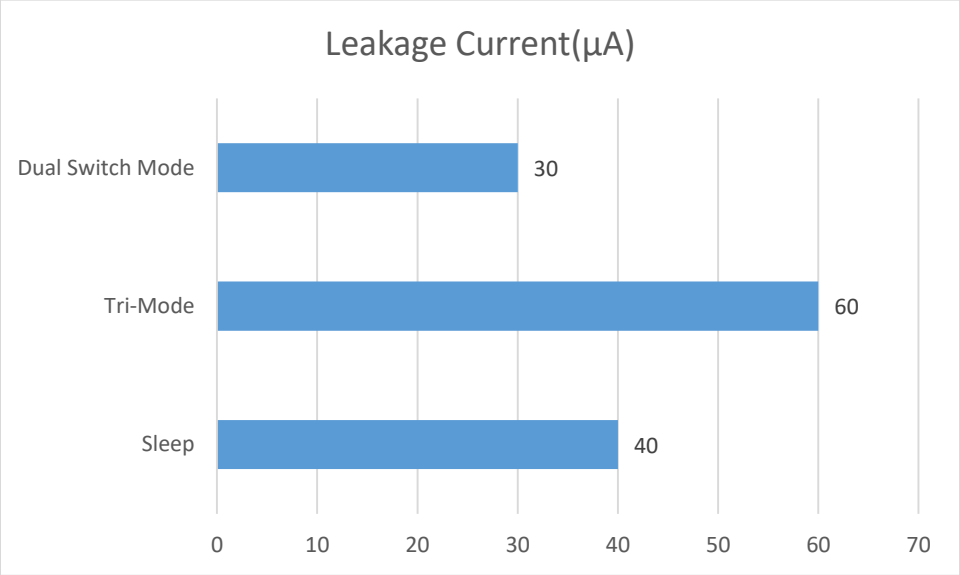

Figure 4.5 Leakage Current

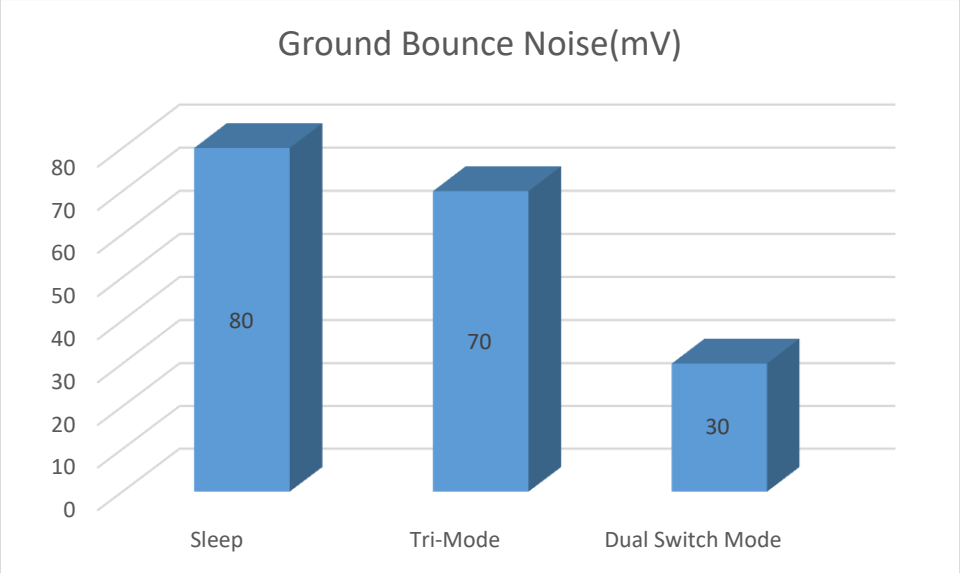

Figure 4.6 Ground Bounce Noise

Figure 4.4, 4.5 and 4.6 represent in chart form improvement in Average Power Consumption, leakage current and ground bounce noise.

Table 4.1 Comparison of different techniques on Ground Bounce Noise

	Sleep	Tri-Mode	Dual Switch Mode
Average Power(w)	6.67E-06	7.13E-06	2.78E-06
Leakage Current(µA)	40	60	30
Ground Bounce Noise(mV)	80	70	30

4. CONCLUSION

- Dual Switch Mode proposed technique best in terms of leakage current and average power and ground bounce.
- 62.5 % ground bounce noise is reduced in power gating dual switch mode when compared to NAND Sleep MOSFET Gate.
- 58.32% average power consumption is increased in dual switch mode.
- Dual Mode technique has the least ground bounce noise.

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