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Optimization Of A Full adder Based On FinFET Technology

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Abstract: In this paper, an adder circuit are designed in which full adder CMOS is included, are designed using MOSFET in 32nm Technology length and in FinFET Technology with 28 transistors in MOSFET and FINFET. Then, they are simulated using HSPICE and the performance parameters of adder such as average power and delay are determined in both FinFET and MOSFET counterpart. It is observed that FAFINFET gives best results in the form of Average Power consumption and delay.

Keywords: Ripple Carry Adder, FinFET, 32nm

1. INTRODUCTION

As the size of transistors has scaled down, so have many digital applications. [5]Cell phones, laptops, sensors, and many other applications all shrunk in size over the last few decades and they are more and more portable.[6] For this to happen, chips in these digital applications have to be designed to optimize the number of transistors used, the fewer the better.[8][9] In this case, pass transistor logic is an attractive solution because a circuit can usually be implemented in pass transistor logics with around half of the number of transistors required for static CMOS implementation.[10][11] However, pass transistor logic allows inputs to be tied to the source and the drain of a transistor, thus create possible situations where NMOS has to drive a logic 1 and PMOS has to drive a logic 0.[12] Since NMOS is not a good pull up device, the output of a pass transistor circuit will suffer from a voltage drop Vth and never achieve a full voltage swing to VDD. With the continuing scaling of supply voltage, this voltage drop cannot be tolerated. [1] The additional back gate of a FinFET gives circuit designers many options. The back gate can serve as a secondary gate that enhances the performances of the front (primary) gate.[14][15] For example, if the front gate voltage is VDD (transistor is ON) the back gate can be biased to VDD to provide bigger current drive, which reduces transistor delay. [3]If the front gate voltage is 0 (transistor is OFF), the back gate can be biased to 0, which raises the threshold voltage of the front gate and reduces the leakage current. [2][3]

2. IMPLEMENTATION OF ADDERS ON MOSFET AND FinFET

Full adder is a unit that adds two numbers and the carry, and generates sum and carry. The full adder circuit adds three one-bit numbers (A,B,Cin) and outputs two one-bit numbers (S,Cout). [7] The logic circuit of full adder is shown in figure 1 and the truth table is shown in table 1.

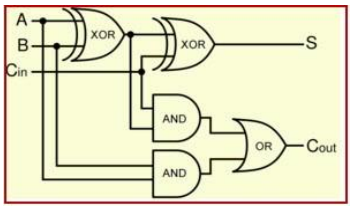

Figure 1: Logic Circuit of Full Adder

Table 1: Truth Table of Full Adder

Input bit for number A	Input bit for number B	Carry bit input C_{IN}	Sum bit output S	Carry bit output C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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The full adder is realized using MOSFETs as shown in figure 2:

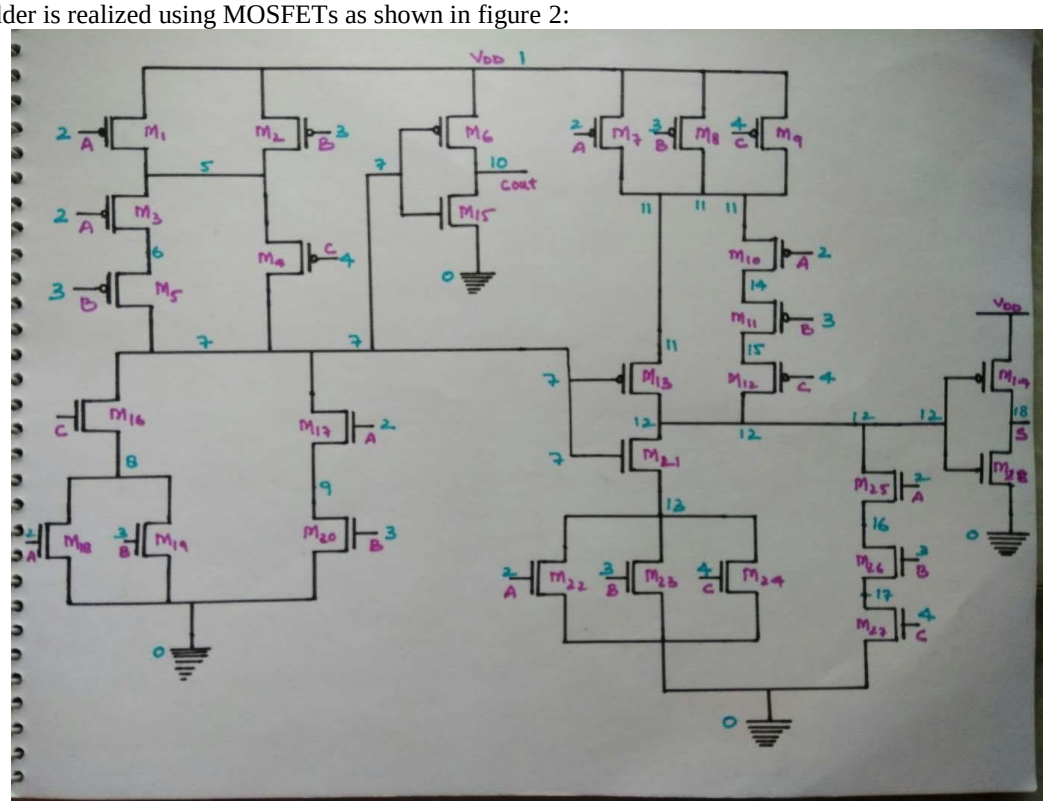

Figure 2: Realization of Full Adder using MOSFETs

The simulated output of full adder is shown in figure 2. In the figure 3 given below, the first three waveforms represent two inputs and carry which is zero here. The fourth waveform gives the carry out and the fifth waveform is the sum obtained. The simulated output of the full adder satisfies the truth table given in table 1.

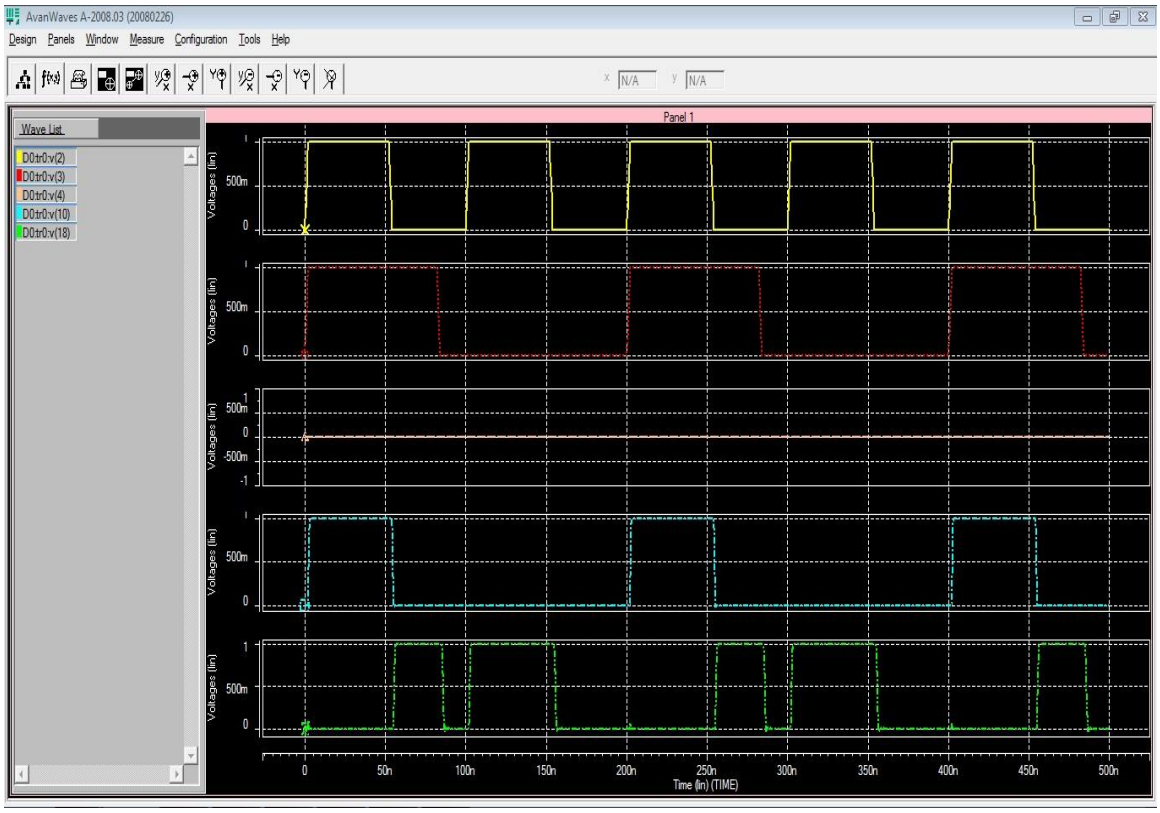

Figure 3: Simulated Output of Full Adder

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3. SIMULATION RESULTS

The average power and the delay have been calculated and are summarized below:

Table 2: Comparison of Delay and Average Power in Adders

	Full Adder MOSFET	Full Adder FinFET
Average Power(w)	7.83E-07	1.50E-07
Delay(s)	4.88E-08	1.16E-10

From the above table, it is clear that the performance of the adders has been improved. It is shown more clearly with the help of charts below:

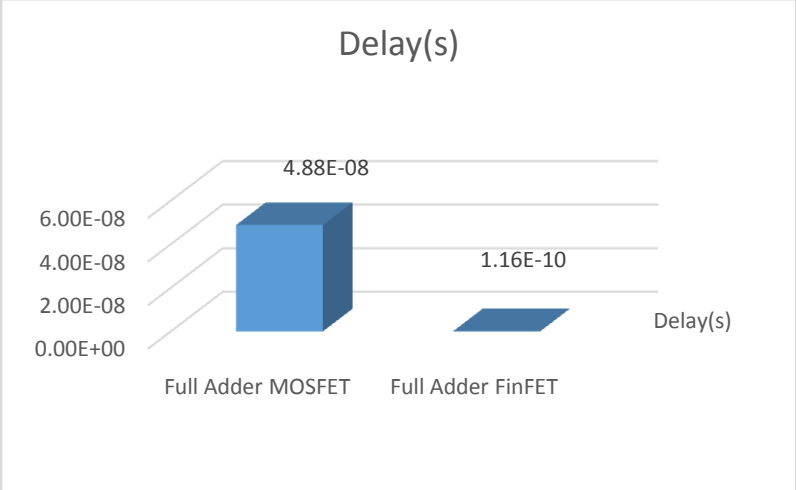

Figure 4: Full Adder Delay

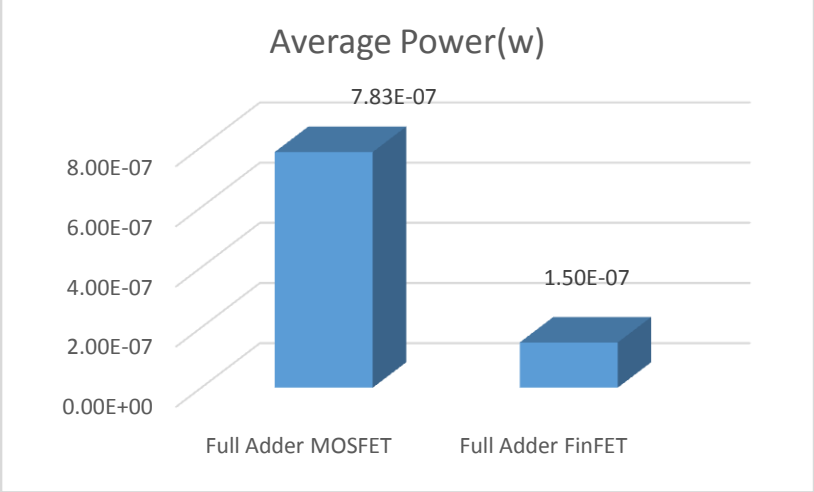

Figure 5: Full Adder Average Power

Figure 4 and Figure 5 clearly show that the performace of FAFinFET is better than FAMOSFET.

4. CONCLUSION

Simulation results show that 28T FA in have improved speed and a lower consumption of average power. The average power and delay is improved by 99.7 % and 80.8% respectively for 28T FAMOSFET and FAFinFET.Technology scaling has provided us with increased circuit performance over the past two decades. However, scaling of conventional transistors beyond the 22nm node is very difficult due to short-channel effects, such as drain-induced barrier lowering (DIBL), sub threshold slope and sub threshold leakage current. DGFETs have emerged as a possible solution to continue technology scaling.Among DGFETs, FinFET have emerged as the most viable solution due to their ease of fabrication.

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