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AXI Interface with a Multiple Master and Slave through Interconnect

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Abstract: AMBA protocols are today the de facto standard for 32-bit embedded processors . The AMBA AXI protocol supports high-performance, high-frequency system designs. It is suitable for high-bandwidth and low-latency designs and provides high-frequency operation without using complex bridges. It provides flexibility in the implementation of interconnect architectures and is backward-compatible with existing AHB and APB interfaces. This Project is aimed at the Verification of the AMBA based AXI protocol has an additional write response channel to allow the slave to signal to the master the completion of the write transaction AXI protocol has an additional write response channel to allow the slave to signal to the master the completion of the write transaction. This slave interface can be used to connect different peripherals into AMBA based processors.

Keywords: Advanced Microcontroller Bus Architecture (AMBA), Advanced Peripheral Bus (APB), AMBA High-performance Bus (AHB), Advanced Extensible Interface (AXI), Sysytem on Chip (SoC)

I. INTRODUCTION

The Advanced Extensible Interface (AXI) is a part of the Advanced Microcontroller Bus Architecture (AMBA) which is developed by ARM (Advanced RISC Machines) company. It is an On- Chip communication protocol. The AMBA AXI protocol supports high-performance, high-frequency system designs. The AXI protocol is suitable for high-bandwidth and low-latency designs. It provides high-frequency operation without using complex bridge. It meets the interface requirements of a wide range of components. AXI protocol provides flexibility in the implementation of interconnect architectures. It is backward-compatible with existing AHB and APB interfaces. The key features of the AXI protocol are that it has separate address/control and data phases & support for unaligned data transfers, using byte strobes. It utilizes burst-based transactions with only the start address issued. It has separate read and write data channels that provide low-cost Direct Memory Access (DMA). It supports for issuing multiple outstanding addresses. It support for out- of-order transaction completion. It permits easy addition of register stages to provide timing closure.

II. LITERATURE REVIEW

The Advanced Microcontroller Bus Architecture (AMBA) is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in System-On-a-Chip (SoC) designs. It facilitates development of multi-processor designs with large numbers of controllers and peripherals. Since its inception, the scope of AMBA has, despite its name, gone far beyond micro controller devices. Today, AMBA is widely used on a range of ASIC and SoC parts including applications processors used in modern portable mobile devices like smart phones.

AMBA was introduced by ARM in 1996. The first AMBA buses were Advanced System Bus (ASB) and Advanced Peripheral Bus (APB) [1&2]. In its second version, AMBA 2, ARM added AMBA High-performance Bus (AHB) that is a single clock-edge protocol [3-5]. In 2003, ARM introduced the third generation, AMBA 3 [6&7], including AXI to reach even higher performance interconnect and the Advanced Trace Bus (ATB) as part of the Core Sight on-chip debug and trace solution.

In [8], a new methodology flow which will allow the visual definition of a complex SoC through instantiation of parametric were proposed Script based automation helps in integrating any IP with any configurations, selects relevant and corresponding Verification IPs (in-house developed-if Design IPs are standard) , uses suitable Bus rappers (OCP, EBI, Avalon, Micro Blaze, Pico Blaze, PIF, AXI, AHB, APB, Generic and others) and stitches all the components design as well verification (synthesizable test bench components) together and making use of TLMs, BFM (replacing CPUs with Master BFMs) or Process Core based designs creates an CSOC environment. The framework reduces the time to build integration and verify the functionality-it also has the complete set up from assembler to DFT. The main perspective of the complete CSOC system is that it not only integrates various designs IPs but also integrates

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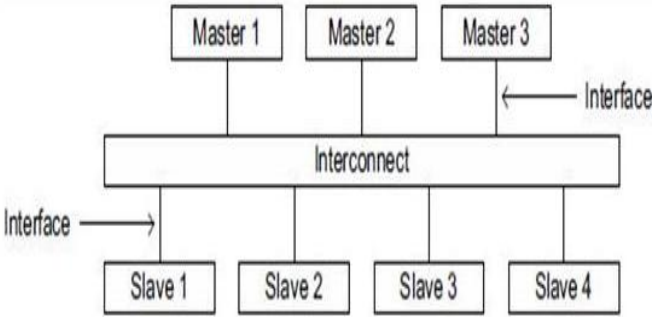
corresponding inbuilt standard VIPs (Verification IPs) that are needed to verify a SoC in real life. These VIPs sit on the same bus that is inside the SoC and share the bus with various Design IPs. Advanced microcontroller bus architecture (AMBA) protocol family provides metric-driven verification of protocol compliance, enabling comprehensive testing of interface intellectual property (IP) blocks and system-on-chip (SoC) designs. The AMBA advanced extensible interface 4 (AXI4) update to AMBA AXI3 includes the following: support for burst lengths up to 256 beats, updated write response requirements, removal of locked transactions and AXI4 also includes information on the interoperability of components. AMBA, AXI4 protocol system supports 16 masters and 16 slaves interfacing. The design is implemented using Verilog- HDL [11-13].

III. PROPOSED METHOD

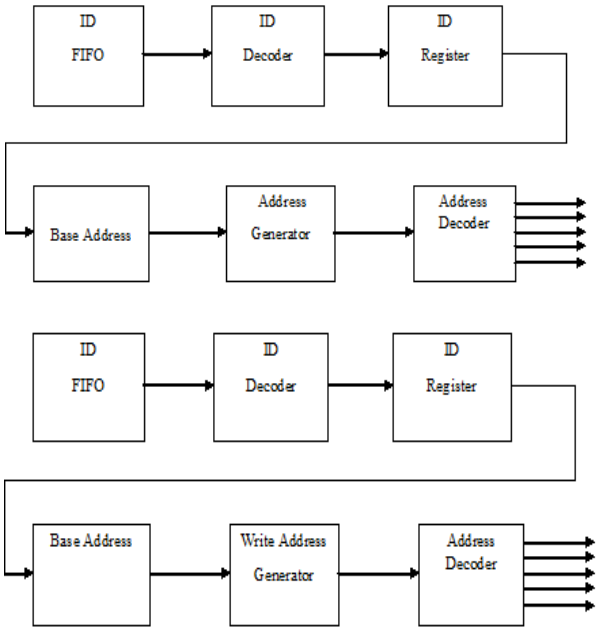
A typical system consists of a number of master and slave devices connected together through the Interconnect. The AXI protocol provides a single interface definition, for the interfaces:

- Between a master and the interconnect
- Between a slave and the interconnect
- Between a master and a slave.



3.1 AXI System Topology

The AXI protocol is burst-based and defines the following independent transaction channels: Read Address Channel, Read Data Channel, Write Address Channel, Write Data Channel and the Write Response Channel. An address channel carries control information that describes the nature of the data to be transferred. The data is transferred between master and slave using either: A write data channel to transfer data from the master to the slave. In a write transaction, the slave uses the write response channel to signal the completion of the transfer to the master. A read data channel to transfer data from the slave to the master. The AXI protocol permits address information to be issued ahead of the actual data transfer. It supports multiple outstanding transactions. It also supports out-of-order completion of transactions.



3.2 Read and Write address Channel

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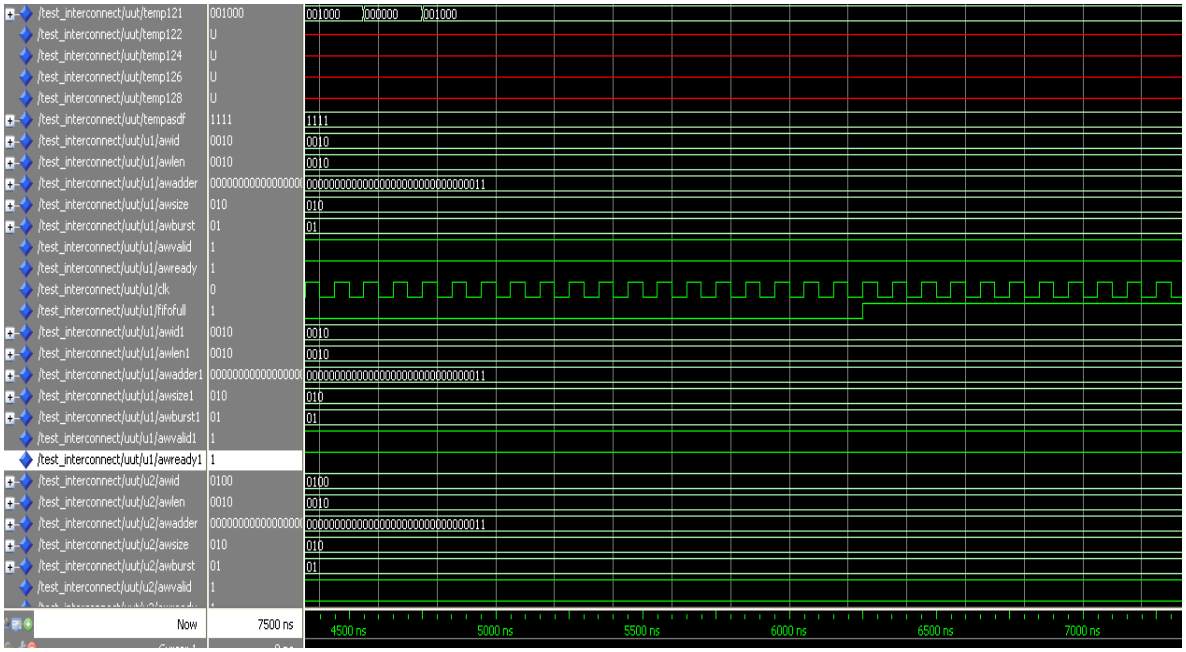
IV. SIMULATION AND RESULTS

Simulation is carried out Modelsim 6.5e Simulator and syntheses is done using Xilinx 13.1

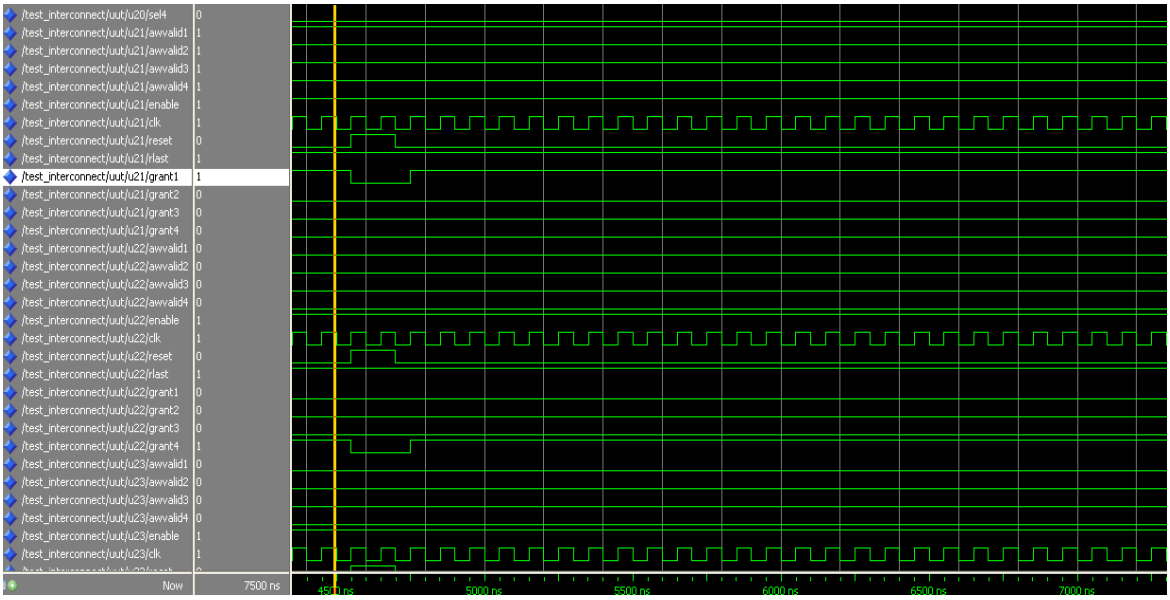
Master :



4.1 Simulation waveform for Master

Here the simulation of Master interface has been shown in master as the awvalid & fifofull gets = to 1 & equal to 0 then signal bit given to awvalid port will be transferred to the awavlid similarly other controlling signal like awid,awlenawadder,awsize,awburst will be transferred to their respective signal.

Arbiter



4.2 Simulation waveform for arbiter

The waveform of arbiter is being shown in which as if rlast='1', enable='1' & if awvalid1='1' then grant1<='1'; and if awvalid is not equal to one the then arbiter will check wether awvalid2 is equal to one or not if awvalid2 is equal to one then arbiter will assert the Grant2 high and other grant signal will be equal to "0" then else again awalid3 will be

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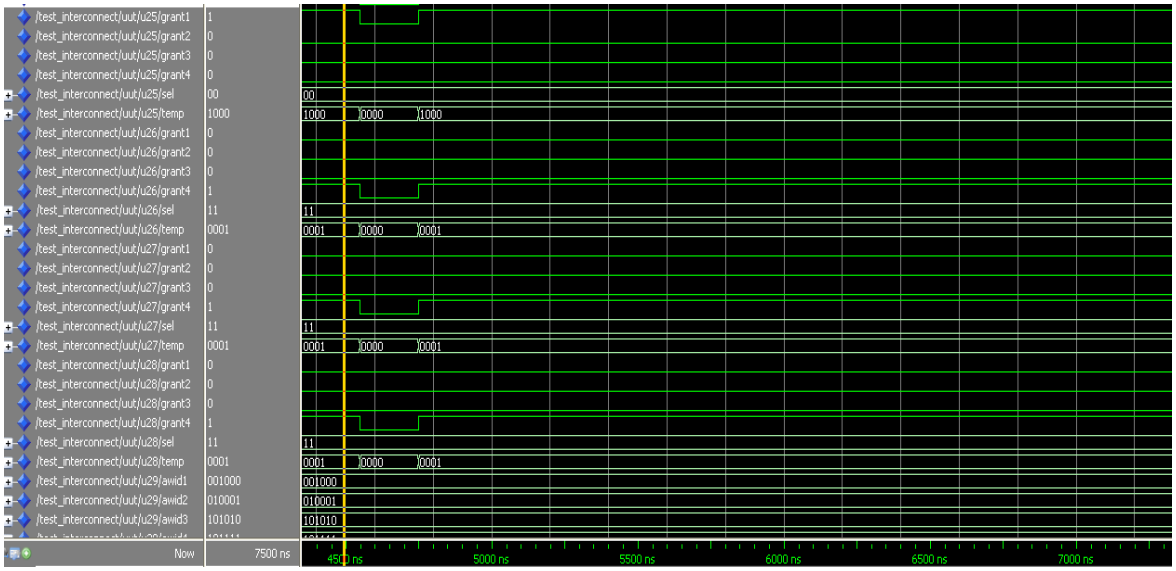
checked wether that is equal to one or not if Awalid3 is equal to one then grant3 will asserted as high in a similar way on the basis of fixed priority arbiter selects the Master.



4.3 Simulation waveform for encoder

In above simulation result, encoder simulation has been shown in wave. It is shown that if grant1 is asserted as high then sel signal will be equal to "00" then if grant2 is asserted as high then sel signal will be equal to "01"and if grant3 is asserted as high then sel signal will be equal to "10" and if grant4 is asserted as high then sel signal will be equal to "11".

CONCLUSION

We have implemented AXI 2.0 protocol which removes the limitation of communication architecture, which efficiently interface with multiple master and slave otherwise reduce the speed of data transfer in System on chip.

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BIOGRAPHY

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