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High Efficiency Two-stage ZVS AC / DC Converter with PFC

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Abstract: A High Efficiency Double–Stage AC-DC Converter is introduced and simulated, which can be used in Vehicle charging application. Front–end Converter is a half-bridge Zero Voltage Switching (ZVS) AC-DC with Power Factor Correction (PFC) topology. For improved efficiency and reduction of stress SiC MOSFET could be used and also high frequency switching could be possible thus by reducing conduction and switching losses. The Second-stage is a LLC resonant DC-DC Converter that help in achieving ZVS. The proposed topology is verified by simulating the model in MATLAB.

Keywords: ZVS; PFC; Double-Stage; High Efficiency, MATLAB

I. INTRODUCTION

Large use of Electric Vehicles(EV) are limited by the limitations in on-board charger development and efficiency. Size reduction, lightness, improved efficiency should be achieved for saving the space and load on EVs. A double - stage AC - DC Converter topology with PFC and an isolated DC-DC stage together comprise of achieving high power factor and reduced current ripple. Past PFC topologies has a diode bridge and a boost converter topology with three or more semiconductor devices for the current traveling path, all that leading to large conduction losses and switching losses as well. Bridgeless PFC topology is a concept without diode bridge rectifier, which helped to reduce the device in the current travelling path. But all among them, the half-bridge PFC converter topology becomes the simplest in structure that has the lesser number of devices in the path of current. So, thus concluded with this topology for achieving the higher efficiency in AC-DC conversion.

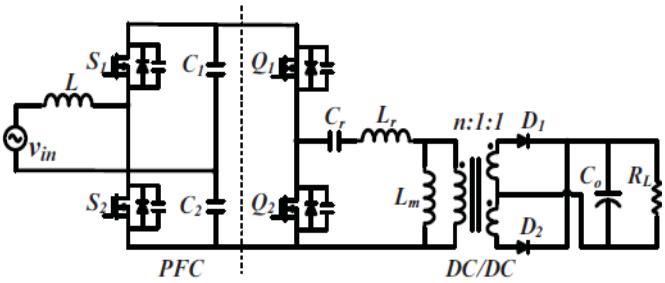

Fig.1 The proposed ZVS Double-stage AC/DC Converter

For achieving ZVS cascading a DC-DC stage with the AC- DC half bridge stage will help and soft switching is achieved for MOSFET's on primary side under every conditions of load. It also provides the wide range of input and output voltage and ZCS of diode at secondary under different condition which are required for on- board charging. The output voltage Vo in half-bridge circuit, will be double the value of the peak input voltage at least for the proper working boost operation. Therefore, nominal single phase voltage 230 V input range, output voltage will result to higher voltage greater than 760V. Thus this high voltage stress could be tackled by introducing SiC MOSFET which have higher voltage rating and frequency bearing with also a lesser on-stage resistance.

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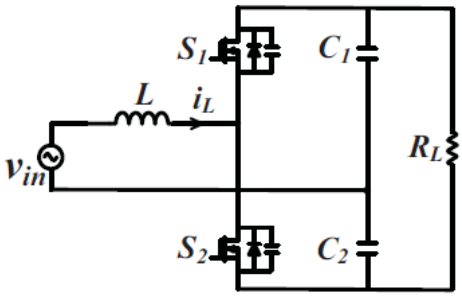
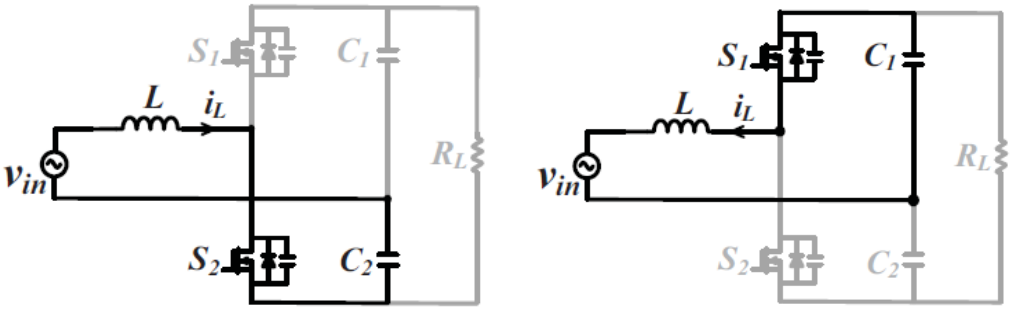


Fig.2 Half bridge PFC topology

Fig.2 shows a half-bridge PFC converter and it is simplified to form different equivalent circuits for every single switching cycles are shown.Only single switch conducts during the switching cycle, thus leading to lower conduction losses. But high stress voltage is observed when the switch is in off state , therefore inorder to reduce the stress voltage SiC devices are used. Due to the new development in wide band gap of semiconductor devices which includes silicon carbide (SiC) and gallium nitride (GaN), which opens a new era in power electronics improving the efficiency and its power density. Here for an input of 230V rms , expecting nearly 800V stress across the single switch , by considering the safety factor also the PFC half bridge converter can use 1200V SiC MOSFETs. These devices are selcted accordingly to the peak overshoot of the devices under its working conditions.Intial PFC stage hysterisis current control stratergy is used for improving PF.



(i) S_2 on, S_1 off (ii) S_1 on, S_2 off

Fig.3 Modes of operation of half-bridge PFC Converter

II. CONTROL STRATEGY OF ZVS HALF BRIDGE PFC

A. Hysterisis Current Control (HCC)

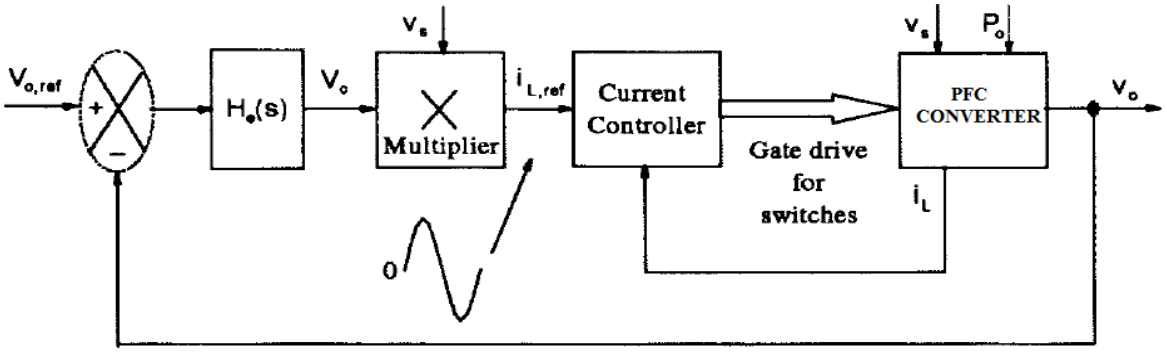


Fig.4 HCC for PFC converter

In hysteresis current control technique, input current i_L kept within a band width about a reference current $i_{L,ref}$ thus by approximately switching the mosfet switches S1 and S2.

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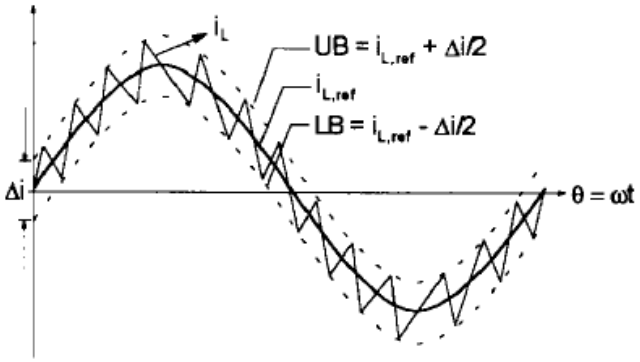
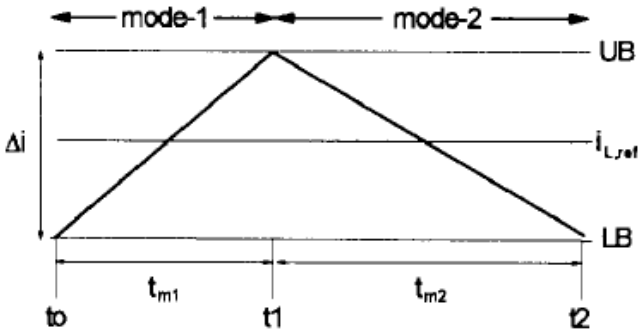


(i) Over one line cycle

Basically two mode of operation takes place, when the current through inductor hits the lower bound at time t_0, S1 turns on.



(ii) Over one switching cycle

Fig.5 Current waveforms in HCC technique

If i_L greater than zero, S1 conducts, D1 conducts otherwise. But when inductor current has a positive slope as the capacitor voltage becomes greater than the line voltage peak (in boost operation) and the inductor current hits upper band at t_1 time S2 conducts , otherwise depending on the polarity of inductor current D2 turns on.

B. Computation of Switching Frequency and Duty Cycle

The expression for time t_{m1} and t_{m2} are

$$t_{m1} = \frac{L\Delta i}{(V_p \sin\theta + \alpha V_0)} \quad (1)$$

$$t_{m1} = \frac{L\Delta i}{(V_p \sin\theta + (1-\alpha) V_0)} \quad (2)$$

Expression for switching frequency is given by:-

$$f_s = 4 f_{s\max} (\alpha + \frac{1}{M}\sin\theta)((1-\alpha) - \frac{1}{M}\sin\theta) \qquad f_s = 4 f_{s,max} (\propto + \tfrac{1}{M} sin\theta)((1-\propto) - \tfrac{1}{M} sin\theta \quad (3)$$

Where

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$$M = \frac{V_o}{V_p} > 2 \quad (4)$$

thus

$$f_{smax} = \frac{V_0}{4L_m i} \quad (5)$$

Maximum frequency occurs at an angle shown below,

$$L_m < \frac{t_{dead}}{16 f_{sw} . C_{oss}}$$

$$\theta = \sin^{-1}\{M(0.5-\alpha)\} \quad (6)$$

Thus the above equation denotes that maximum frequency occurs at zero crossing of line voltage. The equation shown below is the minimum switching frequency which occurs at peaks of line voltage and is given by

$$f_{s,\min} = 4 f_{s,\max}\left(\alpha + \frac{1}{M}\right)\left((1-\alpha) - \frac{1}{M}\right) \quad (7)$$

for

$$\theta = \frac{\pi}{2} + 2n\pi \quad (8)$$

Where n=0,1,2,3….etc.
The duty cycle ‘d’ for the switch S1 could be given as

$$d = \frac{t_{m1}}{t_{m1} + t_{m2}} = \left((1-\alpha) - \frac{1}{M}\sin\theta\right) \quad (9)$$

The duty cycle becomes maximum at negative peak and become minimum at positive peak of line voltage. The minimum and maximum duty cycles could be given as

$$d_{\max} = \left(1 - \alpha + \frac{1}{M}\right) \quad (10)$$

$$d_{\min} = \left(1 - \alpha - \frac{1}{M}\right) \quad (11)$$

Thus duty cycle for switch S2 is given as

$$d' = 1 - d = \left(\alpha + \frac{1}{M}\sin\theta\right) \quad (12)$$

III. DESIGN EQUATIONS FOR LLC CONVERTER

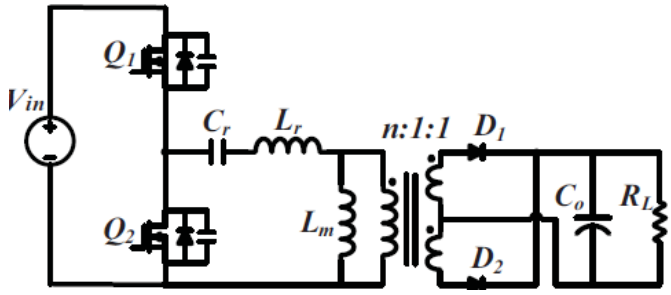

Fig.6 Half bridge LLC Converter

The DC-DC LLC resonant converter is introduced in the second stage which help to attain and ensure ZVS operation of the converter switches.Basically two mode of operation when Q1 on , Q2 off and vice versa.the switching frequecy should be choosen such that it is above the resonant frequency to occur and thus to achieve ZVS operation of the

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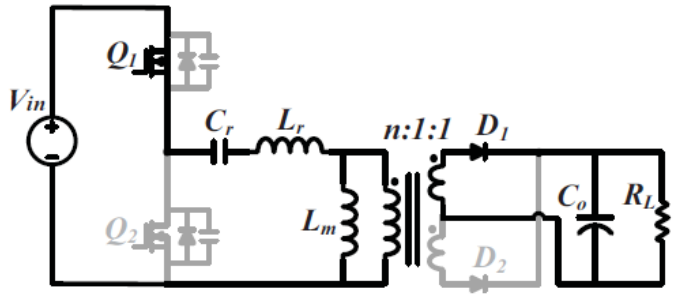
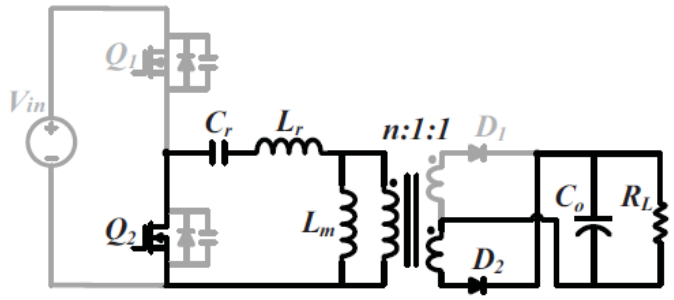
converter switches. In this stage basically it allows to isolate and provide a required output voltage for the battery to get charged at different modes. This stage should be carefully designed for the proper operation of the converter to occur,



(i) Q1 on, Q2 off

For a input DC voltage of 800V as V_{in} , we can use SiC MOSFETs with breakdown voltage of 1200V are selected by considering the possible overshoot voltage that could cause across the switches Q1 and Q2.Selection Q value and the graph versus Q factor and at different gain is plotted in the Fig.8.



(ii) Q2 on, Q1 off

Fig.7 Equivalent switching for different switching modes

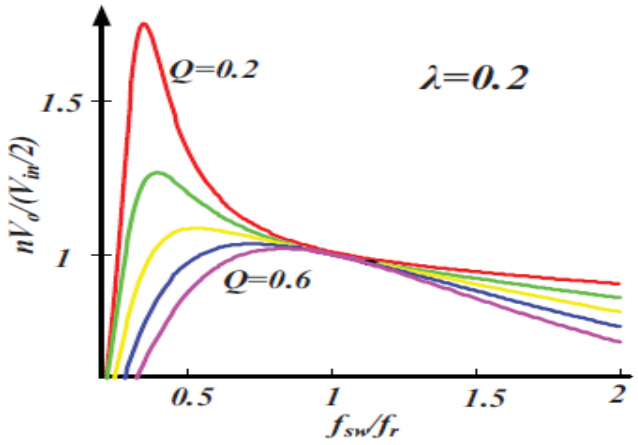


Fig.8 Gain characteristics for different Q values

The characteristics shown above for the half bridge LLC converter is based on first harmonic approximation(FHA) and thus these variables could be defined as

$$Q = \frac{\sqrt{L_r / C_r}}{R_{ac}} \qquad (13)$$

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$$R_{ac} = \frac{8n_r^2 R_L}{\pi^2} \quad (14)$$

$$\lambda = \frac{L_r}{L_m} \quad (15)$$

$$f_r = \frac{1}{2\pi\sqrt{L_m C_r}} \quad (16)$$

For achieving Zero voltage switching (ZVS), thus magnetic inductance could be obtained by

$$L_m < \frac{t_{dead}}{16 f_{sw} C_{oss}} \quad (17)$$

here, f_{sw} is the switching frequency, the junction capacitance is denoted by C_{oss} C_{oss} of the primary MOSFETs. The resonant capacitor and inductor C_r C_r and L_r are chosen according to the Fig.8 for meeting the voltage gain under every load conditions with switching frequency f_{sw} and f_r f_r, resonant frequency.

IV. SIMULATION AND RESULT

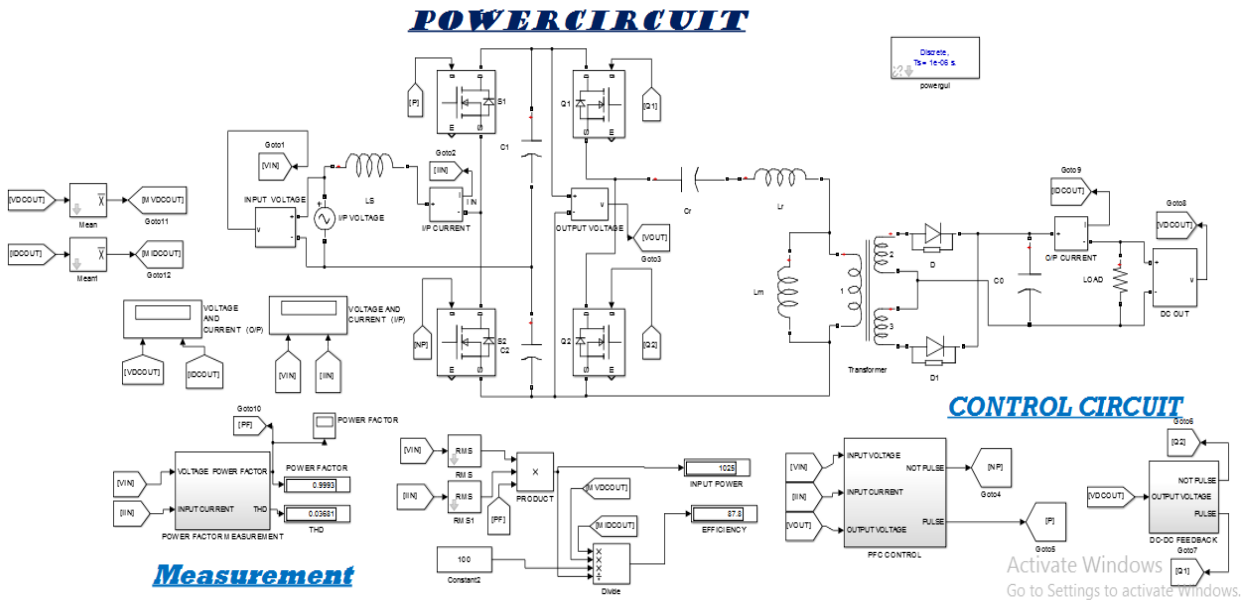

Fig.9 Matlab Simulation diagram of two stage AC-DC converter

The above shown is the simulation diagram in MATLAB in which both the stages are simulated with designed values. The converter is designed for an AC input of 50V peak and an output battery charging voltage of 24 V, 3.1A is achieved and is confirmed with simulation.

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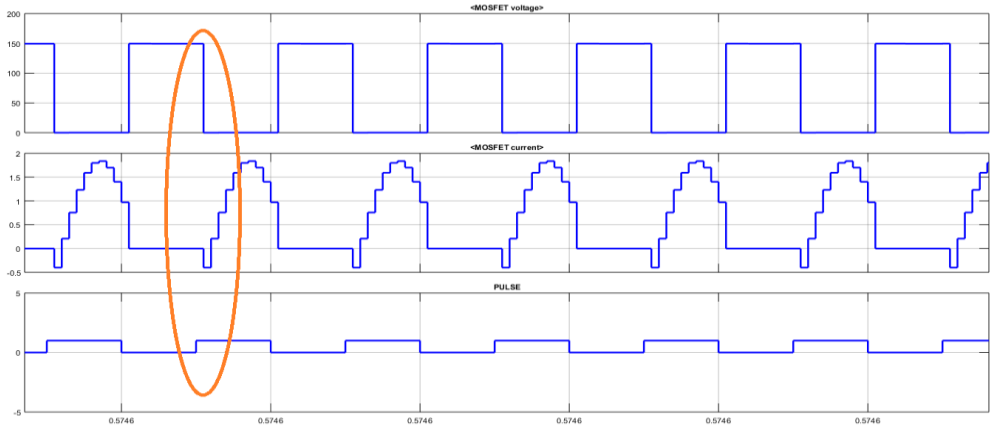

Fig.10 ZVS achieved across the MOSFET switch

As per the topology the second stage is a LLC converter in which Zero voltage switching is achieved. The figure 10 shows the achievement of ZVS across the switch. Thus a loss less power conversion is achieved with this converter for charging a low power battery with a rating of 24V, 3.1A.

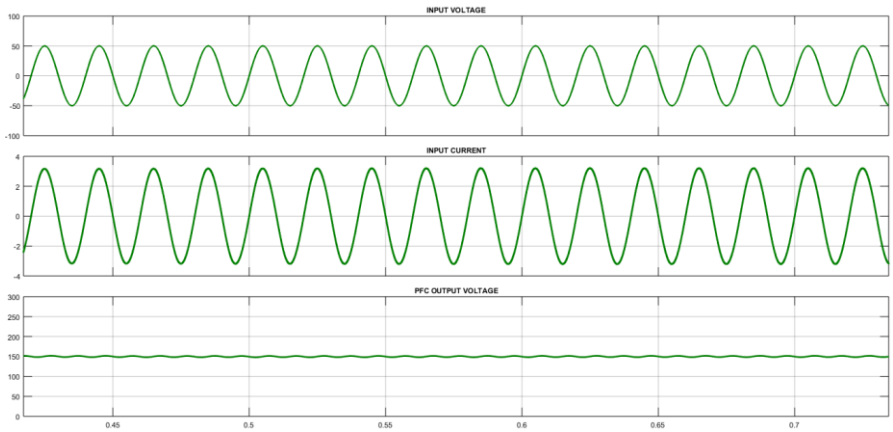

Fig.11 PFC achieved in the first stage of the converter topology

The first stage as explained earlier is Power Factor Correction AC-DC conversion stage in which here the converter acheives 0.99 power factor. The above figure 11 shows the power factor corrected input current. First stage of conversion has implemented using hysterisis current control technique.

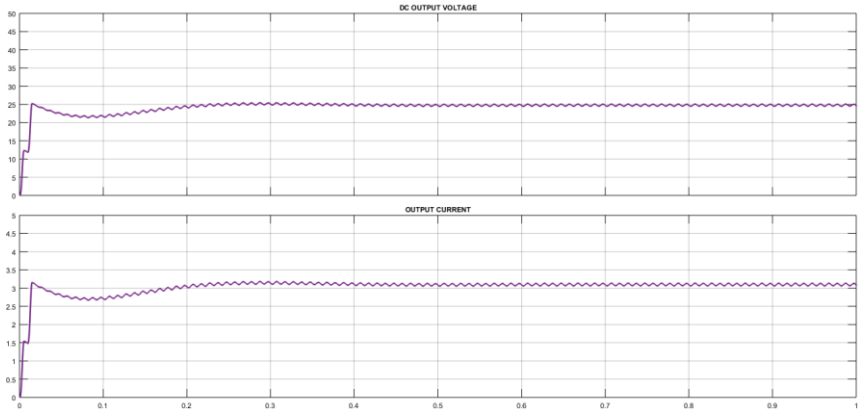

Fig.12 Battery charging voltage and charging current (Final output of the converter)

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Figure 12 show the output voltage and current of the LLC converter. An output power of 75 W low power battery charger is simulated for easiness. The design is applicable high power also as explained in the above section. Handling high voltage needs more care in selection of MOSFET switches as high voltage stress or reverse voltages has to be with-stand.

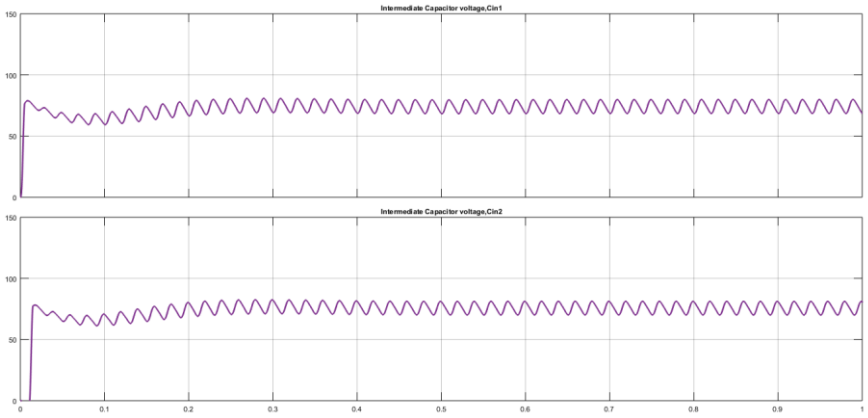

Fig.13 Intermediate DC bus capacitor voltage

The figure shows the intermediate DC bus capacitor voltage. The capacitor filters the voltage and provide a DC voltage into the input of the second stage of the DC-DC LLC converter. Thus this voltage is a very high voltage compared to the given maximum input AC voltage as the voltage boosts accordingly for about at least 2 times the given input voltage.

Table: 1 Simulation Parameters

SL N.o	Parameters	
	Element	Specification
1.	Source inductance	1.27 µH
2.	MOSFET,IRF840	500V, 8A
3.	Intermediate Capacitor, C_{o1}	1000 µF
4.	Resonant Capacitor, Cr	33 nF
5.	Resonant inductor, Lr	78µH
6.	Output filter capacitor, Co	1000 µF
7.	Load resistance, Ro	7.8Ω

V. CONCLUSION

A 1-phase converter with two-stage conversion with an efficiency of about 98% is achieved. The front-end converter resembles a pure power factor correction with Hysteresis current controlled technique. The final stage of conversion is the DC-DC conversion with ZVS which contributes the efficiency improvement of the converter and generation of proper voltage and power rating for charging a battery module. By using Sic mosfet the issue of high voltage stress in the front end conversion can be rectified for hardware implementation of the converter.

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