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# Resonant Parallel Operated Buck - Boost Converter in ZVS mode with Voltage Regulation

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**Abstract:** This paper presents a voltage regulated two stage buck-boost converter with a soft switching operation. Many dc-dc converters are available in which the converters are divided into several types depending on the increase or decrease of the output voltage level with respect to the input voltage. This paper deals with a soft switched buck boost converter with voltage regulation in ZVS mode. The efficiency of the converter is the main issue which is reduced through zero voltage soft switching. Other issue regarding the dc to dc converters are the lack of voltage regulation, which is reduced through closed loop feedback circuit. Also, utilizing only one inductor as an extra element to achieve this goal makes the converter more economical and reliable with a simpler structure. The main feature of the project is its high frequency resonance operation. Frequency controlled operation enables more efficient converter characteristics.

**Keywords:** Resonant Converter, ZVS Operation, Buck Boost Converter

## I. INTRODUCTION

Nowadays DC-DC converters are needed widely. In such case many converters are practiced. These types of converters are divided into several types depending on the increase or decrease of the output voltage level with respect to the input voltage. The main application of step-up/down converters is in regulated DC power supplies, where the output negative polarity may be desired with respect to the common terminal of the input voltage supply. The efficiency of DC-DC converters is an important issue. In this regard, various control strategies and converter topologies are presented for the soft switching operation of the converters to achieve minimum switching losses leading to more efficient operations. Soft switching techniques utilizing the features of zero-voltage or zero-current switching substantially reduce the switching losses. This is a double-deck buck-boost converter with an effective ZVS technique. The operational principles of the converter are surveyed and summarized in eight modes. It is shown that the switching process can perform with the minimum losses by applying the gate signals at particular time interval. Moreover, it is also concluded that utilizing of two converters in parallel causes less ripple in the output load voltage. In addition, the fact of using only one inductor as an extra element to achieve the main goal of this converter suggests that the converter is more economical than the soft switched converters by adopting coupled inductors or transformers. Interleaved converters are utilized in many applications and provide many advantages such as increasing efficiency reducing the voltage and current ripple, and supplying more load power [5].

In the early periods conventional PWM power converters were operated in a switched mode operation. Power switches have to cut off the load current within the turn-on and turn off times under the hard switching conditions. Hard switching refers to the stressful switching behavior of the power electronic devices. During the turn-on and turn-off processes, the power device has to withstand high voltage and current simultaneously, resulting in high switching losses and stress. Dissipative passive snubbers are usually added to the power circuits so that the dv/dt and di/dt of the power devices could be reduced, and the switching loss and stress are diverted to the passive snubber circuits. However, the switching loss is proportional to the switching frequency, thus limiting the maximum switching frequency of the power converters. The stray inductive and capacitive components in the power circuits and power devices still cause considerable transient effects, which in turn give rise to Electro Magnetic Interference (EMI) problems.

Increasing the frequency of operation of power converters is desirable, as it allows the size of circuit magnetic and capacitors to be reduced, leading to cheaper and more compact circuits. However, increasing the frequency of operation also increases switching losses and hence reduces system efficiency. One solution to this problem is to replace the "chopper" switch of a standard SMPS topology (Buck, Boost etc.) with a "resonant" switch, which uses the resonances

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of circuit capacitances and inductances to shape the waveform of either the current or the voltage across the switching element, such that when switching takes place, there is no current through or voltage across it. A circuit employing this technique is known as a resonant converter (or, more accurately, a quasi-resonant converter, as only part of the resonant sinusoid is utilized). A Zero Current Switching (ZCS) circuit shapes the current waveform, while a Zero Voltage Switching (ZVS) circuit shapes the voltage waveform.

In a ZC resonant switch, an inductor Lr is connected in series with a power switch S in order to achieve Zero-Current Switching (ZCS). If the switch S is a unidirectional switch, the switch current is allowed to resonate in the positive half cycle only. The resonant switch is said to operate in half-wave mode. If a diode is connected in anti-parallel with the unidirectional switch, the switch current can flow in both directions. In this case, the resonant switch can operate in full-wave mode. At turn-on, the switch current will rise slowly from zero. It will then oscillate, because of the resonance between Lr and Cr. Finally, the switch can be commutated at the next zero current duration. The objective of this type of switch is to shape the switch current waveform during conduction time in order to create a zero-current condition for the switch to turn off.

In a ZV resonant switch, a capacitor Cr is connected in parallel with the switch S for achieving Zero-Voltage Switching (ZVS). If the switch S is a unidirectional switch, the voltage across the capacitor Cr can oscillate freely in both positive and negative half-cycle. Thus, the resonant switch can operate in full-wave mode. If a diode is connected in anti-parallel with the unidirectional switch, the resonant capacitor voltage is clamped by the diode to zero during the negative half-cycle. The resonant switch will then operate in half-wave mode. The objective of a ZV switch is to use the resonant circuit to shape the switch voltage waveform during the o_ time in order to create a zero-voltage condition for the switch to turn on.

## II. CIRCUIT CONFIGURATION AND ANALYSIS

A resonant parallel buck-boost converter with an effective ZVS technique is presented. The operational principles of the converter are surveyed and summarized in eight modes. In this converter the switching process can perform with the minimum losses by applying the gate signals at particular time intervals. Moreover, the utilizing of two converters in parallel causes fewer ripples in the output load voltage. The inductor placed between two parallel converters is called the interleaved inductor and displaces the resonating current between two converters at particular time intervals in order to perform the soft switching operation. In addition, the fact of using only one inductor as an extra element to achieve the main goal of this converter suggests that the converter is more economic.al than the soft switched converters by adopting coupled inductors or transformers.

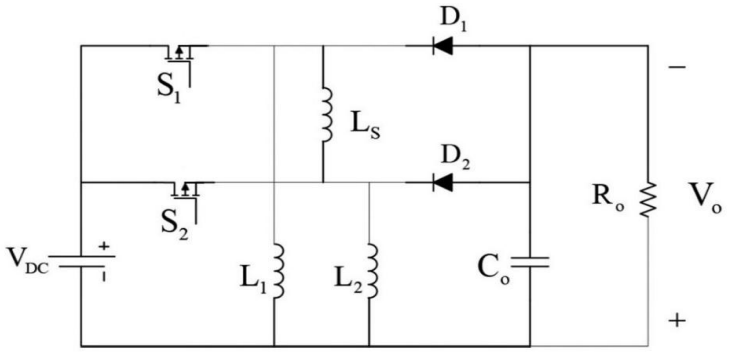


Figure 1: Configuration of parallel buck-boost converter

The configuration of the double deck buck boost converter is depicted in Figure 1. It is composed of two identical buck-boost converters working in parallel. The source and the output capacitor Co are shared between two converters. The interleaved inductor Ls is placed in parallel with two switches. This element plays an important role in main plot of the soft switching manner of the converter. It discharges the intrinsic capacitances of the switches by creating a resonant circuit. Then, the switching could be done when the intrinsic anti parallel diodes of the switches conduct the negative half-cycle of this resonating current and the voltage on the switches is clamped at zero. Two power MOSFETs, $S_1$ and $S_2$, are adopted high frequency switching with the same switching frequency. The duty ratio D for each of the switches is identical and slightly greater than 0.5 to create overlapping intervals. It is assumed that the converters operate in the continuous current mode (CCM). The equivalent circuit shown in Figure 3.2 is utilized to

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describe the procedure of the converter operation. To simplify the analysis, it is considered that the currents of inductors $L_1$ and $L_2$ and also the output currents are constant, and modelled by a constant current source, as shown in Figure 3.2. Moreover, the output voltage is assumed to be almost fixed because of the large output capacitor $C_0$. To describe how the ZVS is achieved, the detailed models of the power MOSFETs are utilized.

They consist of the intrinsic anti parallel diode and capacitance in parallel with an ideal switch. The operation procedure of the converter can be presented in eight modes depending on the different statuses of the switches. Because the two buck-boost converters are completely identical, all the circuit elements such as $L_1$, $L_2$,$C_{S1}$, and $C_{S2}$ have the same values. In all stages, the forward voltage drops on diodes $D_1$ and $D_2$, and switches $S_1$ and $S_2$ are considered negligible. The equivalent circuit of each mode is shown in Figure .2. The elements which are conduct are distinguished with the elements that are not. The theoretical waveforms related to each mode are demonstrated in figure 3.7.

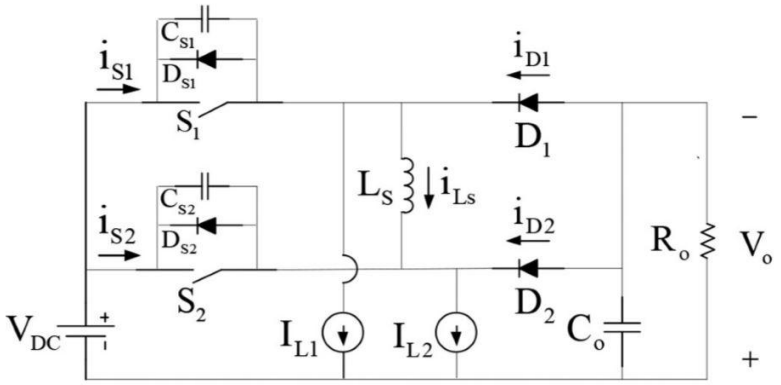


Figure 2: Equivalent circuit of the double deck converter

## III. VOLTAGE REGULATION

Normal open loop system shows variation in output voltage with change load. In order to regulate the output voltage a closed loop feedback is required. The output voltage is compared with a reference voltage and the error is given to the ADC of the controller. The gate pulse is generated in accordance with the error voltage and the pulse frequency is varied accordingly. The closed loop logic is shown in figure 3.

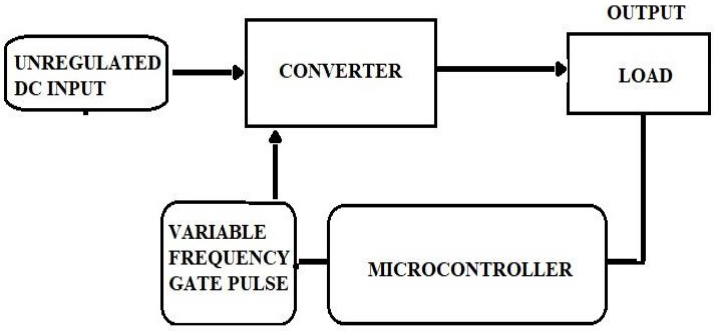


Figure 3 Schematic block diagram of closed loop voltage regulation

A. Modes of Operation

**i) Mode 1:** $t_0 < t < t_1$ **:** to describe the first mode, it is considered that the diode $D_2$ freewheels the load current $I_0$. So, according to Figure 4, the diode $D_2$ current is equal to $I_{L1}+I_{L2}$ and the current $I_{L1}$ passes through the inductor Ls reversely. Mode I begin when the switch $S_1$ is closed and $D_2$ freewheeling current is decreasing to zero. Therefore, the voltage $V_{DC}+V_O$ which was clamped on the capacitor $C_{S2}$ is imposed on the inductor $L_S$ by the polarity depicted. Therefore, the inductor current $I_{L2}$ increases linearly from $-I_{L1}$ to $I_{L2}$ as depicted in Figure 3.8. Meanwhile, $I_{S1}$ increases

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linearly simultaneous with the $I_L$S increment. As reaches zero, the current $I_{L1}$ passes through the switch $S_1$. When $I_{LS}$ rises up to $I_{L2}$, $I_{S1}$ reaches $I_{L1}$+$I_{L2}$. At the end, the freewheeling current of $D_2$ reaches zero, as shown in Figure 8. On whole, $V_{CS2}$ is considered to be constant and equal to $V_{DC}$+$V_O$ in this process. Figure 3.4 shows the equivalent circuit diagram of this mode.

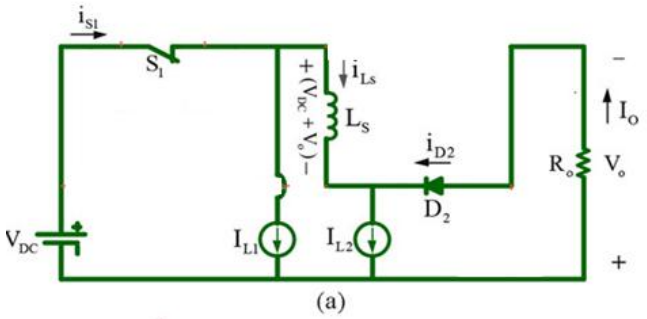


Figure 4: Mode 1 operation

**ii) Mode 2:** $t_1 < t < t_2$ **:** this mode starts when the freewheeling current of $D_2$ reaches zero. Then, a resonant circuit is formed between $C_{S2}$ and $I_{LS}$. This resonating current discharges the capacitor $C_{S2}$ which was clamped on $V_{DC}$+$V_O$ before entering this mode. After $V_{CS2}$ decreases to zero, $D_{S2}$ will be forward biased to conduct the resumption of the resonant current cycle. Now, both of the resonant current and the inductor current flow through the interleaved inductor $L_S$ therefore, $I_{LS}$ becomes a small bit larger than $I_{L2}$, as illustrated in Figure 8. Figure 5 shows the equivalent circuit diagram of this mode.

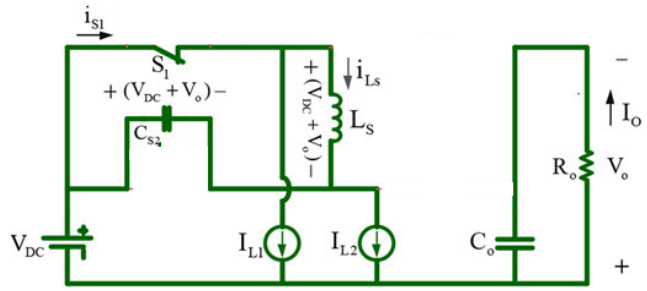


Figure 5: Mode 2 operation

**iii) Mode 3:** t2 < t < t3 : at the beginning of this mode, DS2 whose voltage was fixed at zero begins to conduct a small current reversely through the switch S2 . This current is the difference between $I_{LS}$ and $I_{L2}$ . Therefore, the voltage across the switch $S_2$ which is the same as $V_{CS2}$ becomes equal to zero as shown in Figure 8. Thus, it is a great opportunity to apply the gate signal of the switch as $V_{GS2}$ during this interval. So, the switch $S_2$ turns ON at the zero voltage. Figure 6 shows the equivalent circuit diagram of this mode.

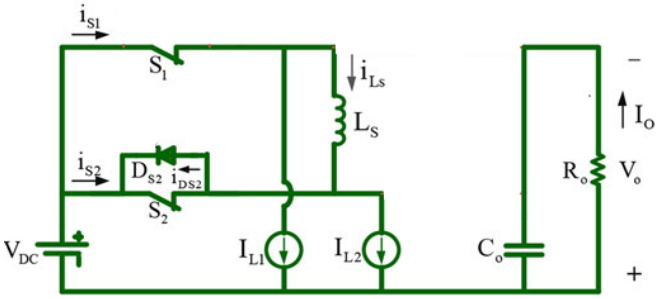


Figure 6: Mode 3 operation

**iv) Mode 4:** $t_3 < t < t_4$ : at the beginning of this mode, the gating signal of the switch $S_1$ is removed and it is turned OFF. Therefore, the intrinsic capacitor $C_{S1}$ is charged rapidly to $V_{DC}$+$V_O$ by the sum of currents $I_{L2}$ and $I_{L1}$. According to Figure 3.7, along with an increase in the $C_{S1}$ voltage, the current $I_{LS}$ begins to decrease and reverses its direction

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towards to $-I_{L1}$ because $V_{CS1}$ is imposed on the inductor $L_S$. By applying the KVL to the end of this mode, the voltage of diode $D_1$ becomes equal to zero. Thus, it begins to freewheel the load current. Due to the symmetry of the converter, modes V to VIII could be summarized in similar scenarios for the switch $S_1$.

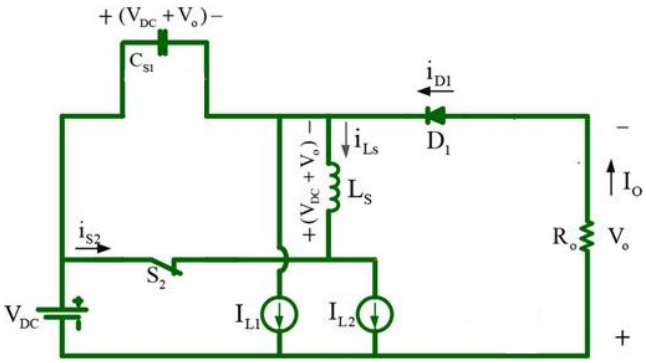


Figure 7: Mode 4 operation

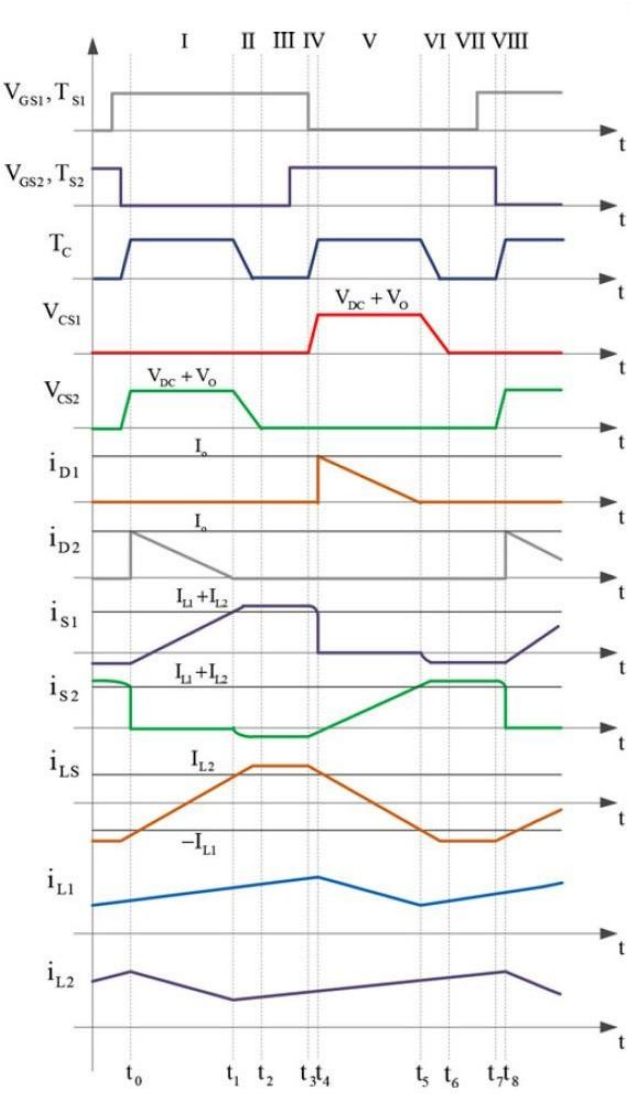


Figure 8: Typical waveforms of key components

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## IV. CIRCUIT ANALYSIS AND DESIGN

For the circuit analysis and design as mentioned above the duty ratio of switches must be considered slightly greater than 0.5. Therefore it causes a small overlap between the gating signals of the switches.

$$D_E = \frac{T_S - T_C}{T_S} \quad (1)$$

Where $T_S$ and $T_C$ are the switching and commutation times, respectively. As shown in Figure 7, in the time interval $T_C$, $I_{LS}$ almost swings between the values of $I_{L1}$ and $I_{L2}$ and vice versa, and because the voltage across the inductor $L_S$ is clamped at $V_{DC} + V_0$ , the commutation time can be represented as follows:

$$T_C = \frac{L_S(I_{L1}+I_{L2})}{V_{DC}+V_0} = \frac{L_S I_{in}}{V_{DC}+V_O} \quad (2)$$

On the other hand, the relations between the output and input values of a usual buck-boost converter in the CCM are stated as follows:

$$V_O = \frac{D_E}{1-D_E} V_{DC} \quad (3)$$

$$I_O = \frac{1-D_E}{D_E} \quad (4)$$

Therefore, inserting Equation 3 and Equation 4 into Equation 2, the commutation time $T_C$ can be represented in terms of the output current, input voltage and inductance $L_S$ as follows:

$$T_C = \frac{D_E L_S}{V_{DC}} I_O \quad (5)$$

Combining Equation 4 with Equation 5, the effective duty ratio of the converter can be obtained as ;

$$D_E = \frac{1}{1+\frac{f_S L_S}{V_{DC}} I_O} \quad (6)$$

The voltage ratio of the converter can be obtained by inserting Equation 6 into Equation 3 in terms of switching frequency, load resistance, and the value of the inductance $L_S$,

$$V_O = \sqrt{\frac{R}{f_s L_s}} V_{DC} \quad (7)$$

Therefore, it can be concluded that the control over the output voltage could be possible by modifying the switching frequency $f_S$, while not changing the duty ratio of the switches like conventional buck-boost converters. Since the effective turn off interval of the converter is just in Modes I and V, and also, it is known that at these intervals the current of the interleaved inductor LS swings between values $-I_{L1}$ and $I_{L2}$ , therefore, considering these intervals to be $(1-D_E)T_S$ , the following equation can be written for the inductor $L_S$

$$\frac{di_{L_s}}{dt} = \frac{I_{L1}-I_{L2}}{(1-D_E)T_E} = \frac{V_{L_s}}{L_S} \quad (8)$$

As it is indicated in Figure 2.7, the voltage across the inductor $L_S$ is equal to $V_{DC} + V_0$ at intervals I or V. Thus, if $I_{L1}$ and $I_{L2}$ are considered equal, the variation of iLs can be assumed $2I_{L1}$. According to Fig. 2.7, neglecting the ripple of inductors L1 and L2 currents, the average value of $i_{L1}$ is equal to half of the summation of the input and output currents. Therefore, equation (8) can be represented as ;

$$\frac{I_{in}+I_O}{(1-D_E)T_S} = \frac{V_{DC}+V_O}{L_S} \quad (9)$$

Simplifying Equation 9 by substituting Equation 3 and Equation 4, results in the value of the inductance LS for a specified input dc voltage as follows:

$$L_S = \frac{(1-D_E)V_{DC}}{f_S I_O} \quad (10)$$

Inductances $L_1$ and $L_2$ are obtained by considering the magnitudes of the $i_{L1}$ and $i_{L2}$ current ripples. The maximum permissible current ripple should not exceed the rated output current, so the converter could operate in the CCM. Thus,

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considering Modes I and V , $i_{L1}$ and $i_{L2}$ are decreased due to voltage $-V_0$ which is clamped at the inductances $L_1$ and $L_2$. Therefore, the value of inductances $L_1$ and $L_2$ should meet the following constraint;

$$L_{1,2} > \frac{D_E V_{DC}}{f_S I_O} \qquad (11)$$

To determine the value of the output capacitor, it is considered that the ripple and the average value of the converter output current flow to the output capacitor $C_0$ and the load, respectively. On the other hand, the current of the diode in the buck-boost

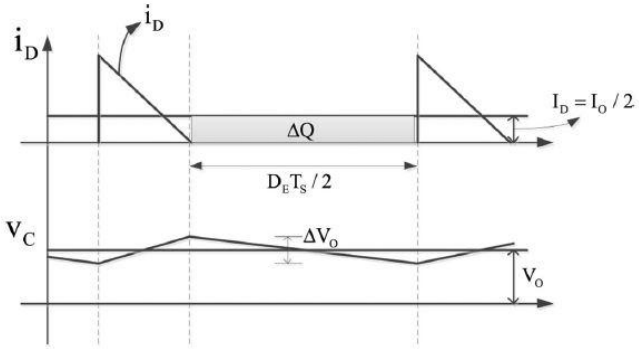


Figure 9: Diode current and output voltage ripple across the output capacitance

Converter can be considered equal to the output current. Therefore, the ripple of the diode current causes the ripple in the output voltage across capacitance $C_0$, as indicated in Figure 8. Because the two conversion units work in parallel, the average current of each diode can be assumed to be half of the average current of the load, as shown in Figure 1. To achieve the amplitude of the output voltage ripple, the charge variation of the capacitor $C_0$ could be easily calculated by computing the surface $\Delta Q$ in half of the effective turn on period $D_E T_S$, as depicted in Figure 8. Thus, the capacitance $C_0$ can be obtained as follows:

$$C_O = \frac{\Delta Q}{\Delta V_O} = \frac{D_E T_S I_O/4}{\Delta V_O} = \frac{D_E}{4 f_S R(\Delta V_O/V_O)} \qquad (12)$$

Where $\Delta V_O/V_O$ is the relative output voltage ripple usually considered to be less than one percentage of the output nominal voltage.

TABLE I describes the simulation parameters for the converter. Simulation of resonant parallel buck-boost converter is carried out using an input of 20 V, switching frequency $f_s$ of 133 kHz and 60 % duty ratio.

Table I: Simulation Parameter

| COMPONENTS | PARAMETER |
|---|---|
| Input DC Voltage | 20V |
| Inductor $L_1$ & $L_2$ | 180µH |
| Inductor $L_s$ | 30µH |
| Capacitor $C_o$ | 100µF |
| Duty Ratio | 55% |
| Switching Frequency | 100-200kHz |

Simulation is performed with a 20 V input DC source and a 25 ohm resistive load. The switching frequency has been considered 133 kHz. Two power MOSFETs $S_1$ and $S_2$, are adopted for high frequency switching with the same switching frequency. The duty ratio D for each of the switches is identical and slightly greater than 0.5 to create overlapping intervals. The inductor LS placed between two parallel converters is called the interleaved inductor. This element plays an important role in main plot of the soft switching manner of the converter. It is assumed that the converters operate in the continuous current mode (CCM).

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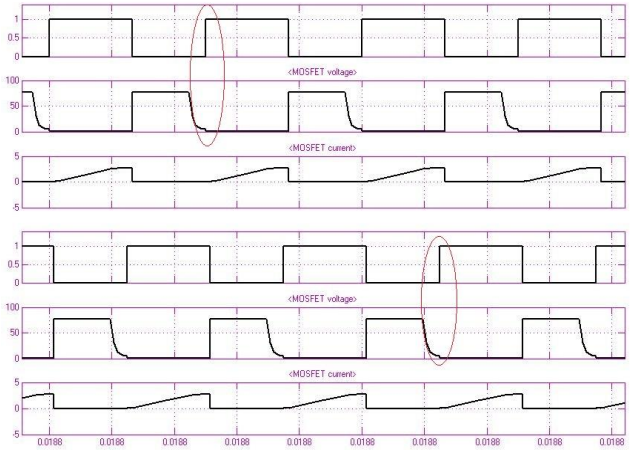


Figure 10: Simulation results of (a) Voltage across switch S1 (b) Gate pulse of switch S1 (c) Current through switch $S_1$ (d) of Voltage across switch S2 (e) Gate pulse of switch S1 (f) Current through switch $S_1$

Figure 10. shows the switching pulse applied to the switches and voltage across the switches. Stress across these switches is 61 V. From the marked portions in the waveforms, it is clear that the switch voltage waveform create a zero-voltage condition for the switch to turn on. Thus zero voltage switching is achieved.

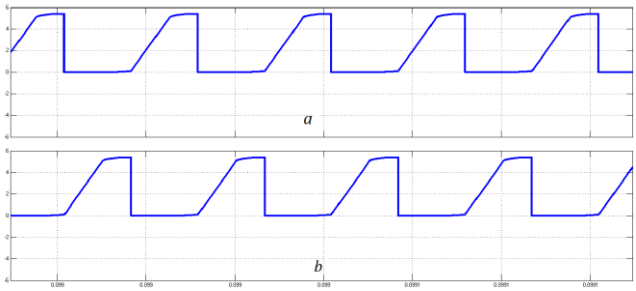


Figure 11: Simulation results of (a) current through switch S1 (b) current through switch S2

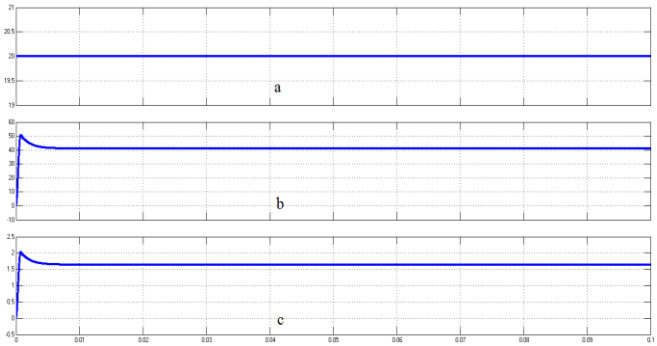


Figure 12: Simulation results of (a)Input voltage (b)Output voltage (c)output current

Figure 12 shows the waveforms of input voltage, output voltage and output current. For an input voltage of 20 V, 133 kHz switching frequency and 0.55 duty ratio the output voltage is obtained is 41 V. That is the output voltage is boosted. The output voltage can be regulate by varying switching frequency instead of duty ratio.

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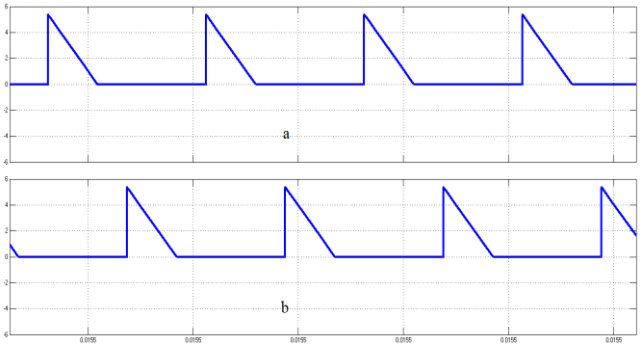


Figure 13: Simulation results of (a)current through diode D1 (b)current through diode D2

Figure 13 shows the current through the inductors and voltage across the switches. The ripple in the inductor currents IL1 and IL2 is 0.29 . Ripple in the capacitor voltage C0 is 0.03

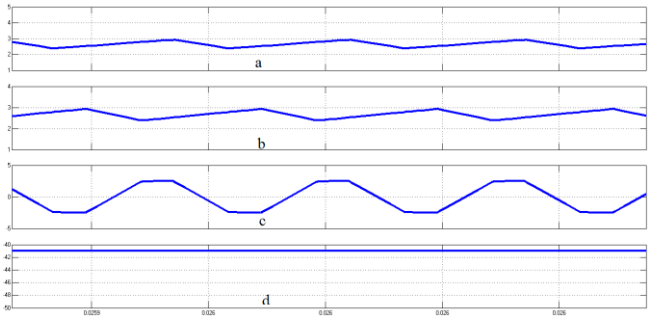


Figure 14: Simulation results of (a) current through inductor L1 (b)current through inductor L2 (c)current through inductor LS (d)voltage across output capacitor C0

Simulation results obtained verified the performance of the converter. For an input voltage of 20 V, 133 kHz switching frequency and 55% duty ratio, the output voltage is boosted and is obtained as 41 V. Ripple in the inductor currents $I_{L1}$ and $I_{L2}$ is 0.29 A and the ripple in the output capacitor voltage is 0.03 V. That is ripple in the inductor currents and ripple in the output capacitor voltage is reduced. The output voltage is regulated by varying the switching frequency instead of duty ratio. Performed analysis to achieve the zero-voltage-switching operation of the converter has been verified and the switches can be turned on at the zero voltage and it means that the switching losses are decreased.

## V. HARDWARE RESULTS

The hardware consists of three parts: a pulse generating circuit a driver circuit and a double deck converter circuit. The input to the converter is fed from a rectifier circuit with 10A current rating and the control of converter is generated using dsPIC30f2010. The voltage is sensed using a potential divider and a opto-coupler. Output compare logic is used in dsPIC to generate gate pulse with varying frequency. The generated gate pulse is given to the driver circuit. Driver circuit consist of two individual TLP250 with isolated power supply. The individual gate pulses from the driver circuit is given to the converter.

Gate pulse algorithm with 55% duty ratio is realized in dsPIC30F2010. Two independent driver circuit is achieved with TLP250. Independent driver output from DSO is shown in figure 15. Input DC supply is made through 10A bridge rectifier circuit. A closed loop Double Deck buck boost converter prototype is tested in PCB circuit with 100W load. Boost operation is obtained with switching frequency of 132kHz, an output of 80V is reached with an input of 20V. The figure 15 shows the gate pulse for independent parallel converters. An overlap of 5% is given in each gate pulses to achieve zero voltage soft switching. A fixed duty ratio of 55% is used to get this overlap. A logic algorithm is used in dsPIC controller to get this gate pulses. And TLP250 driver is used to drive the MOSFET switch.

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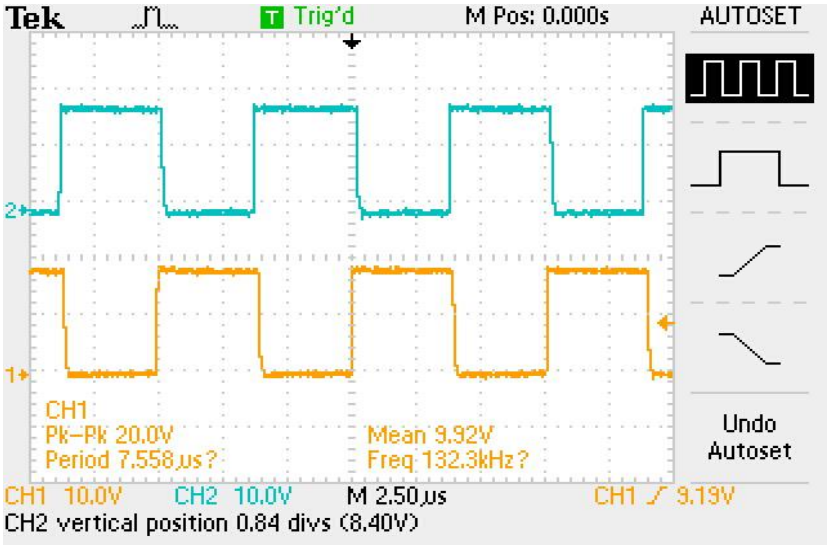


Fig. 15 : Gate pulse from driver circuit TLP250

Table II: Experimental results

| INPUT VOLTAGE | LOAD | OUTPUT VOLTAGE | REGULATION |
|---|---|---|---|
| 20V | 100% | 80V | 0% |
| 15V | 100% | 78.5V | 1.8% |
| 20 | 80% | 81V | 1.25% |
| 20 | 60% | 82V | 2.5% |

Fig. 16: Experimental Setup

The experimental setup is shown figure 16. Separate PCB circuits are used for converter circuit, driver circuit and controller circuit. A load of 20-100Ω resistance is given through a Rheostat of current rating 6A. Input dc voltage is obtained from a rectifier circuit with varying voltage arrangement using auto transformer. A 10A bridge rectifier with 1000µF filter is used as input voltage source. The experimental results are shown in TABLE II.

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## VI. CONCLUSION

A soft switched double deck converter is simulated using MATLAB SIMULINK with voltage feedback and regulation. A hardware prototype is setup and outputs are verified. With an input voltage of 20 V, 133 kHz switching frequency and 55% duty ratio an output of 80V is obtained. The effective duty ratio is varied using changing the frequency of the gate pulses. As the frequency increases the output voltage decreased and vice versa. With a closed feedback circuit, it is made to maintain a constant output voltage. The voltage regulation using the closed loop error correction helps to charge Electric Vehicles and other DC requirements. Soft switching techniques utilizing the features of Zero-Voltage Switching (ZVS) substantially reduce the switching losses. With soft switching operation the efficiency is improved.

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