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Implementation of Kogge Stone Adder for Signal Processing Applications

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Abstract: Low power system design has turn out to be a significant performance goal. The Finite Impulse Response Filter is an efficient component for digital signal processing applications. Adders and multipliers plays an essential role in implementation [R1] of FIR filter. The proposed FIR Filter is designed by using Kogge stone adder and booth multiplier. Kogge stone adder is a high speed adder which is used for designing high performance circuits and Booth multiplier is a multiplication algorithm which is used to perform multiplication by using 2's complement notation. Thus the proposed design can reduce the delay and power consumption of FIR filter. The proposed FIR filters are designed with the help of verilog Hardware Description Language and synthesized using Xilinx ISE 12.4 tool.

Keywords: Booth Multiplier; Digital Signal Processing (DSP); Finite Impulse Response Filter (FIR); Kogge Stone Adder

I. INTRODUCTION

Nowadays digital signal processing has become popular in industry owing to the use of low cost in growth of software and hardware. Filtering plays a major role in digital signal processing applications and also in the field where difficulty is less [Damini Ku Dandade C et al, 2017]. In high bandwidth applications, FPGA or ASIC are used for the operations of filtering. The expectations of most of the people are system with good efficiency, accuracy and error free operation. The process of filtering is performed by using digital filter. The multipliers and adders plays main role in FIR filter design while considering the power. The FIR filter consists of n+1 number of multipliers and n adders. The FIR filter has high efficiency by reducing the number of operations. Digital filter performs three basic functions as multiplications, addition and delay element. The major blocks present in FIR filter are adder and multiplier which gives in reduction of power, delay and area for each operation.

The dissipation in power of the CMOS circuits can be categorized as static power dissipation, short circuit power dissipation and dynamic power dissipation. Thus in CMOS circuits, total power dissipation can be given as

$$P = \alpha f_c C_L V_{dd}^2 + I_{sc} V_{dd} + I_{leakage}\ V_{dd} \qquad (1)$$

In above equation, the first term represent dynamic power dissipation, the second term represent static power dissipation and the third term represent leakage power dissipation. Among this, when compared to other types, dynamic power dissipation is more dominant. Attaining high speed adder and multiplier and also less power consumption are the major goal of this paper. Carry select adder is used for designing FIR filter with low power consumption and lesser delay [Ashwini A.Lokhande, et al, 2015] but the speed is less. Second Bypassing method is used for multiplication operation to minimize the dynamic power dissipation. Low power bypassing based multiplier [Saranya Krishnamoorthy et al, 2017] is an effective and efficient multiplier for reducing the dynamic power consumption but it acquires more delay. Moreover, decreases in power consumption and delay also valuable in increasing the speed. The system performance in digital signal processing is improved by using Kogge stone adder and Booth multiplier. The paper is organized as follows, section II gives the FIR filter theoretical concepts for signal processing applications, section III details with parallel prefix adder, section IV offers Booth multiplier. Section V carry outs the comparative analysis and simulation results of FIR filter, Section VI affords conclusion

II. THEORETICAL CONCEPTS OF FIR FILTER

Linear convolution is performed between filter coefficients and the input signal for designing FIR filter. Let us consider the filter having the input sequence x(n) = [0,1,2,3,……,N-1] of length 'N' and impulse response b(n) = [0,1,2,3,…….M-1] of length 'M'[8].

The output sequence of the FIR filter y(n) is expressed as the convolution between input signal x(n) and filter coefficients b(n). The output expression of FIR filter is specified by

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$$y(n) = x(n) * h(n)$$

$$= \sum_{n=0}^{N-1} b(n)x(k-n) \qquad (2)$$

By elaborating the above equation (2), the output of FIR filter is given by,

Y(n) = b(0)x(n) + b(1)x(n-1) + b(2)x(n-2) + b(3)x(n-3) +……..+b(M-1)x(n-M+1) (3)

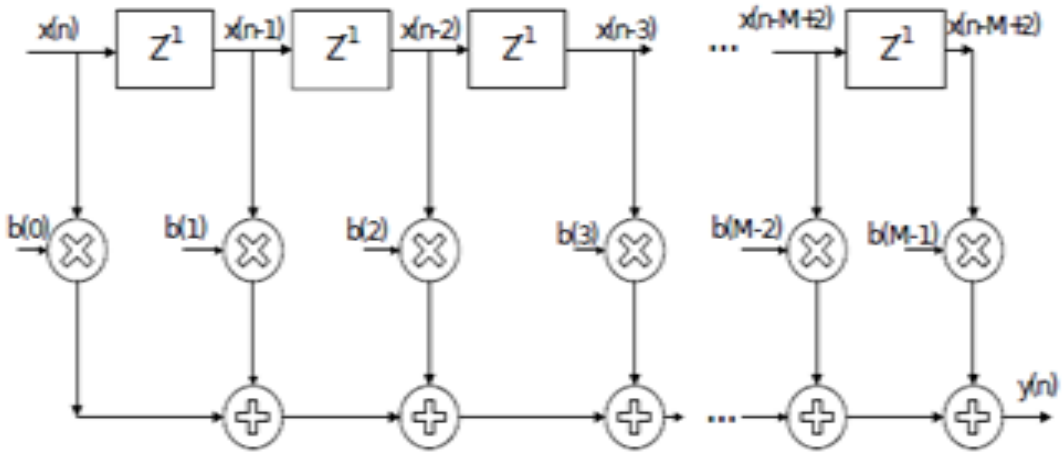

Fig 1: Realization of Direct Form FIR Filter

The expansion of direct form representation is also called as canonic form. The order of difference equation will be decided by the number of delay elements present in the realization of direct form. The realization of FIR filter shown in the Figure 1 consists of M multiplication, M-1 additions and M-1 delay blocks. The below figure represents the realization of direct form FIR filter. Because of input sequence and filter coefficients are finite, the linear convolution between these sequences will also be finite.

III. PARALLEL PREFIX ADDER

Binary addition is the frequently used arithmetic operation [1]. Parallel prefix adders are used when high speed operation is essential in signal processing applications. In this adder, the operations are performed in tree like structures. The diagrammatical representation of parallel prefix adder (PPA) is shown in the figure 2.

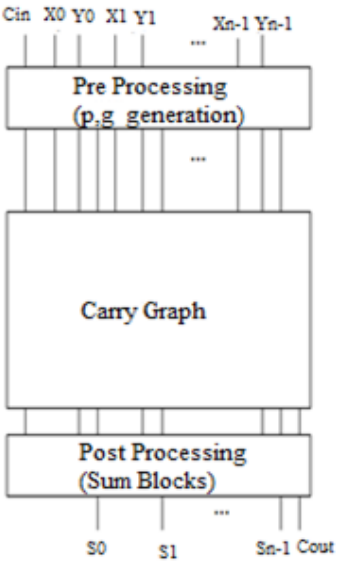

Fig 2: PPA Structured Diagram

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Parallel prefix adder comprises of three main parts explicitly pre-processing for p,g generation, carry graph and post-processing for addition operation. The generate (g) and propagate (p) terms are found in pre-processing step. The realization of PPA carry bit is unique when compared with other type of adders. The high-speed arithmetic addition operations are performed in parallel form using generated carry bits

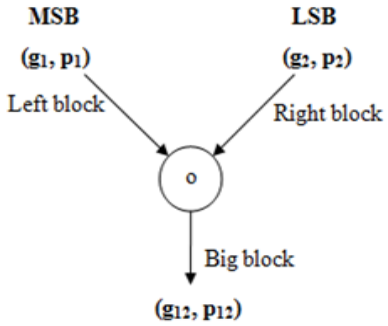

Fig 3: Function of Carry Operator

Figure 3 shows the attainment of the carry bit at an instantaneous time C_{in}. In the above figure, the symbol 'o' represents associative operator and also called as prefix operator.

$$(g_1,p_1)\ o\ (g_2,p_2) = (g_1+g_2.p_1,p_1.p_2) \qquad (4)$$

where g_1,g_2 represents generation bits and p_1,p_2 represents propagation bits.

Based on the equation (4), there are two conditions for generating carry which are;

i. Left block (MSB) has a carry generated **OR**
ii. Right block (LSB) generates a carry **AND** left block propagates it.

If both right and left blocks are propagating the carry, the big block will propagates a carry. The classification of parallel prefix adder are uniquely different from each other based on their carry graph and number levels. The parallel prefix adder are classified as many types. There are Brent Kung adder, Kogge stone adder, Ladner Fisher, Hans Carlson and Knowles. Among these types Kogge stone adder is chosen for designing FIR filter.

A. KOGGE STONE ADDER

The Kogge stone adder (KSA) is called as high speed adder in VLSI [5]. Kogge Stone Adderis one of the types of parallel prefix carry look ahead adder.

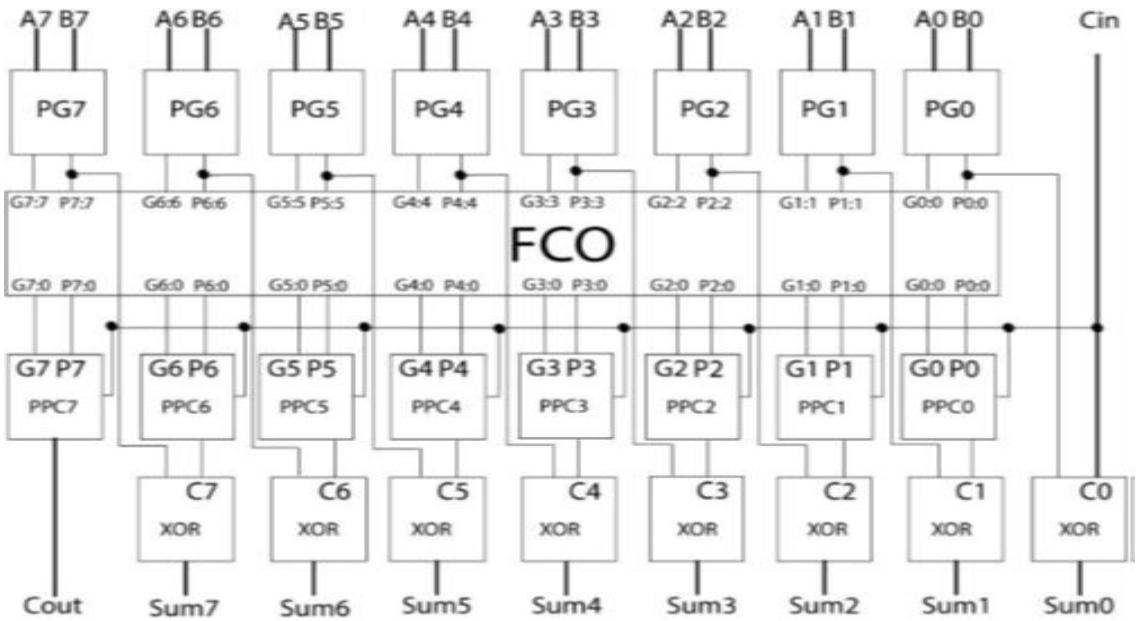

Fig 4: Architecture of 8-bit Kogge Stone Adder

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This adder is considered as fastest adder because it produces carry in O (log n) time and it is broadly used in high performance arithmetic circuits. The architecture of 8-bit Kogge stone adder are shown in figure 4. The architecture of Kogge stone adder is analogous to Carry Look Ahead (CLA) adder. Pre-processing, carry generator and post-processing blocks are the major blocks of Kogge stone adder. The Fundamental Carry Operator (FCO) lies amid of PG and PPC blocks. Thus, this FCO block will generate the propagate (p) and generate (g) bits in pre-processing step. The architecture of FCO is shown in the figure 5.

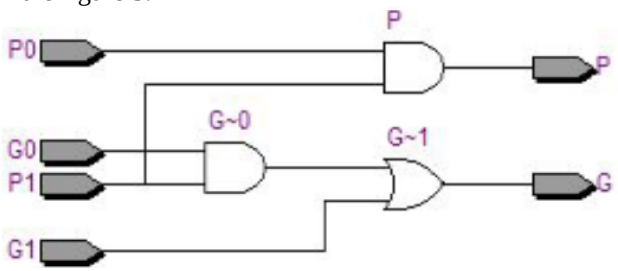

Fig 5: Architecture of FCO

The Kogge stone adder of 1-bit circuit need 2 gate delays which can be used to combine any P_i and G_i signals that are already combined. Each bit of PPC block contain input as C_{in} which is firmed by external factors. The input of next PPC block are assumed as C_{out} from previous block. By using this architecture, we obtained lesser delay and high speed.

B. Booth Multiplier

Booth multiplier is used to perform multiplication operation between two binary numbers in 2's complement notation[4].

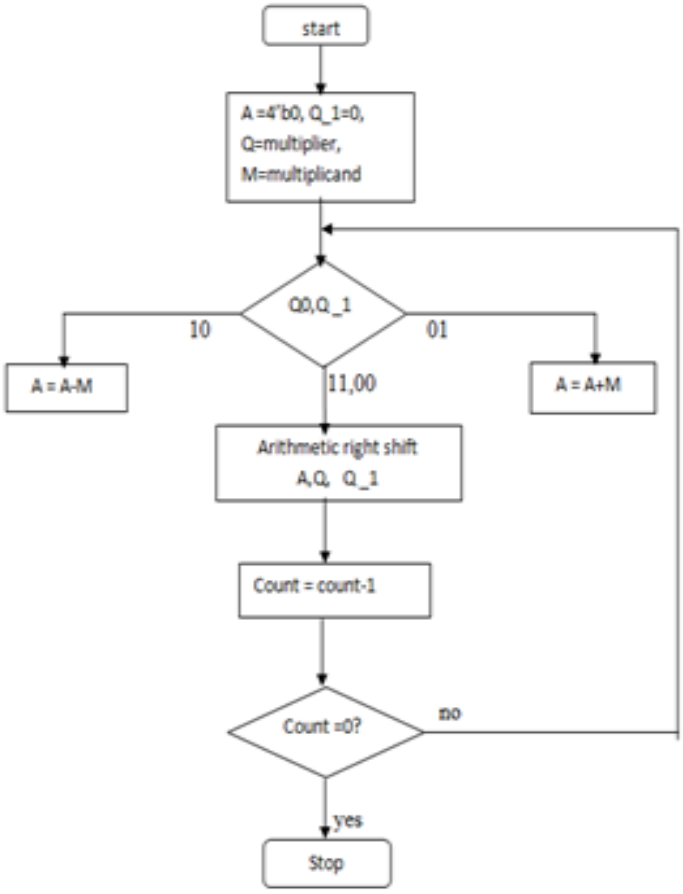

Fig 6: Flow chart of Booth Algorithm

The proposed FIR filter is based on radix-4 modified booth encoding algorithm which provides lesser delay andlow power consumption. Booth multipliers performs shift and add operation. The flowchart of Booth algorithm is shown in the figure 6.Booth multiplication is performed in three steps. The first step is partial product generation using booth

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encoder, second one will be the partial product accumulation using compressor and at last final product generation using fast adder. The main advantages ofbooth multiplier are reducing the number of partialproducts generated and hence only less number of addersare used to design the FIR filters. Booth multipliers are evaluated with respect to both error analysis and hardware implementation. It can also used in image processing.

IV. RESULTS AND DISCUSSION

The proposed FIR filter using Kogge stone adder and Booth multiplier are simulated and synthesized using Xilinx ISE tool via verilog hardware description language. The FIR filter consists of three blocks namely adder, delay element and multiplier. The figure 7 shows the simulation result of FIR filter.

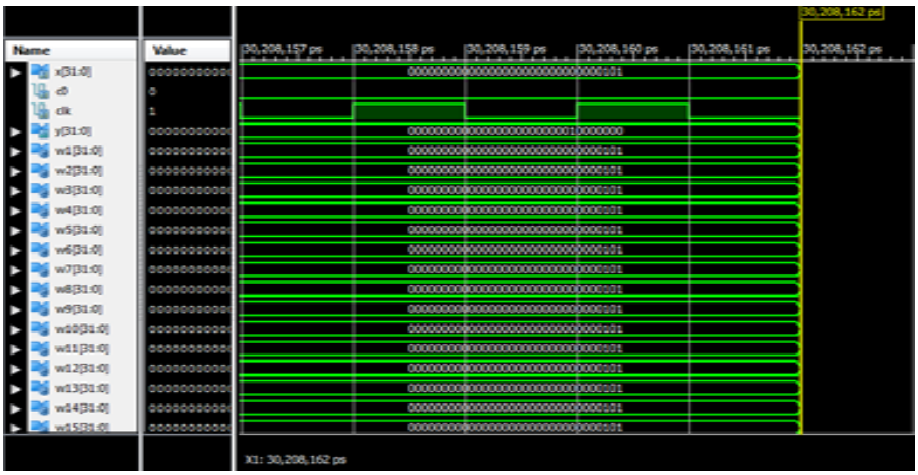

Fig 7: Simulation result of FIR filter

The comparison result of proposed FIR filter with existing FIR filter is shown in the below table.

Table 1: Comparison of Fir Filter

Parameters	FIR filter using CSLA	FIR filter using Kogge stone adder
Power (mW)	0.76	0.72
Delay (ns)	189.324	156.798

From this analysis, we illustrated that FIR filter using Kogge stone adder acquired lesser delay and low power consumption.

VI. CONCLUSION

In this paper, Kogge stone adder and Booth multiplier are used to implement Finite Impulse Response (FIR) filter. Due to parallel addition process of Kogge stone adder, it achieves high speed. According to the analysis, the existing FIR filter consumes more power and delay will be high when compared with proposed FIR filter. The proposed FIR filter is simulated and analysed using Xilinx ISE tool.

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BIOGRAPHIES

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