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A Survey on Ultra Wide Band and Narrow Band Low Noise Amplifiers for Wireless Transceivers

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Abstract: This paper presents the survey of the design of Low Noise Amplifier (LNA) for different wireless applications. This paper focuses diverse design techniques and new architectures in the design and implementation of low noise amplifier such as self-biased, forward bias, common source cascade, Cascode, body bias and LNA based on dual resonance techniques. These design methodologies are serving to reduce the power consumption and enhance the performance such as gain and noise factor in wireless applications. In this paper, recent design methodologies of different LNA is meticulously analyzed and new design method will be proposed to enhance the performance of the LNA.

Keywords: Cascade, Cascode, CMOS, LNA, Low Power And Low Noise

I. INTRODUCTION

In recent days, the wireless applications such as 4G and 5G have become major part in our day to day life and industrial applications (Gayathri R et al., 2017). Hence, the role of LNA is essential to get better performance in 4G and 5G applications. Digital receivers are playing a vital role in RF communication fields like mobile communication, wireless sensor networks and Zig-bee etc (Muruganantham T et al., 2017). To design an efficient receiver the design of mixer, low noise amplifier and digital filters are important. Here the low noise amplifiers are playing an important role in receiving the RF signal from the antennas with reduction of noise. The performance of the LNA decides the performance of the receiver. Hence, the design of efficient LNA is very much needed.

II. LOW NOISE AMPLIFEIR

As the high requirements of RF receiver the Low noise amplifier performance also being increases with different parameters. As the important and first part of the receiver is low noise amplifier the basic needs have to be satisfied are low power consumption, less occupied area if CMOS transistors are involving, low noise figure and High gain. Based on the designs and specifications of an low noise amplifier it will be suitable for Ultra wide band (3.1 to 10.6Ghz) and Narrow band applications. The basic specification of wireless applications such as reliability, accuracy, flexibility and high performance rate are achieved through the basic requirements of low noise amplifier. The recent works of Low noise amplifiers are discussed in the following topics.

III. DESIGN METHODOLOGIES

1. Foeward body bias



Fig.1 The Forward body bias technique of LNA(Wu.J, et al., 2012)

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The forward bias LNA is implemented to reduce the power consumption. In this technique the Low noise amplifier (Wu.J, et al., 2012) is designed by 0.18micro meter cmos technology and it's operating frequency is 2.4GHz with supply voltage of 0.6v and noise figure of 2.88dB ,gain is 10.1dB and it consumed power0.84mW. The forward body bias method is shown in Fig 1.

I. The Forward Body Bias Topology.



Fig.2. The Nmos threshold voltage when VBS 0 from 0.5V (Wu.J, et al., 2012)

The treshold value of NMOS transistor is given by

$$Vth = Vth0 + \gamma(\sqrt{2\emptyset f - Vbs} - \sqrt{2\emptyset f})$$
(1)

From Fig.2, it can be observed when the VBS increasing to 0.5V, VTH decreases to 0.291V from 0.475V. Low noise amplifier is achieved without affecting other device gain, linearity and NF with low power (Wu.J, et al., 2012, Taeyoung Chung, e al., 2015). The LNA circuit consists of very a very small amount of leakage current in body source junction of NMOS transistor.

2. Common source cascade design

The impedance matching and less noise figure is achieved and makes it suitable for low noise amplifier design with common source cascade methodology. The low noise amplifier is shown in Fig2.common cascade amplifier with passive inductor and the source follower (Kia. H.B, et al., 2012). The impedance of an output of the source follower for the circuit is by 1/gm and it is equal to 50Ω . The gain of the LNA design is less than 0 dB and schematic diagram is shown in Fig3.



Fig. \Box LNA topology with common source cascade (\Box ia \Box \Box \Box \Box , et al., 2012)

The schematic has been designed with 0.18micro meter cmos technology which helps to improve the low power operation and less occupied area.



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3. Cascode design

The general and common architecture is being used to design the Low noise amplifier is Cascode.Main advantages of Cascode design is to avoid the Miller effect impedance matching problems and providing good isolation (Becky Mary Ninan1, et al., 2017). The circuit design of Cascode is shown in Fig4.



Fig.4.The cascode structure (Tang. X, et al.,2012)

This topology is widely used in transceiver systems because of the low noise figure and improved gain



Fig.5 The source inductance negative feedback with cascode LNA(Tang. X, et al., 2012).

The schematic diagram of the source inductance negative feedback with cascode LNA is shown in Fig.5.By varying bias voltage the output matching is obtained. The gain, Noise figure and impedance matching of LNA is achieved through the source inductance negative feedback with cascade design. Design with 0.13micrometer CMOS technology results low noise figure and power consumption is 5.8mW

4 .CMOS based LNA with gain variability through body biasing

This implemented CMOS based LNA schematic uses a Nmos and Pmos transistors and the same bias current is shared because of reduced supply voltage and Vth is reduced. The transconductance of this topology becomes the sum of the transconductance of individual transistors which is mentioned in (Taris. T, et al., 2006). This will help to improve the gain.

$$g_{m=}g_{mn} + g_{mp}$$

In the Fig, M1 and M2 transistors are complementary MOS structure and M3 is the Transistor used for biasing. The load inductance is formed with the help of L3 & L4 connected to the drain terminal of all transistors separated by a capacitor C2. The capacitor C2 Providing the isolation between the transistors. The LNA design is shown in Fig.6

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Due to the variation in Vsb to 0.4v from -0.4v, the Vt is represented in the graph as available in Fig7.From Fig 6, Vt is changed to 0.6v from 0.05v for a Δ Vsb= 0.6v(Becky Mary Ninan1, et al., 2017)



5. Ultra -wideband common Gate LNA using body bias technique

The common gate (CG)cascaded low noise amplifier at 2-10 GHz for UWB application with body biased technique is proposed. This proposed 180 nm CMOS based Two-stage LNA is designed. The impedance of an input is matched to impedance of an antenna that is 50Ω .For 2-stage configuration it is needed that the increased voltage requirements because of stacking of transistors. The reduced supply voltage is achieved through the body bias technique which helps for reduction in power utilization with reduced noise figure. The 1st and 2nd stages are enhancing the gain of LNA and good isolation. The implemented Low noise amplifier gives the input return loss of less than -13dB, noise figure of 3.7-6.2 dB and gain of 12.2 dB for 3 GHz (Syed Mubashir, et al., 2017) over the full frequency band. The design power consumption is about 48 mW for a 1.8 V supply. The schematic design is shown in Fig.8

The simulated S parameter is available in Fig 9 and the simulated result of Frequency versus Noise Figure is shown in Fig 10. The input return loss is below -10dB. The stability of the proposed LNA also can be evaluated.

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For the wideband input matching the CG transistors M1 and M2 with C1 and L1 are used. The inter-stage matching network is established because of the combination of L2, L3 and C2. The M3 and M4 in the cascode design provides the better isolation and gain. The transistor M5 gives the output impedance of 50 Ω .





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6. CMOS based UWB LNA by Dual-Resonance

A high gain and low power ultra wideband LNA with low noise figure 130nm technology is presented. The commongate topology is connected with Dual resonance network for input matching and noise figure. The Combination of inductive-series peaking technique and the frequency response of CG-common source cascade topology is implemented. The LNA gives the high power gain of 12 to 15dB with 13 dB input return loss and 3.9 to 4.7 dB noise figure for frequencies from 3 GHz to 12 GHz (Nan Li, et al., 2017). The occupied area of LNA is 1.09 0.8 mm2 and consumed 8.5mW with 1.2V. The proposed diagram is shown in Fig.11



Fig11 Schematic of CMOS UWB LNA (Nan Li,et al., 2017)



Fig.12 Simulated parameters of Frequency versus Noise figure



Fig.13 Simulated parameter of Frequency Versus S parameter

The measured result shows that the proposed LNA technique is suitable for wireless UWB applications.



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7. Low power and High gain UWB low noise amplifier with forward bias technique

The first stage yields an high gain due to high trans conductance of the input side. The wideband machine of an input and low noise figure (NF) with the aid of source degenerated inductors. The 90nm CMOS technology is used in this proposed design and achieves $S_{21} \ge 20$ dB in the UWB frequency range and consuming 12.6 mW power for a 0.6 V supply. The simulation results shows the minimum NF below 1.7 dB in the frequency range of 3.1–10.6 GHz and input return loss $S_{11} < -10$ dB in the frequency range of 3.5–10 GHz. The schematic of proposed LNA is shown in Fig.14



a) S-Parameter resultsc) NF versus Frequency

b) S11 against Frequencyd) P1 dB versus GCP

The schematic is simulated using a 90 nm CMOS technology with $V_{dd} = 0.6$ V and consumed power of 12.6 mW the result of simulation includes the gain and return loss with different V_{bs} . The simulated result is shown in Fig.15.a,b,c and d. It is clearly indicates if V_{bs} is increasing, the gain is also increasing. The main reason for this increasing gain is high transconductances (Sunil Pandey, et al., 2015) of the transistors $M_1 \& M_2$. If the V_{bs1} increases, then theg_{m1} and



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 g_{mb1} are increases. However, the increment of g_{m1} is greater than g_{mb1} , this is the main reason for gain improvement of this LNA. The 0.4v is choose as the body bias voltage and to get minimum value of V_{th} as 0.2 V.

8. Automatic gain controllable LNA for FM receiver

The automatic controlling gain of an LNA(AGC-LNA) for wireless applications is proposed and the LNA adopting the reused dual boosting technique saving the power and a simple type of GC loop is providing the higher resolution gain control. The measurements show power regulation range Implemented in a 65 nm CMOS technology with 40 dB, 12 to 30 dB of variable gain over the different frequency ranges with reduced NF of less than 2.9 dB. The schematic of proposed LNA (Chang-Jin Jeong, et al., 2015) is shown in Fig.16





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The simulated results shown in Fig16.a,b and c for different frequency ranges with gain and noise figure.

9. A wideband CMOS noise canceling LNA with High linearity

This paper presents a wideband noise-canceling LNA focusing on canceling inter modulation of the fundamental componentIMD2 and IMD3.By using a complementary CMOS parallel push-pull structure, the IMD2 is cancelled. The modified noise canceling circuit properly suppresses the IMD3 (Taeyoung Chung, et al., 2015. The 65 nm technology is used to implement the proposed LNA with a 13dB gain and the range of NF from2.1 to 3.5 dB the frequency ranges from 0.1 to 1.6Ghz.The consumed power is 20.8mW at 1.2v and the area is 0.0142mm².The schematic diagram for the LNA is shown in Fig.17





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10. Linearization of LNA for WSN

This proposed LNA is used in RF receiver system for wireless sensor networks. The proposed LNA adopt post distortion technique and achieves less NF 2.14dB and 16.6dB gain. The LNA consumes 11.6mW for 1.8v supplied voltage. The proposed LNA is implemented in 180nm Cmos technology. The proposed LNA is shown in Fig18.



Fig.18 The schematic of LNA

Where the Lg, Ls and Ld are the on chip spiral inductors. The gate inductor Lg is used for tuning & Ls is used for input matching and Ld is offering the output resonance with output capacitance which helps to achieve high gain. The Lc is used for inter stage matching. The linearity can be achieved with the capacitor (Cs) between G and S. The current mirror is formed byM3 and accompanied by transistor M1 which helps to reduce the utilization power of the circuit. (Radha Jisha. S, et al., 2017)





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The Fig.19 and Fig.20 shows the performance of the proposed LNA with frequency versus Gain and noise figure.

11) Improved Design of RF BJT Low Noise Amplifier for 5 to 6 GHz Frequency Range

This paper presents the design of Low noise Amplifier (LNA) using Bipolar junction transistor for the frequency range from 5 to 6 GHz. The LNA uses the shunt series RLC feedback architecture. The stability is increased with the help of stability network. The input return loss, output return loss and gain are analyzed in this paper. The gain and noise figure at 5.3GHz frequency achieved is 30% and 31% improvement compared to the existing design (Vimal.S, et al., 2015). The schematic of the BJT based LNA is shown in Fig.21





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The stability is increased because of RLC feedback network (Vimal.S, et al., 2015) shown in Fig.22



Fig.22 RLC feedback network

In this approach the noise figure achieved is 1.159dB and the stability is achieved 0.8 with the gain of 13.56dB.This proposed LNA can be used for Wide band applications.

12) Design and performance analysis of LNA with filters for WBAN based health monitoring system

This paper presents the LNA with filters is used for wireless health monitoring systems. The receiver should have the efficient LNA to receive the bio-medical signal to be analyzed for monitor the patient. This paper proposes LNA with band pass, butter worth and chebychev filters. The proposed LNA is simulated using ADS tool. The different parameters like Gain, return loss and Noise Figure are analysed and the performance of the LNA with different filters has been analyzed and it gives the solution that LNA with band pass filter provides good performance compared to LNA with butter worth and chebychev filters (Maheswari.M, et al., 2017). The performance of LNA with different Filters is mentioned in table 1.

| Table1.comparison | of different filter | performances |
|-------------------|---------------------|--------------|
| | | |

| PARAMETERS | LNA-BANDPASS FILTER | LNA- BUTTERWORTH FILTER | LNA-CHEBYSHE FILTER |
|------------|------------------------|----------------------------|------------------------|
| GAIN | 13.042 | 10.346 | 3.192 |
| NOISE | 1.526 | 1.821 | 1.095 |
| STABILITY | 1.095 | 0.996 | 1.526 |

The schematic structure of the LNA with filters is simulated in ADS tool. The simulation results are measured at 5.6Ghz.The input reflection coefficient is -16.566dB, the reverse transmission coefficient is -21.391dB,the forward transmission coefficient is 10.346dB,the output reflection coefficient is-3.409dB, and the stability is 0.996with the NF is 1.821dB (Maheswari.M, et al., 2017)

IV. SUMMARY

The Table 2 shows the performances comparison of recent and different LNAs. The self -biased inverter LNA is achieving less power consumption.

The design of forward bias and self biased inverter techniques can be operated under less voltage leads to low power consumption. When the inductive degeneration cascode design is used will gives better performance in NF and enhancing gain with less power. However the different techniques of LNAs reported can be utilized for different application with satisfying the specific parameters. Performance comparison of Proposed LNAs

| Parameter | CMOS Process (µm) | Supply voltage (V) | Frequency (GHz) | NF (dB) | Gain (dB) | power(mw) |
|-----------|----------------------|-----------------------|--------------------|------------|--------------|-----------|
| 1 | 0.18 | 0.6 | 2.4 | 2.88 | 10.1 | 0.8 |
| 2 | 0.13 | 1.8 | 0.9,1.5,1.9,2.4 | 1.7-3.6 | 17-20 | 20 |
| 3 | 0.13 | 1.2 | 6 | 1.8 | 22.8 | 5.8 |
| 4 | 0.09 | 1.1 | 60 | 2.14 | 8.05 | 2.6 |
| 5 | 0.18 | 1.8 | 2 to 10 | 3.7-6.2 | 12.2 | 48 |
| 6 | 0.18 | 1.2 | 3 to 12 | 4.3 | 13.5 | 8.5 |
| 7 | 0.09 | 0.6 | 3.1 to 10.6 | 1.7 | 20 | 13 |
| 8 | 0.065 | 1.2 | 0.088 to 0.108 | 2.9 | Upto 30 | 23 |
| 9 | 0.065 | 1.2 | 0.1 to 1.6 | 2.1 to 3.5 | 13 | 21 |
| 10 | 0.18 | 1.8 | 2.4 | 2.14 | 16.6 | 12 |

Table 2 Performance comparison of LNAs



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V. CONCLUSION

The LNA implementation using cmos technology is the one of the great challenge which is due to optimize the different targets with requirements such as good gain ,low noise with enhancing the sensitivity of the receiver and increasing better performance with low power consumption & occupied small area to reduce the cost. Therefore, the multiple methodologies are to be considered while implementing a low noise amplifier & with the help of the reviews any of the basic design is to be adopted for different applications.

REFERENCES

- [1]. Ayers. J, Mayaram. K, and Fiez. T, "Tradeoffs in the design of CMOS receivers for low power wireless sensor networks," in IEEE International Symposium on Circuits and Systems, (2007), pp. 1345-1348.
- [2]. Becky Mary Ninan1, Karthigha Balamurugan2, Amrita Vishwa Vidyapeetham, "Design of CMOS based Low Noise Amplifier at 60 GHz and it's Gain Variability through Body Biasing"2017 International Conference on Computer Communication and Informatics (ICCCI -2017), Jan. 05 – 07, 2017, Coimbatore, INDIA
- [3]. Chang-Jin Jeong, Yang Sun, Seok-Kyun Han, and Sang-Gug Lee, "A 2.2 mW, 40 dB Automatic Gain Controllable Low Noise Amplifier for FM Receiver" IEEE transactions on circuits and systems—I: regular papers, vol. 62, no. 2, february (2015)
- [4]. Dr.Maheswari.M, Gayathri.R and Vimal.S "Design and performance analysis of Low Noise Amplifier With Filters For WBAN Based Health Monitoring System" Pak. J. Biotechnol. Vol. 14 (1) 49-54 (2017)
- [5]. Kia. H. B, A'ain. A. K, Grout. I, and Kamisian. I, "A Reconfigurable Low-Noise Amplifier Using a Tunable Active Inductor for Multistandard Receivers," Circuits, Syst. Signal Process., vol. 32, no. 3, pp. 979–992, Oct. (2012).
- [6]. Nan Li, Weiwei Feng, and Xiuping Li, "A CMOS 3–12-GHz Ultrawideband Low Noise Amplifier by Dual-Resonance Network" IEEE Microwave and wireless components letters, vol. 27, no. 4, april (2017)
- [7]. Radha Jisha. S and Mathew "Linearization Of Low Noise Amplifier For Wireless Sensor Networks" International Conference on Inventive Systems and Control (ICISC-2017).
- [8]. Song. T, Oh. H, Hong. S, and Yoon.E, "A 2.4-GHz Sub-mW CMOS Receiver Front-End for Wireless Sensor Network," Microwave and Wireless Components Lett., vol. 16 (1), pp. 206–208, (2006).
- [9]. Sunil Pandey, Jawar Singh, "A 0.6 V, low-power and high-gain ultra wideband low-noise amplifier with forward body-bias technique for low-voltage operations" IET Microw. Antennas Propag., (2015), Vol. 9, Iss. 8, pp. 728–734.
- [10]. Syed Mubashir, Vikram Singh, "A 2-10 GHz Ultra-Wideband Common-Gate Low Noise Amplifier using Body Bias Technique in0.18 μm CMOS"(2017) Devices for Integrated Circuit (DevIC), 23-24 March, 2017, Kalyani, India
- [11]. Taris. T, Begueret. J, and Deval.Y, "A 60µw LNA for 2.4 GHz wireless sensors network applications," in IE EE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006.
- [12]. Tang. X, Huang. F, and Zhao.D, "Design of a 6GHz high-gain lownoise amplifier," in 2012 International Conference on Microwave and Millimeter Wave Technology(ICMMT), (2012), no.2, pp. 1–4.
- [13]. Taeyoung Chung, Hankyu LeeDaechul Jeong, Jehyung Yoonand Bumman Kim, "A Wideband CMOS Noise-Canceling Low-NoiseAmplifier With High Linearity" IEEE microwave and wireless components letters, vol. 25, no. 8, august (2015)
- [14]. Vimal.S, Dr.Maheshwari. M, Improved Design of RF BJT Low Noise Amplifier for 5 to 6 GHz Frequency Range.International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.20 (2015) © Research India Publications
- [15]. Wu J, Y. Lin, and Y. Tsai, "A Sub-mW CMOS LNA for WSN Applications," in Asia-Pacific, Mic rowave Conference Proceedings (APMC), (2012), pp. 899–901.
- [16]. Zhao. B & Yang. H, "Design of radio-frequency transceivers for wireless sensor networks," Wirel. Sens. Networks Appl., vol.40, no. 1, pp. 4–7, (2012).
- [17]. Gayathri R, Maheswari M, Design And Fabrication Of Dual Band RFID Antenna Using Hybrid Coupler With CSRR, Pakistan Journal of Bio Technology, Vol.14 (1), pp. 87-89, (2017).
- [18]. Muruganantham T, Surendar U, Balakumar A, Dual Band Bandpass Filter With Sharp Passband Resonances Using Dual-Mode SIRs, International journal of microwave applications, volume 6, no.2, (March-April 2017).