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A Novel Architecture for Multiplier and Accumulator unit by using Parallel Prefix Adders

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Abstract: MAC unit is mostly demanded in the DSP application. It performs the both addition and multiplication. Here the MAC unit is designed by using the parallel prefix adders like kogge-Stone adder, Brent-Kung adder, Han-Carlson adder and Ladner Fischer adder these adders are the high-speed adders to improve the speed of MAC unit and multiplication purpose. In this design, these four adders are implemented to the array multiplier and to design the MAC unit. The performance and analysis of MAC unit is done by the Verilog HDL and the MAC unit is simulated and synthesized in Xilinx ISE 14.7 for Spartan-6 family technology. The simulation results show that low power, high speed and low area consumption MAC unit.

Keywords: MAC, HDL, Fast Adders, DSP

I. INTRODUCTION

In recent years, Multiply-Accumulate (MAC) unit is developing for various high-performance applications. MAC unit is a fundamental block in the computing devices, especially Digital Signal Processor (DSP). MAC unit performs multiplication and accumulation process. Basic MAC unit consists of multiplier, adder, and accumulator. MAC unit model is designed by incorporating the various multipliers such as Array Multiplier, Ripple Carry Array Multiplier with Row Bypassing Technique, Wallace Tree Multiplier and DADDA Multiplier in the multiplier module and the performance of MAC unit models is analyzed in terms of area, delay and power.

II. DESIGN OF MAC UNIT

In Digital Communication, Digital Signal Processor (DSP) is an important block which performs several digital signal processing applications such as Convolution, Discrete Cosine Transform (DCT), Fourier Transform, and so on. Every digital signal processor contains MAC unit. The MAC unit performs multiplication and accumulation processes repeatedly in order to perform continuous and complex operations in digital signal processing. MAC unit also contains clock and reset in order to control its operation. Many researchers have been focusing on the design of advance MAC unit architectures.

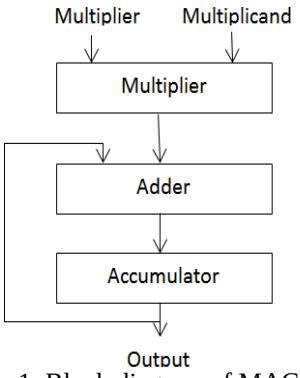

Figure 1: Block diagram of MAC unit

III. DESIGN OF ADDER ARCHITECTURE

Different adders that can be used for the design of a MAC unit are ripple carry adder, carry save adder and carry look ahead adder. Ripple adder is a regulararrangementofsinglebitadderswhichisbeingusedtraditionally.Inthe design the carry- output of one stage is connected to the carry-input of the next stage. Propagation of the carry generated by the fulladder circuits is avoided using the carrysave adder logic. The circuits ends the intermediate carries towards the outputs. Like ripplecarry adder it does not propagate the carry to the next stage.

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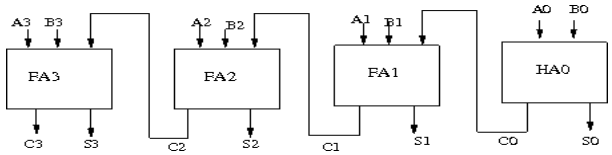

Figure 2: Ripple Carry Adder

The carries thus generated are propagated at the end when all the intermediate carries have been generated. Consequently, two outputs are obtained one is the sum (S) and another bit vector as carry (C). Therefore, total delay imposed by the circuit is equivalent to the delay as that posed by a single full adder circuit. However, it occupies more area in comparison to the ripple carry adder i.e. n times as that occupied by the full addercell.

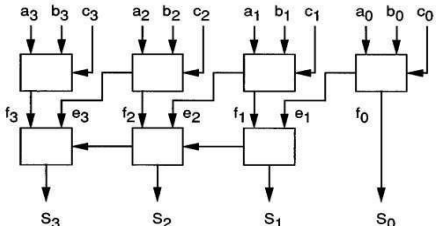

Figure 3: Carry Save Adder

The carry-look ahead adder follows an entirely different logic for addition by computing group generate signals and group propagate signals. It does not wait for the carry of the previous stage as in case of ripplecarry order which helps in optimizing the speed of the circuit. As the carry generated in a circuits stage does not depends on the operands at that instant but at stagei+1 it is marked by the generation of carry in the previous stage i. Hence it leads to the conclusion that a separate network for carry propagation can be implemented thus reducing the delay to wait for the carry generated at various stages. The carry-look ahead adder follows a two-level logic circuit in which, AND gates are followed by an OR gate. For each carry input c_i on loading of adder inputs in parallel, all generator group terms g_i and propagation group terms p_i are created simultaneously. Hence for the carry for each bit is computed independently in the circuit. In actual, the carry signal c_i is obtained through two-stage logic simultaneously, which results in a constant time complexity in the circuit.

IV. DESIGN OF MULTIPLIER

An existing array multiplier is very much regular in its structure when compared to the conventional array multiplier and uses an only short wire that goes from one full adder cell to adjacent full adder cell. It has very simple and efficient layoutinVLSIandcanbeeasilyandefficientlypipelined.Theconventionalarray multiplier is synthesized using 16T full adder cell. The existing full adder cell is made of 16T which is designed using XNOR gate, pass transistor and transmission gate. The 16T full adder cell consumes less power when compared to the conventional CMOS full adder cell that uses 28 transistors. This cell produces full swing at the output nodes. This low power full adder cell has a drawback of giving large delay when compared to other adders.

V. RESULTS AND DISCUSSIONS

The result of the design made are discussed with the comparison of various adders to design multiplier and accumulator units. Table 1 shows the synthesis report of 64 bit adder of different architecture which could be used for the design.

Table 1: Synthesis report of 64-bit adders

Parameters	Ripple	Carry Save	Carry Look Ahead
No. Of Slices	74	220	96
Bonded I/O	194	322	193
Level of Logic	66	67	65
Combination al Delay(ns)	42.84	40.383	55.662
Logic Delay (%)	31.6	33.6	39.1
Route Delay (%)	68.4	66.4	69.1
Total Power(W)	0.374	0.236	0.375
Destination Port	65	66	65
Total No. Of Paths	4353	29817	4288

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Table 2: Synthesis result of 64-bit MAC units with different adders

Parameters	Ripple	Carry Save	Carry Look ahead
No. Of Slices	5318	5349	5318
Bonded I/O	257	257	257
Level of Logic	2735	2687	2735
Combinational Delay(ns)	1532.50	1530.435	1532.50
Logic Delay (%)	26.1	56.7	25.5
Route Delay (%)	73.9	43.3	74.5
Total Power(W)	0.252	0.168	0.249
Destination Port	128	128	128

Table 3: shows the synthesis results of different 64-bit adder units.

Parameters	Kogge-Stone Adder	Brent-Kung Adder	Ladner Fischer Adder	Han- Carlson Adder
No. Of Slices	49	17	23	23
Bonded I/O	50	47	49	49
Level of Logic	10	3	6	6
Combinational Delay(ns)	11.891	5.422	8.397	8.397
Logic Delay (%)	45.7	76.7	54.8	54.8
Route Delay (%)	54.3	26.3	45.2	45.2
Total Power(W)	0.374	0.236	0.375	0.375
Destination Port	19	17	17	17
Total No. Of Paths	397	36	160	160

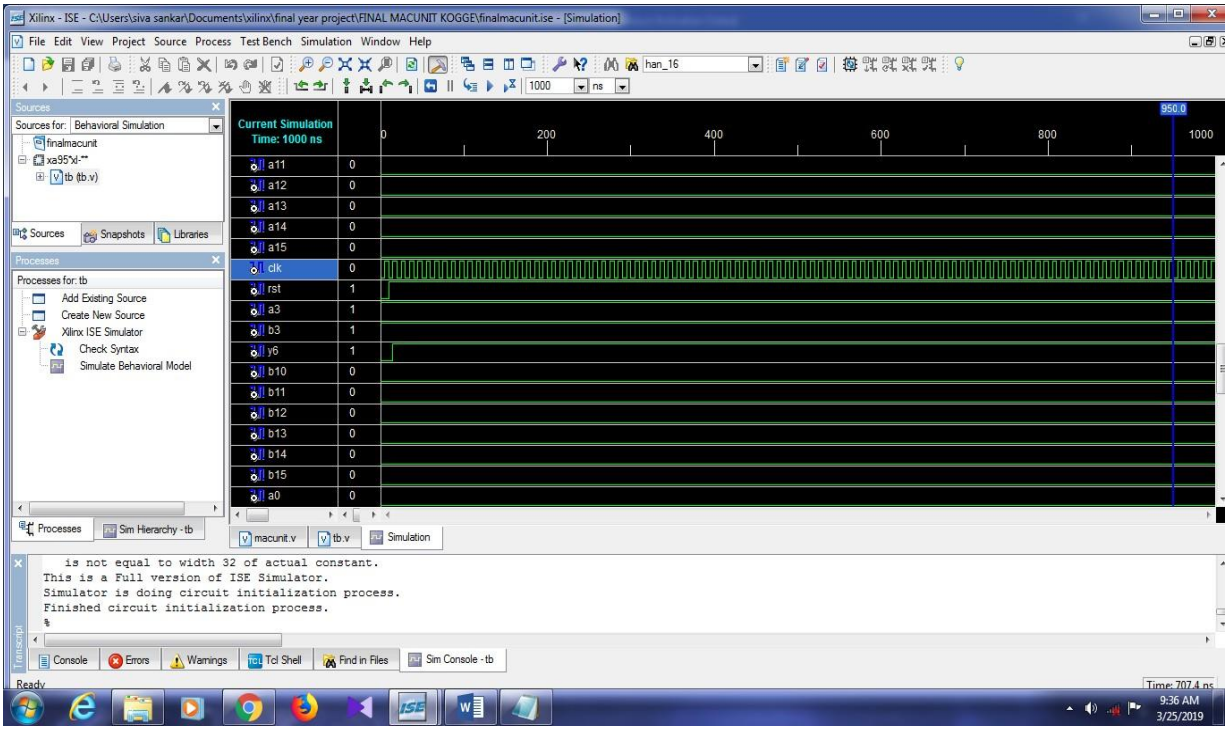

Figure 4: 32-bit MAC unit using kogge-Stone adder

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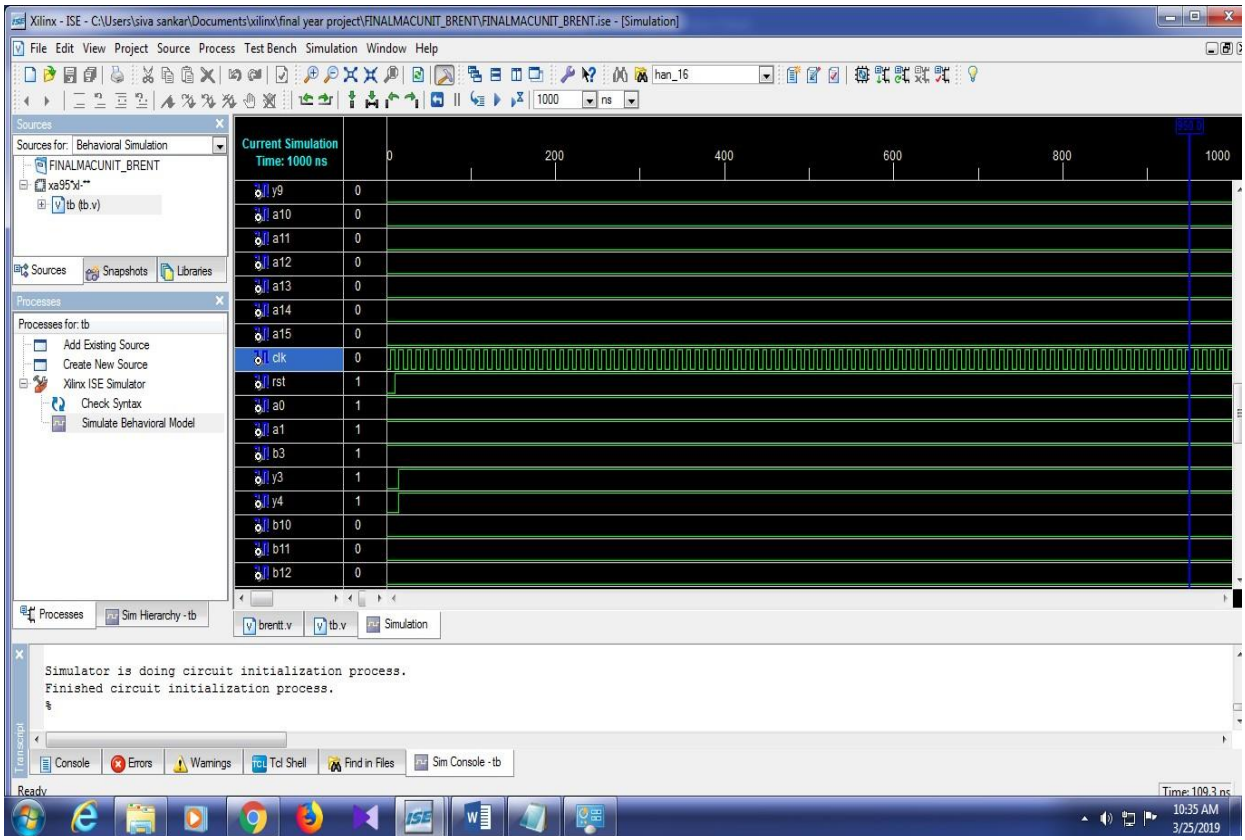

Figure 5: 32-bit MAC unit using Brent-Kung adder

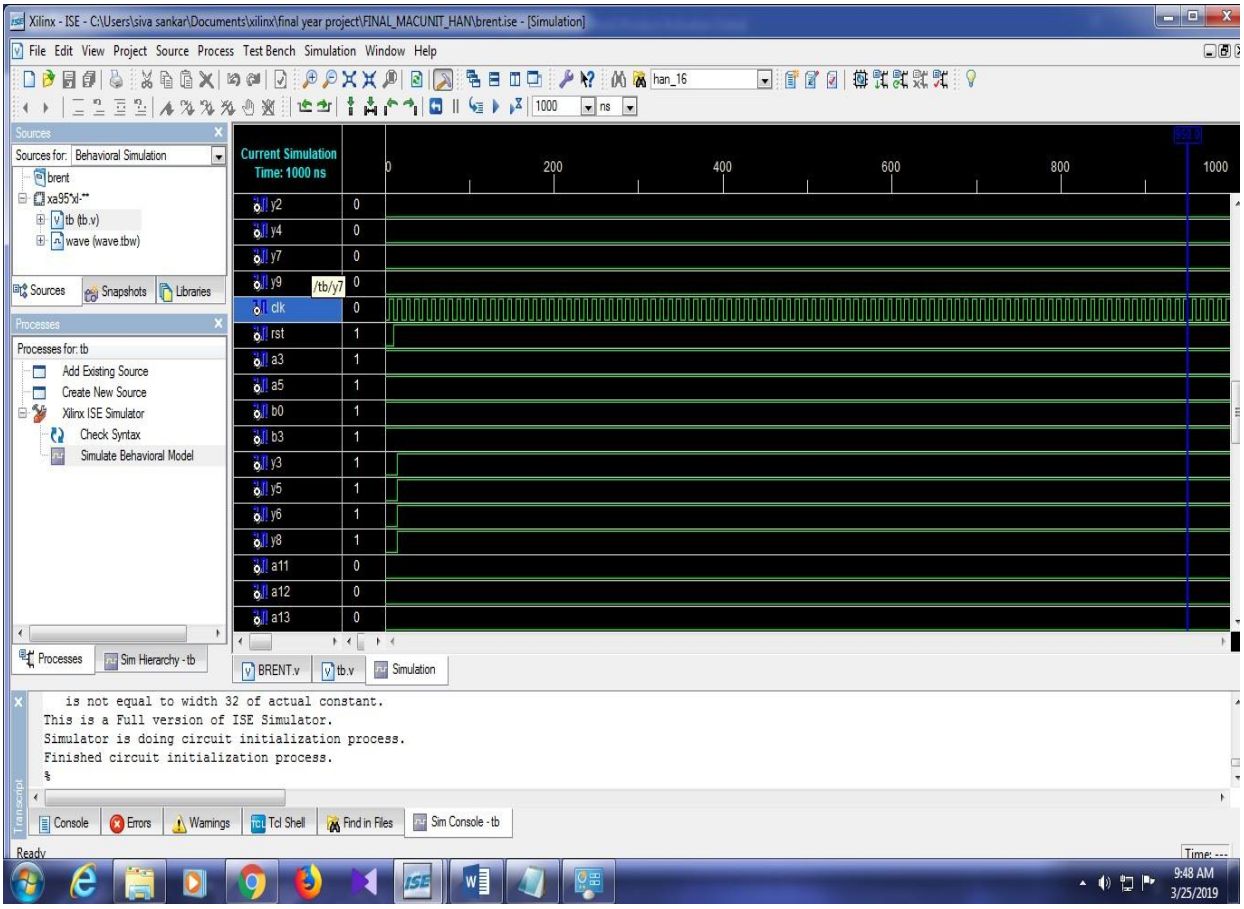

Figure 6: 32-bit MAC using Han-Carlson adder

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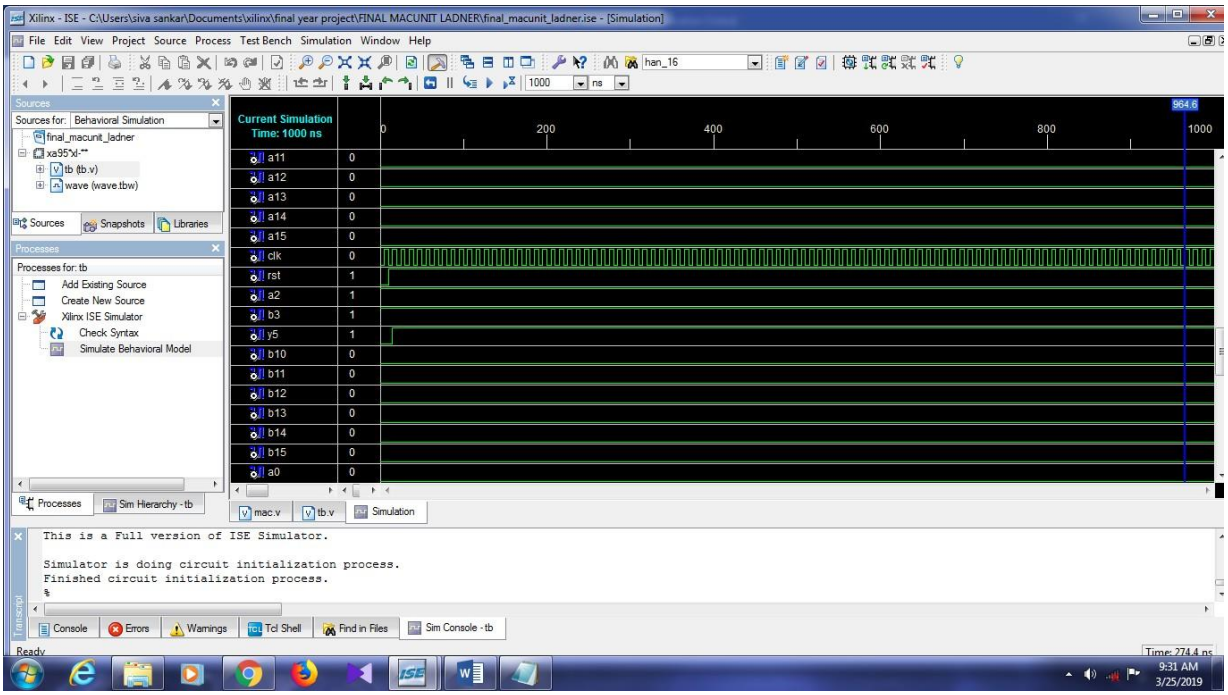

Figure 7: 32-bit MAC using Ladner Fischer adder

V. CONCLUSION

From synthesis results it has been observed that a 64-bit carry save adder is taking maximum area on the chip, but its combinational logic delay is less in comparison of carry look ahead adder circuit. Carry save adder is found good in case of less power consumption as compared to the other two adders. However, when these topologies of adders are in turn combined with array multiplier for implementing a MAC unit. It consumes the area almost equivalent to that of the other adders. But the routing delay of the circuit is less as compared to the MAC unit combined with the other adders. Power consumption is again an add on advantage in the circuit as it consumes less power i.e. 0.227W as compared to other adders. Hence, it is concluded that MAC unit implemented using carry save adder is useful for the low power applications, but it is not useful for the applications where area on chip is a major constraint. The Multiplier-accumulator (MAC) unit supports large number of digital signal processing (DSP) applications. It also furnishes signal processing ability to the microcontroller for various applications such as servo/audio control etc. MAC, being an execution unit in the processor implements a 3-stage pipelined arithmetic architecture which optimizes 16×16 multipliers.

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