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A High Linearity & High Stability Cascode CMOS LNA for RF Front-End Applications

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Abstract: In this research paper, a high linearity CMOS LNA with source degenerate topology followed by cascode topology is presented. The circuit is implemented on ADS using TSMC 45nm technology using Intermodulation distortion technique for RF front end applications. The LNA is having S11=-70.841dB, S12=-41.067dB, S22=-28.018dB, S21=14.072dB and NF =4.060dB from a 1V power supply and the circuit is having an IIP3=9dBm at 2.4GHz frequency.

Keywords: LNA, Cascode topology, Source degenerate topology, Intermodulation distortion Technique.

I INTRODUCTION

Radio frequency refers to the electromagnetic signals used in wireless communication. This includes the waves ranging from few 3 KHz to 300 GHz where frequency refers to the rate of oscillations (of the radio waves). The waves propagate at the speed of light in free space carrying voice, video and data at microwave frequency.[1] RF communication includes many industrial applications like mobile platform networking ,radar system, remote monitoring and many more. In, contrast RF modules, transceivers and SOCs often includes data link layer for supporting one or more communication protocols. One of the major wireless application: Zigbee IEEE 802.15.4 [2]; at 2.4 GHz requires devices with low power consumption, high data rate with simple networking protocols. With its application like WPANs (wireless personal area network) and internet of things are implemented using mesh networking topologies in which the network setup consists of nodes capable of interacting with each other. The major block of the RF front end receiver section includes low noise amplifier which increases the amplitude of the weak RF signal for its processing at the receiver end without adding noise or distortion to the signals. The transceiver architecture designed for wireless sensor network requires low power consumption and its configuration and designing is based on designers' requirements. Its important [3] characteristics include dynamic range, selectivity, sensitivity linearity, leakage effect and image band rejection ratio. However, the important characteristics of LNA are bandwidth of operation, stability, linearity supply voltage and chip area optimising and controlling these parameters requires adequate knowledge of active devices and components and there method of fabrication with fewer trade-offs. This paper is simulated at 2.45GHz ISM band which stands for industrial, scientific and medical band defined by ITU radio regulations which are internationally reserved for radio frequency applications. Organisation of this paper is as follows section II gives the brief description of the topologies, intermodulation technique and matching circuits. Section III describes the circuit and simulation results and comparison of work is done. In section IV, conclusion is given.

II CIRCUIT IMPLEMENTATION

In this paper, the circuit is implemented using a cascode topology [4] which consists of common source stage of the Ist amplifier connected to the common gate stage of the second amplifier. This topology provides better stability, better gain, input output isolation and high slew rate. However, it causes higher input impedance due to the miller effect causing reduction in the gain which can be optimized using gain boosting technique or adjusting the biasing currents. The source degenerate topology with inductive termination provides an efficient input matching network of 50 Ω input resistance without the resistive thermal noise. The source degenerate reactance causes the wideband CMOS LNA to attain minimum noise figure and for attaining minimum input power condition another inductor is placed at the gate of the MOSFETs so that the combined network including C_{ex} can resonate at the desired frequency of operation. However, the excessive source inductance can cause LNA to oscillate because of higher gain at high frequency. The input matching network allows the system to attain minimum S_{11} [5] without introducing additional noise. Main transistor section ensures that the system attains high linearity, high gain and minimum noise figure at the time of proper input and output matching network. The input and output impedance matching network ensures the maximum power transfer by minimizing the reflections which is attained when $Z_L=Zs^*$. Intermodulation distortion technique is defined as a method of interaction of two or more signals in a nonlinear way. The intermodulation product generates signals due to the addition and differences of the original set of signals. This method improves the third order intercept point by using the passive components which forbids the use of auxiliary amplifier for the suppression of the third order distortion components and therefore circuit does not incur extra power consumption.

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III. CIRCUIT DESIGN

The given circuit is implemented using a pie matching network through C_1,,L_1 and C_2 having 2 degrees of freedom. The transistor M1 forms a source degenerate topology with inductor Ls to provide a 50Ω termination. Thus, improving the linearity and gain of the circuit. The external inductance Lg and Ls and capacitance Cex are found to be resonating at 2.45GHz frequency. The transistor M2 forms the cascoded structure which provides the input and output isolation. The increase in the input resistance of the circuit causes the gain of the circuit to reduce which is optimized by adjusting the biasing currents. The resistance at the input of M2 causes the reduction in the noise figure of the circuit. The linearity or IIP3 is improved by IMD technique implemented using M3 PMOS folded transistor by cancelling the first and third g_{m1} and g_{m3} with those of M1.

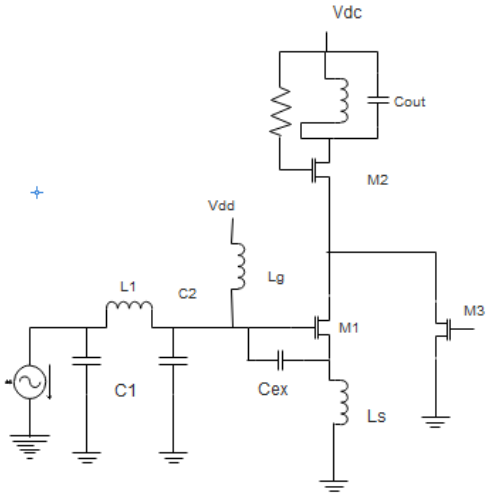

Fig. 1: Circuit Diagram for Proposed LNA

$$z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega Cgs} + \frac{gmL_s}{Cgs}$$

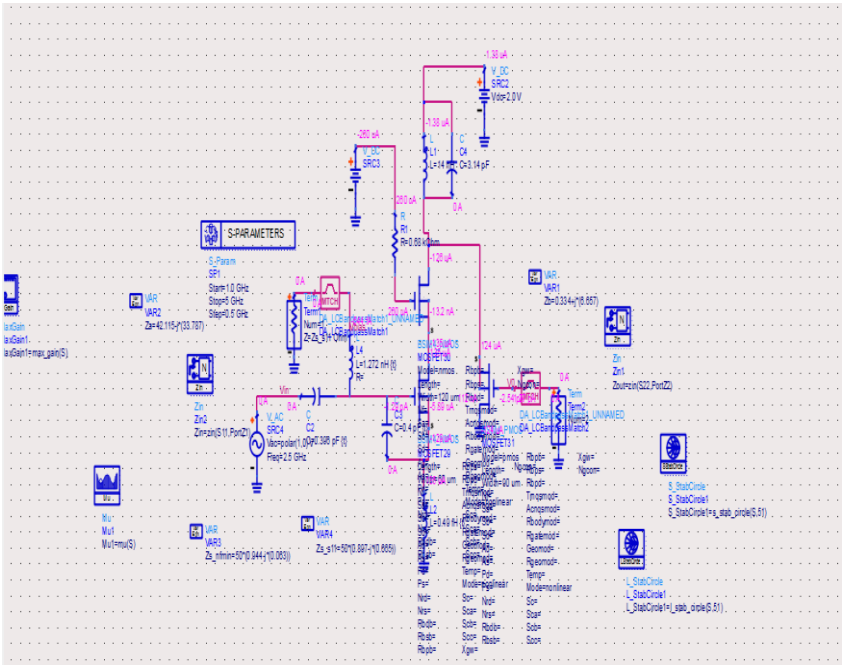

Fig. 2: Schematic for Proposed LNA

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IV SIMULATION RESULTS AND COMPARISON

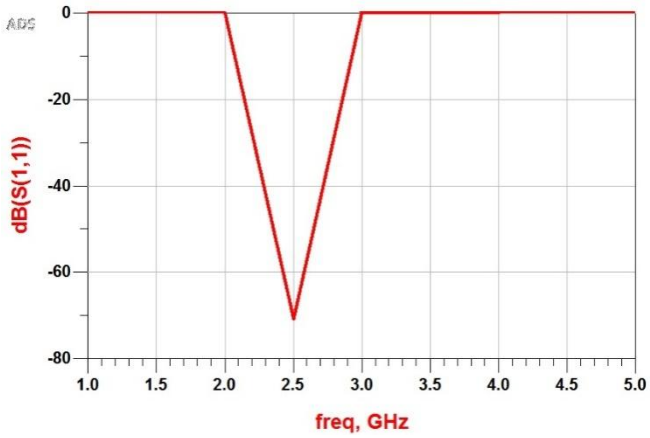

Fig. 3: Input Return Loss

The S_{11} parameter is called input voltage reflection coefficient. It gives the estimate of the input RF signal bounced of the LNA at 2.45 GHz. S_{11} is -70.841dB.

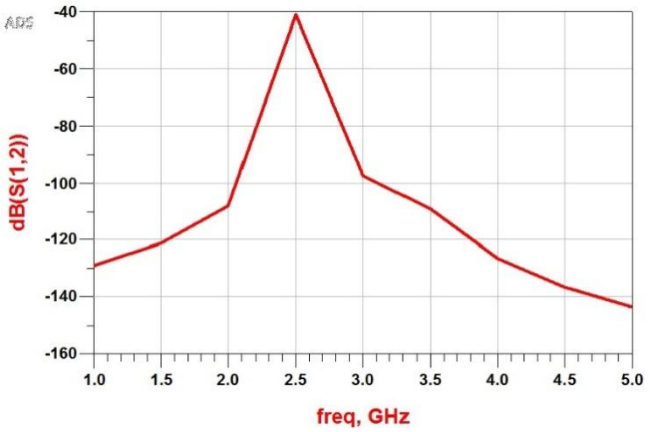

Fig. 4: Reverse Transmission Coefficient

S_{12} is also called as reverse transmission coefficient. It determines the amount of input signal reflected back or the amount of isolation between the input and the output ends. The S_{12} parameter at 2.45GHz is found to be -41.067dB.

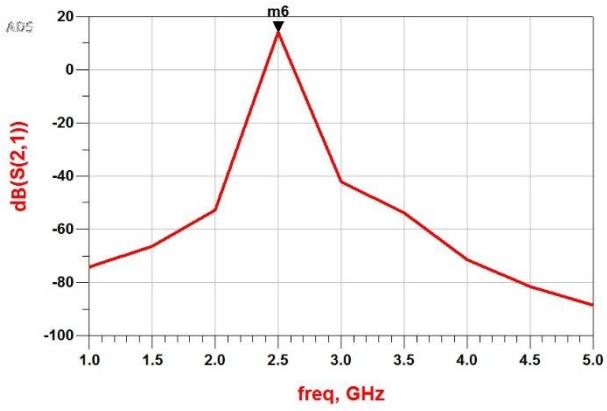

Fig. 5: Forward Transmission Coefficient

S_{21} is also called as forward voltage gain or forward transmission coefficient. It measures the power gain of the LNA. The S_{21} parameter at 2.45 GHz is found to be 14.073dB.

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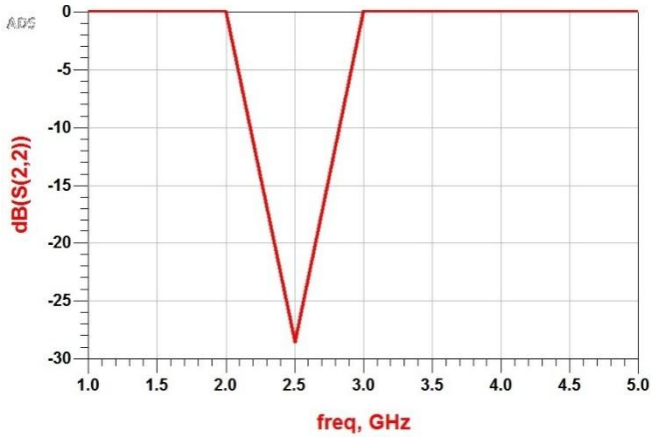

Fig. 6: Output Reflection Coefficient

The S_{22} is also called as output voltage reflection coefficient. It determines the matching between the load impedance and output impedance. For this circuit the S_{22} parameter is found to be -28.018dB at 2.45 GHz frequency.

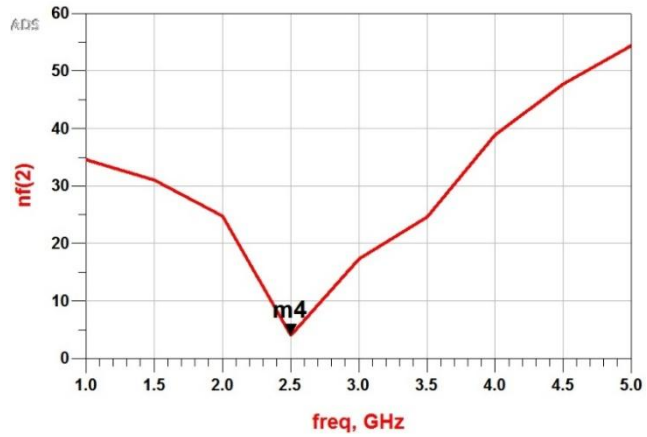

Fig. 7: Noise Figure

The noise figure is a measure of degradation in the signal to the noise ratio. The lower the value of a noise figure the better is the performance of the receiver. At 2.45GHz, the noise figure for the circuit is found to be 4.060dB.

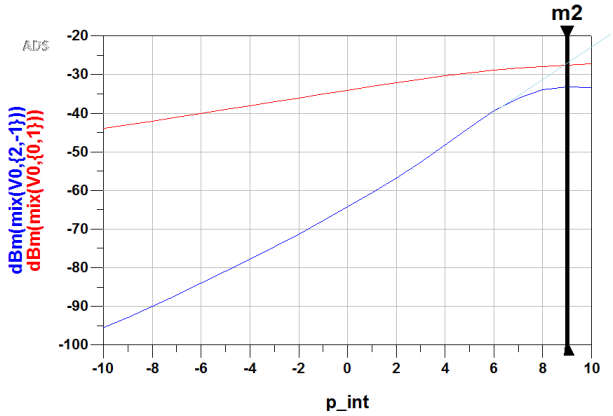

Fig. 8: Third Order Intercept Point

LNA along with having high amplification and noise figure should also have high linearity. The third order intercept point is a measure of linearity of the circuit. For this circuit it is found to be 9.0 dBm which shows that the circuit is having good gain and good linearity without affecting the noise performance. Infact good linearity of the circuit also causes the system to become more stable. Thus, it [6]implies that the circuit can have either high gain,noise figure with poor linearity or low gain low noise figure or high linearity.

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$$IIP_3 = 10\log\left(\frac{4}{3}\left|\frac{g_m}{g_m^{11}}\right|\right)$$

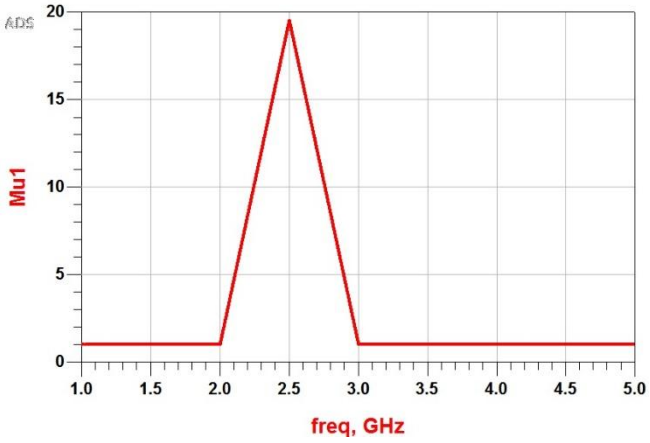

Fig. 9: Stability

Stability of an LNA [7] measures the tendency of an amplifier to oscillate. From LNA perspective, it can be either unconditionally stable or potentially unstable. Oscillations occur when there is an improper matching between the output impedance and load impedance or at the source end. The stability factor of an LNA is determined by two factors Rollett stability factor or Mu. (Mu>1) is the sufficient and necessary condition for an unconditional stability for a two port network.

Rollett stability factor or K>1 for unconditionally stability:

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

where

$$\Delta_s = S_{11}S_{22} - S_{12}\,S_{21}$$

Table 1: Results obtained for Proposed LNA

Technology (nm)	45	IIP_3(dBm)	9.0
S_{11}(dB)	-70.841	Power consumption(mW)	3.59
S_{12}(dB)	-41.067	Frequency(GHz)	2.45
NF(dB)	4.060	Supply(V)	1
S_{22}(dB)	-28.018	S_{21}(dB)	14.073

Table 2: Comparison of Proposed LNA with other Published Works

Ref.No.	[8]	[9]	[10]	This work
Tech(µm)	0.13	90nm	45nm	45nm
NF(dB)	3.34	4.34	1.42	4.060
S_{11}(dB)	-16.5	-11.32	-18.43	-70.841
PDC(mW)	3.9	17.4	1.98	3.54
IIP_3(dBm)	-10	8.7	-9.87	9.0
Supply(V)	0.9	1	1	1
Freq(GHz)	2.44	2.44	2.45	2.45

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V CONCLUSION

The above circuit is implemented using a source degenerate topology providing an efficient input matching of 50Ω and noise figure of 4.060dB. It is followed by cascode topology which provides input and output isolation with better stability. The circuit is found to be consuming 3.54mW of power for RF front end applications and attains a S_{11} = 41.067dB and IIP3 of 9.0dBm, with a stability factor of 18 which is best reported so far.

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