IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 8, Issue 10, October 2019

Design of Low Power Vedic Architecture using CSA & UTS : A Review

Vikram Kumar Jha[1], Mrs. Swati Gupta[2]

Student, ECE, Vidhyapeeth Institute of Science & Technology, Bhopal, India[1]

Assistant Professor, ECE, Vidhyapeeth Institute of Science & Technology, Bhopal, India[2]

Abstract: Multipliers are main building block of ALU, which improves the speed of many functions like Fourier transformation, digital filters and Digital Signal Processor (DSP). For any function we need to reduce the delay in system. Vedic mathematics provides mathematical approaches to increased speed and reduced power consumption as in comparison to conventional multiplier designs. Vedic multiplication algorithm with Vedic mathematics Urdhava Tiryakbhyam Sutra (UTS) method and Carry Select Adder (CSA) technique are useful to reduce power. UTM means vertically and cross wise vedic mathematics. It is ancient Indian technique used for decimal number multiplications. The speed of the computation process is increased and the processing time is reduced due to decrease of combinational path delay compared to the existing multipliers. Leakage power and low speed has become a general issue in circuit design. In our proposed multiplication algorithm, we get less time delay compared to other algorithms. In this paper, Low Power Vedic Architecture is designed reviewed. These Vedic multiplier architectures are decrease in the power consumption and generate the results faster.

Keywords: VLSI, CSA, Vedic Multiplier, RCL, High Speed, Urdhava Tiryakbhyam Sutra

I. INTRODUCTION

Multiplication is one of the essential and mostly used functions in computer operations. Arithmetic logical unit is basic blocks in Digital Signal Processing applications and in arithmetic & logical operation multiplication is the basic function to be implemented. Multipliers are the key block in high speed arithmetic logic units, multiplier and accumulate units, digital signal processing units etc. [5,6] With the increasing constraints on delay, more and more emphasis is being laid on design of faster multiplications. High speed multipliers in multiplication operations redudce their execution time. The execution time of a DSP chip still depends on the multiplication time.[2,4] The recent improvement of technologies in many digital and signal processing applications, the need of high speed processors increased. The Vedic multipliers based on Vedic mathematics are presently under focus on one of the fastest and low power multiplier.[4] There are sixteen sutras in Vedic multiplication in which “Urdhva Tiryakbhyam” has been noticed to be the most efficient one in terms of speed. [11] A large number of high speed Vedic multipliers have been proposed with Urdhva Tiryakbhyam Sutra & CSA technique. [8,11]
This paper is organized into three sections. Firstly a brief study of different types of digital adders architecture and working will be discussed in Section II. We will be discussing about the hardware requirements , speed of switching advantages and disadvantages by comparing the results obtained by exhaustive simulations of Carry Select Adder (CSA), Ripple Carry Adder (RCA) and Carry Look Ahead Adder (CLA) in Section III. Conclusions drawn after comparing results and future work proposed will be discussed in the last section IV.

II. BACKGROUND & RELATED WORKS

The design of various adders such as Full adder, Carry Look Ahead Adder (CLA), Carry Skip Adder (CSkA), Carry Save Adder (CSA), Ripple Carry Adder (RCA), Carry Increment Adder (CIA), Carry Select Adder (CSlA) and Carry Bypass Adder (CBA) are in used. [3] The each and every adder is named based on the propagation of carry between the stages. Accurate operation of a digital system is very important component in digital systems because of their use in basic digital operations like subtraction, multiplication and division. In this section we will review the Urdhava Tiryakbhyam Sutra(UTS), Full Adder, Carry Select Adder (CSA), Ripple Carry Adder (RCA) and Carry Look Ahead Adder (CLA).

A. Urdhava Tiryakbhyam Sutra

Meaning of the Urdhava Tiryakbhyam Sutra(UTM) is “vertical and cross-wise”. The least significant bits of the two numbers are first multiplied vertically, followed by addition of the products got by cross wise multiplication of both the digits and finally the most significant bits of the two numbers are multiplied vertically. [8] The result of the

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 8, Issue 10, October 2019

multiplication of the two numbers is got by adding up all the products received in the three steps, i.e., addition of the partial products obtained by vertical multiplication and cross-wise multiplication.
Let the two 2-bit numbers be X_2X_1 and Y_2Y_1;
Result: $X_1Y_1 + (X_2Y_1 + Y_2X_1) + X_2Y_2$.
This Same pattern is followed in multiplication. The numbers are divided into two equal parts, then vertical & crosswise multiplication and addition is done to gain the partial products and finally the sum of the partial products gives final result [4,8]. For two 4-bit numbers $X_4X_3X_2X_1$ & $Y_4Y_3Y_2Y_1$ UTM is implemented in their multiplication. The UTM method as applied to two 2-bit numbers, Hence for the multiplication of two 4-bit numbers there is a requirement of four 2-bit multipliers following the UTM.
Consider two N-bit numbers Xn Xn_{-1} … X_2X_1 and Yn Yn_{-1} … Y_2Y_1. They are to be divided into two halves before multiplication. The final result of multiplication of two N-bit numbers thus require four N/2 bit multipliers following UTM , and these N/2 bit multipliers would further require four N/4 bit multipliers employing UTM and so on until the fundamental 2-bit multiplier is reached.

B. Ripple Carry Adder (RCA)
The logical circuit using multiple full adders used to add bit numbers. Full adder inputs a Cin, which is the Cout of the previous adder in shows in fig.1. This adder is called ripple-carry adder, since each carry bit ripples to the next full adder. [6,9] Note that the first full adder may be replaced by a half adder (Cin = 0). Layout of ripple-carry adder is in shows in fig.1, which allows for fast design time; the ripple-carry adder is relatively slow, because each full adder must wait for the carry bit to be calculated from the previous full adder. Each full adder requires three levels of logic. The gate delay can easily be calculated by inspection of the full adder circuit.

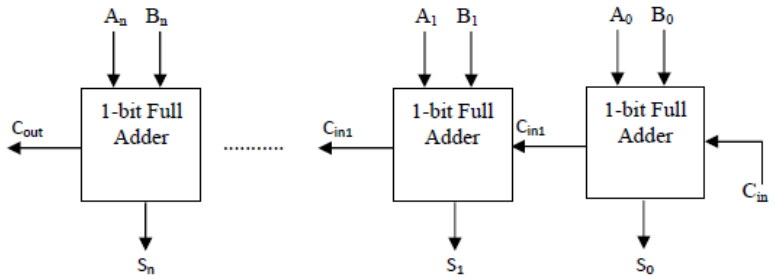

Figure 1: Block Diagram of n-bit Ripple Carry Adder

C. Carry Select Adder (CSA)
A carry-select adder is a way to implement an adder which is a logic element that computes the n+1 -bit sum of two n-bit numbers. Carry-select adder generally consists of 2 RCA and multiplexer. Addition of two n-bit numbers with a CSA is done with two adders in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one shows in fig.2 [10,14].

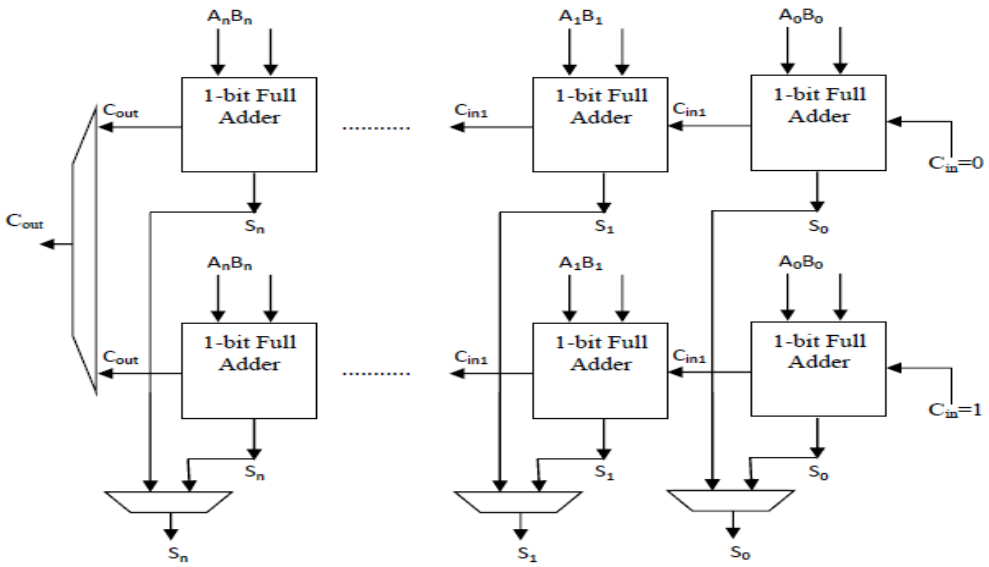

Figure 2: Block Diagram of n-bit Carry Select Adder

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 8, Issue 10, October 2019

D. Carry Look Ahead Adder (CLA).

Look ahead carry generator is a fast adder. In the ripple carry adder the carry output of each full adder stage is connected to the carry input of the next higher order stage. [9,12] That is why the sum and carry outputs of any stage cannot be produced until the input carry occurs, this leads to time delay in the addition process. This delay is called the propagation or path delay.

For each output carry are expressed in sum of product form, thus they can be implementation using $AND-OR$ logic or $NAND-NAND$ logic. Carry $C2C3$,4 are using $AND-OR$ logic. By using a look ahead carry generator 4 bit parallel adder can be constructed. In this designing each sum output requires two exclusive OR gates. The output of first XOR gate generates Pi and the AND gate generatesGi. The carries are generated using look ahead carry generator and applied as inputs to the second XOR gate. Other, inputs to XOR gate is . [3,7] Thus second XOR gate generates sum outputs. Each output each generated after a delay of two levels of gate. Thus outputs $S2$ through $S4$ have equal propagation delay times [18]. the pin diagram and logic symbol for 4 bit parallel adder with look ahead carry generator. It has 4 bit inputs are ($F3$, $A2$, $A1$, $A0$) and ($B3$, $B2$, $B1$, $B0$) then output are ($S4$, $S3$, $S2$, $S1$, $S0$) . Carry look ahead generator accepts up to four pairs of active low carry propagate and carry generate high carries across four groups of binary adders. The look ahead carry adder has active low carry propagate and carry generate outputs which may be used for further levels of look ahead shows in fig.3.

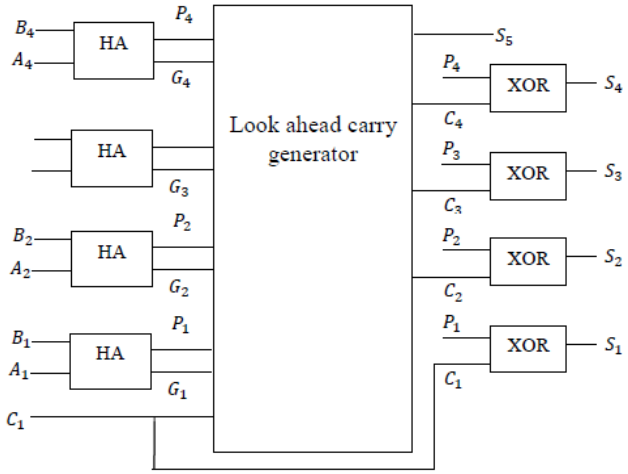

Figure 3: 4-bit Parallel Adder with Look Ahead Carry Generator

III. VEDIC MULTIPLIER

Multipliers have dominant role in most of the VLSI design. VLSI system designers are therefore searching for the advanced multiplier structure.The main limitation of multipliers is that it has a large number of reduction stages and make the whole system much complicated. The ancient Vedic algorithm is proved to more efficient in speed and power saving. Also, complexity can be limited with less area. An 8x8 multiplier is designed using the Urdhva Tiryagbhyam sutra, theorized Vedic multiplication formula. Consider two 8-bit operands and each operand is grouped in to two 4-bit operands. The 8-bit multiplication can be accomplished as the 2-bit multiplication of 4-bit operands [6]. The whole multiplication process can be performed in three stages. [4,11]

Partial products are induced using four 4-bit Vedic multipliers. Each 4-bit multiplier comprises four 2x2 multiplier, one 4bit parallel adder and one carry save adder. The 2x2 multiplier is considered as the basic block in the multiplier design. A 2-bit Vedic multiplier [7] can be designed with a minimum of eight logic gates; six AND gates and two XOR gate. [8]. The intermediate partial product matrix generated in the first stage is reduced to a height of two. Partial product reduction can be achieved with eight full adders. By using a 8-bit multiplier having high speed and low power consumption can be obtained using the Vedic algorithm.

IV. RESULTS & CONCLUSION

In this survey paper we have simulated adders and multipliers using Xilinx 14.2i version. The gate delay count in CSA offers higher speed than the other two. 4 bit, 8 bit Vedic multipliers have been overviewed by simulation. Vedic multipliers designs show lesser delay and use lower power than existing multipliers. These multipliers can be used in DSP and communication applications which require higher speed and lower power consuming systems.

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 8, Issue 10, October 2019

Figure 4: Multiplier Simulation Waveform of 4-bit Number

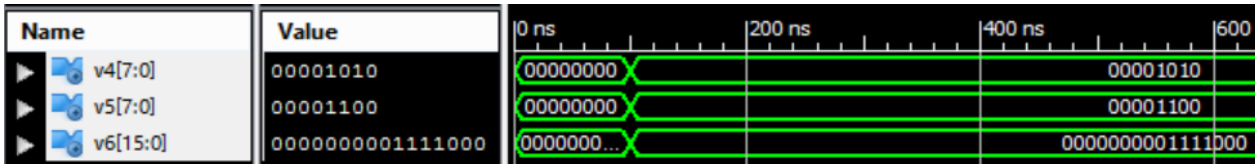

Figure 5: Multiplier Simulation Waveform of 8-bit Number

Future Scope: In future one can obtained results for 16 bits or higher number of bits so that the convergence of results can accurately predicted. The existing multipliers can be replaced with Vedic Multipliers.

REFERENCES

[1]. Assila Yousuf, Mohamed Salih K.K, "Comparison of Sleep Transistor Techniques in the Design of 8-Bit Vedic Multiplier", International Conference on Emerging Trends and Innovations In Engineering And Technological Research, 2018 IEEE.
[2]. Paras Gulati,Harsh Yadav, Manoj Kumar Taleja "Implementation of an efficient Multiplier Using the Vedic Multiplication Algorithm" 2016 International Conference on Computing, Communication and Automation (ICCCA) IEEE (2016).
[3]. H. V. Ravish Aradhya"Design and Performance Comparison of Adiabatic 8-bit multipliers" 2016 IEEE.
[4]. M. Akila, C. Gowribala, S. Maflin Shaby "Implementation of High Speed Vedic Multiplier using Modified Adder' 2016 International Conference on Communication and Signal Processing, IEEE(April 2016).
[5]. Yogendri, Anil Kumar Gupta "Design of High Performance 8-bit Vedic Multiplier" 2016 IEEE, 978-1-5090- 0673-1/16
[6]. S Nikhil† and Mrs. P. Vijaya Lakshmi "Implementation of a High Speed Multiplier desired for HighPerformance Applications Using Kogge Stone Adder".
[7]. M. Akila, C. Gowribala, S. Maflin Shaby "Implementation of High Speed Vedic Multiplier using Modified Adder" International Conference on Communication and Signal Processing, April 6-8, 2016, India.
[8]. Yogendri and A.K. Gupta, "Design of High Performance 8-Bit Vedic Multiplier," 2016 International Conference on Advances in Computing, Communication, & Automation (ICACCA) (Spring), pp. 1-6, Dehradun, 2016.
[9]. Sreehari Veeramachaneni, Kirthi M Krishna, Lingamneni Avinash, Sreekanth Reddy Puppala , M.B. Srinivas "Novel Architectures For High Speed and Low Power 3-2,4-2, and 5-2 Compressors" 20th International Conference on VLSI Design IEEE (Jan 2007).
[10]. H.P. Patil and S.D. Sawant, "FPGA Implementation of Conventional and Vedic Algorithm for Energy Efficient Multiplier," 2015 International Conference on Energy Systems and Applications, pp. 583-587, Pune, 2015.
[11]. R. Sharma, M. Kaur and G. Singh, "Design and FPGA Implementation of Optimized 32-Bit Vedic Multiplier and Square Architectures," 2015 International Conference on Industrial Instrumentation and Control (ICIC), Pune, 2015, pp. 960-964.
[12]. G. Challa Ram, D. Sudha Rani, Y. RamaLakshmanna, K.Bala Sindhuri "Area Efficient Modified Vedic Multiplier" 2016 International Conference On Circuit, Power And Computing Technologies, IEEE (March 2016).
[13]. Josmin Thomas, R. Pushpangadan, Jinesh S "Comparative Study of Performance Vedic Multiplier on the Basis of Adders Used" 2015 International WIF Conference on Electrical and Computer Engineering (WIECON-ECE) IEEE (December 2015).
[14]. Saji. M. Antony, S.Sri Ranjani Prashanthi, Dr. S. Indu, Dr. Rajeswari Pandey "Design of High Speed Vedic Multiplier Using Multiplexer Based Adder", 2015 International Conference on Control, Communication & Computing India(ICCC) IEEE(November 2015).
[15]. Manoranjan Pradhan, Rutuparna Panda, Sushant Kumar Sahu "Speed Comparsion of 16*16 Vedic multiplier", International Journal of Computer Applications, Vol.21, No.6, IEEE(May 2011).
[16]. Vijaya Lakshmi "Performance Analysis For Vedic Multiplier Using Modified Full Adders" International Conference on Innovations in Power and Advanced Computing Technologies (iPACT) IEEE (2017).