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# High Speed and Low Power Consumption Multipliers using FinFET Technology

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**Abstract:** Over the years, the focus of IC Enterprises hasn't shifted from optimizing various performance parameters to validate Moore's law. These enterprises are still striving to scale down these parameters. However, near 20 nm range challenges posed regarding the strength, various side-effects hampering the functionality of the IC. With an aim to bring out a solution this research has been done. The outcome assessing parameters are decreased power dissipation and delay in an Array multiplier implemented using FINFET instead of MOSFET. Tool used is HSPICE of synopsis. Simulation is done and comparison drawn between FINFET and MOSFET implementation for 32nm technology. The outcome validates the advantage of FINFET over MOS.

**Keywords:** FinFET, Average Power, Multiplier

## I. INTRODUCTION

As the IC fabrication processes approached nanometer-technologies, high frequency of operation and compactness, low power consumption became a necessity, be it a portable device or a non-portable one. In battery operated case long battery backups becomes the requirement and the non-battery one faces cooling and packaging issues. Keeping in mind the optimization of all these parameters keeping in mind a new parameter is derived termed as "power budget" [3]. Scaling-down gate of MOSFET in nm faces exceptional difficulty due to the extreme quick channel effect that leads to sharp growth in the sub threshold and gate –oxide leakage. It is reported by Zhichao Lu et al [1]. FinFETs are encouraging substitute for bulk MOSFET at the nanoscale due to the fact that the FinFET manufacturing process and MOSFET is almost identical, as reported by Ajay Bhoj et al [2]. FinFET (Fin-Type Channel) [4] offer favourable strength–delay tradeoff and improved behaviour (brief channel effect) in nanometer. Its aftermath is the enhanced performance. This is reported by M. Prathima et al [5].
We can easily perceive the market trend of miniaturization. The inflow of high speed gadgets is the result of nothing but miniaturization. However, the continuous miniaturization brought into notice the constraints in shape. The electricity intake, chip density and running frequency have elevated due to superior nanometer system technologies within the battery-operated portable devices [1] - [3]. For externally powered devices without battery, power consumption is crucial because then its packaging density and cooling designs, strength of the device along with its reliability potential is affected. Hence the VLSI designs revolve around innovation of designs and innovative fabrication processes to cater the overall performance requirements within a practical "power budget". The processing speed and area are also essential parameters and optimum tradeoff must be carried out in a circuit design. As far as applications are concerned, Samsung Electronics has incorporated FinFET in its 14nm processors. This processor is used in latest Samsung smartphone, the Samsung Galaxy S6

## II. FINFET TECHNOLOGY

What grabs the attention towards FINFET is its structure when kept along with other traditional MOS, wherein the conducting channel is sandwiched by a thin fin and this makes its body. The effective-channel-length of FinFET is measured by the thickness of fin (from source towards drain). FinFET technology grew in the University of Berkley California in hands of Chenning Hu and his colleagues. As MOS are classified into p-type, n-type depending upon the doping, similarly in FinFET, we got P-FinFET, N-FinFET. Moreover, CMOS structure and functionalities are achieved by tying together both gates of FinFET as reported by V Narinder et al [7].

Analysis of FinFET brought out that the circuit offers many advantages overcoming the challenges posed by scaling the electronics, be it "short-channel-effect" or "sub-threshold conduction". Its structure suppressed leakage current by diminishing quick-channel effect and providing near-best sub-threshold voltage swing as mentioned by Mahender Veshala et al [6][9]. In the i-gate and s-gate mode of operation, various misbehaviors were observed in the circuit because of short channel effects such as threshold voltage roll-off, surface scattering, velocity-saturation, punch-through etc. although they are less severe than conventional MOSFET, as mentioned by Ajay.N.Bhoj et al[2]. Figure 1 shows two different configurations of FinFET device.

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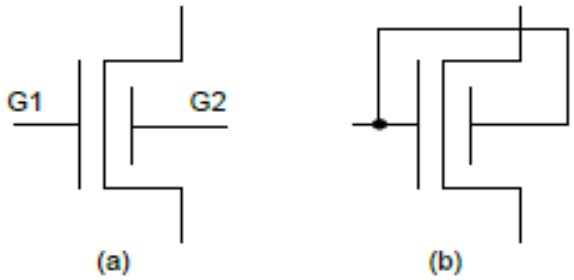


Figure 1: FinFET-Configuration (a) "Independent Gate" (b) "Shorted Gate" [9]

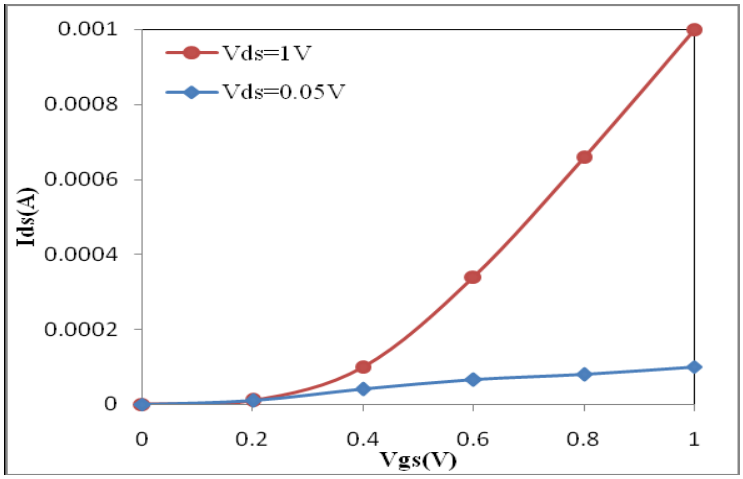


Fig.2: ID-VGS plot of double-gate N-FinFET Device of gate length $L_G$ = 32 nm

By using different logic gates, various arithmetic applications are designed. Based on the circuit requirement logic gates are implanted using Shorted-Gate (SG) FINFET or Independent gate FinFET. In former case front and back gate are tied together to achieve better current-voltage characteristics and also drive strength. In the latter case both gates are driven with different voltages which may help in decreasing transistor count of the circuit. Apart from the two, Low-Power (LP) mode and hybrid IG/LP mode are also devised to meet specific requirements. For an instance in Low-Power (LP) mode, a low voltage to n-type FinFET and high voltage to p-type FinFET is applied which affects the threshold voltage of the devices, which reduces the leakage power dissipation but on the other hand delay increases. A hybrid-IG/LP-mode is obtained by combining LP and IG modes.

Keeping in mind wide variety of applications and increasing demands research work in field of IC technology has entered nanometer range facing enormous design changes and limitations. Industry is increasing density of packaging facing complex interconnections and delay, reducing power consumption at the stake of decreased fan out and so on. Experiments done earlier for the optimization of area and fan out by considering short-circuit current as negligibly small resulted in excessive power consuming circuits. In the power budget calculation contributing parameters are total active-mode-power consumption, the power consumption by the timing circuit, and the average power dissipation due to leakage current. It is analyzed over the time that the arithmetic circuits designed using FinFETs have lower power budget reducing active-mode consumption of power to 45%, clock-power reduction up to 29%, and 53% reduction in leakage current power, with comparable speed to that of the CMOS circuits.

The industry has scaled the conventional transistors for the past six years using several innovative techniques such as high-k dielectrics and strained silicon. Even these fails to overcome difficulties due to short-channel effects, that are "Drain-Induced Barrier Lowering (DIBL)", "sub threshold-slope" and "sub-threshold leakage-current" when scaling range approaches 22nm. Dual Gate FETs then appeared a promising technology. It possesses two gates which provide more control over the channel. The two gates mitigate the effect of the drain-source electric field in the channel and thus provide superior channel control. Among DGFETs and FinFET, the latter is preferable because of the ease to manufacture, owing to the similarity of its fabrication process to that of MOS and other conventional transistors. The tri-gate version of FinFETs was recently announced by Intel as its choice of transistor for fabricating processors at the 22nm technology node.

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FinFETs have been shown to have superior on-current and off-current when compared to a conventional transistor at the same technology node. Their dual-gate structure can be exploited for innovative circuit design. E.g., application of reverse bias to the back gate of IG-mode FinFETs helps to modulate the threshold voltage Vth of the front gate. Since $V_{th}$ impacts both the sub threshold current and delay of a transistor, it can be used as a knob to make delay-leakage trade-offs.

## III. MULTIPLIER

The multipliers play a prime position in arithmetic operations in virtual signal processing programs. The existing development in processor designs aims at low energy multiplier structure utilization. So, the urge for low strength multipliers has accelerated. Subsequently the designers listen more on low energy green circuit designs. Typically, the computational performance of DSP processors is affected by its multipliers' performance. For this reason, we took a strong care to fix those drawbacks using our design. Processors performance is estimated with its multiplier's pace and delivered output. As a consequence, the usage of parallel multiplier is justified over the serial multipliers to achieve better performance. Ignoring the speed requirement multipliers can be designed to be less complex but nowadays advancement is in the area of speed and compactness and energy efficiency only.

## IV. PROPOSED MULTIPLIER DESIGN USING FINFETS

The multiplier circuit incorporated is 2 X 2 multiplier, which has been implemented using four 2-input AND gates and two half-adders, as specified in the block diagram. The total delay is only 2-half adder delay. It is reported by S.Vijaykumar et al[10]

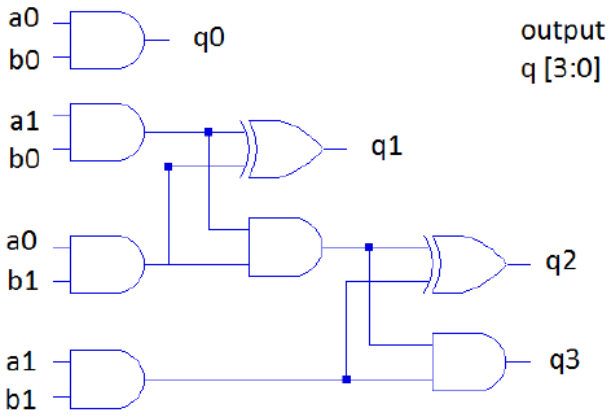


Fig.3: Multiplier Diagram

The results are derived on Synopsys HSPICE. The circuit diagram can be broken in three distinct parts input nodes (that are coded by assigning input values) gates implemented using BSIMCMG FinFET library and output nodes where output voltages are observed. Various performance parameters are analyzed like delay, average power consumption, etc.

## V. SIMULATION-RESULTS

Analysis of results obtained using HSPICE simulation is listed below. Table 1 gives the Average power in MOSFET and FinFET based Multipliers. The resultant figure clarifies the improvement achieved using FinFET

Table 1: Average Power of Multipliers

| **Metric/Circuit** | **32nm Fin-FET Multiplier** | **32nm MosFET Multiplier** |
|---|---|---|
| **Average Power(μW)** | 0.535 | 3.17 |

Another more visual way is the bar graphical representation of Average power consumption comparison in FinFET device circuit and MOSFET device circuit multiplier as shown in Figure 4. The results prove FinFET as most promising power saving and highly efficient device in the emerging IC technologies.

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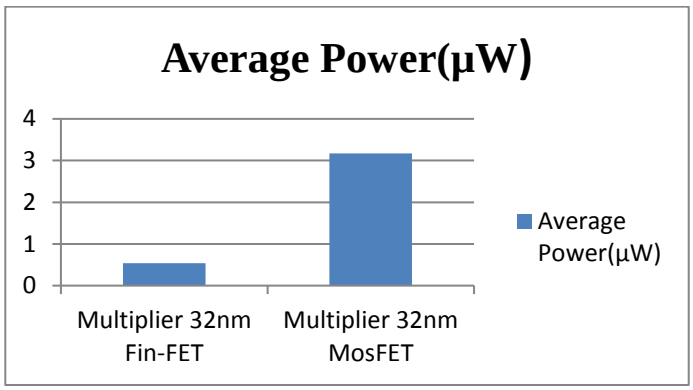


Fig.4: Average Power of Multiplier

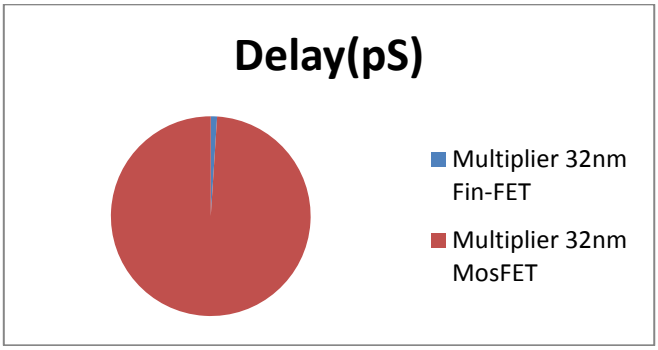


Figure 5: Delay in Multipliers

Now comes the delay analysis. Figure 5 shows tremendous reduction in delay when Multiplier is implemented using FinFET rather than in MOSFET. Below Table 2 provides the figures of delay in Multiplier for the two cases.

Table 2: Delay in Multiplier

| Metric/Circuit | Multiplier (32nm Fin-FET) | Multiplier (32nm MosFET) |
|---|---|---|
| **Delay(pS)** | 3.908 | 380 |

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## VI. WAVEFORMS

The waveforms for the multiplier circuits are obtained using Netlist in SPICE program using HSPICE software from Synopsys. The code for multiplier is obtained using the logic gates blocks, which in turn are designed using MOSFET and FinFET libraries available in the HSPICE and PTM (Predictive Technology Models). FinFETs are used in SG-mode configuration [shorted gate]. Figure 6 gives waveforms for the Inputs and corresponding outputs of the Multiplier circuit implemented using MOSFET or FinFET. The transient behavior in FinFET is improved considerably as the value of path capacitance is decreased due to use of fin as body material.

Table 3: Relevent Information for Fig 6

| Symbol | Graph | Description |
|---|---|---|
| V(a1) | Yellow | MSB for first input sequence |
| V(a0) | Red | LSB for first input sequence |
| V(b1) | Brown | MSB for second input |
| V(b0) | Light Blue | LSB for second input |
| V(q3) | Green | MSB for output sequence |
| V(q2) | Blue | Second significant bit for output sequence |
| V(q1) | Purple | Third significant bit for output sequence |
| V(q0) | Pink | LSB for output sequence |


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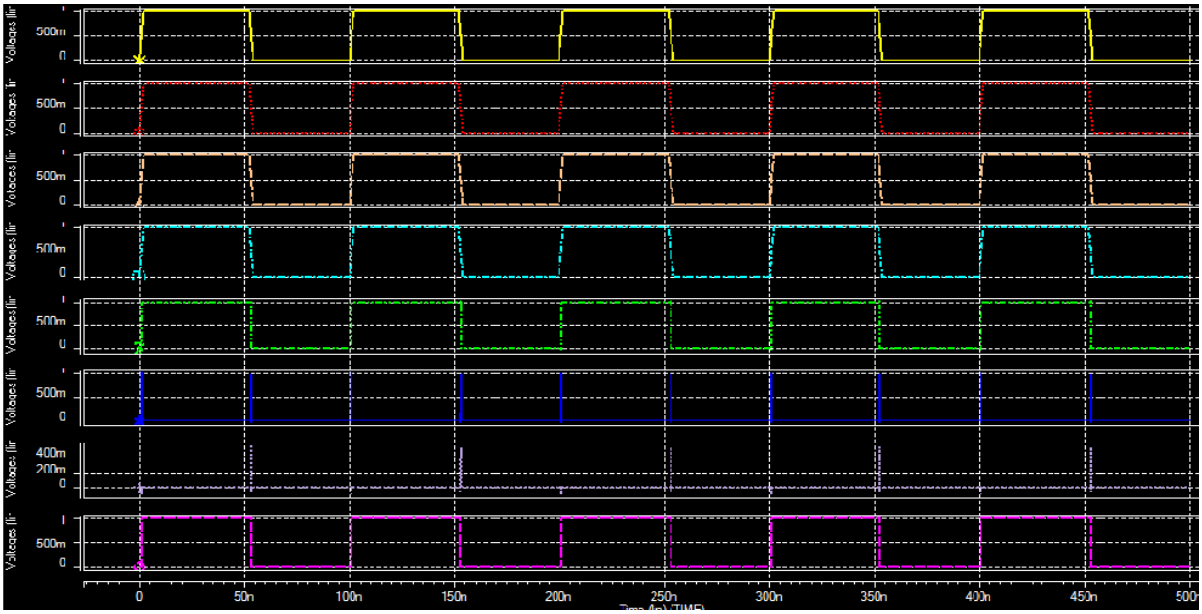


Figure 6: Input and Output waveforms for Multiplier Using FinFET/MOSFET

## VII. CONCLUSION

Beginning with the requirements we ended up to the result obtained from simulation successfully analyzing the hindrances and the possible solutions. The MOSFET occupied market over considerable time and further miniaturization drawbacks was trying to hold the development in IC technology but the advent of FinFETs overcame the slowdown in the industry optimizing th circuit blow 32nm technology which was a challenge in MOSFET era. FinFET reduced the power intake and made the circuits faster. As shown in simulation consequences, the common power consumption and slowdown are substantially reduced in FinFET than MOSFET. Furthermore, there is need to invent new generation so as to permit us to design gadgets beneath 32nm generation.

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