IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 9, Issue 2, February 2020

Power-Delay Behaviour of Digital Circuits Designed using MOSFET, CNTFET and FinFET, with the Scope of Miniaturization in these Transistors

Malti Bansal[1], Harsh Saxena[2]

Department of Electronics & Communication Engineering, Delhi Technological University, Delhi-110042, India[1,2]

Abstract: In current scenario, power–delay trade-off and downsizing in deep submicron transistors is major area of innovation. Double gated MOSFET (also called FinFET) and CNTFET are the apt substitutes to the MOSFET at the nanometer scale. MOSFET experiences sub threshold conduction at the nanometer scale, which hinders its performance. If conventional MOSFET is replaced by FinFET, a better control over its channel can be obtained which will avert sub threshold conduction in it. While replacing MOSFET with optimized CNTFET, the prevailing conduction mechanism of its charge carriers through its channel is totally replaced by novel ballast transport mechanism through the Carbon Nanotube (CNT). In this paper, power dissipation and delay in the digital applications based on above transistors are evaluated. Here Synopsis HSPICE tool is used for simulation.

Keywords: FinFET, Nanotubes, Carbon nanotube FET, Multipliers

I. INTRODUCTION

With the introduction of deep submicron technology, the need of increased speed and efficiency by employing transistors of small size with quicker switching rates is taken care of. The shrinking size of the metal oxide semiconductor FETs boosts the leakage through the channel resulting in increased dissipation of power. The slender body in MOSFET is the basic idea behind the development of FinFET. MOSFET witness troubles like leakage through substrate, short channel behavior & excessive dissipation of power. FinFET is a dual gated MOS that has two gates to modulate the channel and offers distinct merit of scaling down to a nano level, gate lengths. Both the gates work in synergy to limit the potential of the channel, combat the impact of drain leading to enhanced ability to cease Drain Induced Barrier Lowering (DIBL) which reduces channel current. The inhibition of Short Channel Effect (SCE) & the reduction in the power loss can be achieved by decreasing the width of The Fin (Tfin) as reported by P.C.Rajshree et al [1]. The DIBL and SCE shortcomings can be overcome to some extent; and facilitate further downsizing dimensions of field effect transistor by substituting the bulk body channel in the MOSFET with a nanotube made by layered carbon catenation. Carbon Nanotubes (CNT) are extensively employed in carbon nanotube field effect transistors as their transportation channels. A 'Single Walled Carbon Nanotube (SWCNT)' comprises of two-dimensional graphite sheet rolled to form a hollow tube and the sound fabricating technique of this material assures a replacement for the bulk MOSFET.
The first arithmetic application Multiplier plays a vital role in arithmetic operations in virtual signal processing programs. The existing development in processor designs aims at low energy multiplier structure utilization. So, the urge for low strength multipliers has accelerated. Typically, the computational performance of DSP processors is influenced by its multipliers performance. For this reason, we took a strong care to eliminate any existing drawback using our design. Processors performance is typically determined from its multiplier pace and delivery voltage. The second application, which is a full adder, is an elementary component in many pragmatic digital applications. Our most important application is implementation of SRAM array using FinFET technology.

II. SCALING AND LIMITATIONS OF MOSFET

Both p-type and n-type semiconductors are utilized to fabricate MOSFET. MOS transistor's complementary pairs can be used to make on-off toggling circuits with minimized delivery voltage in the form of CMOS logic. MOSFET has constantly been contracted in dimensions from several micrometers to tens of nanometer of technology parameter in modern designing. Intel commenced commercial fabrication of 32 nm technology size with even narrower channel in early 2010. The semiconductor industry follows a global standard "International Technology Roadmap for Semiconductors (ITRS)", which fixes the time bound targets for MOSFET development. The demerits with downsizing

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 9, Issue 2, February 2020

of the MOSFET have been linked with the techniques of semiconductor device fabrication, small channel MOSFETs exhibit higher body currents and reduced output impedance.

Smaller MOSFETs provides more electronic components per unit volume. Hence, more integrated chips per wafer, reducing the expenditure per chip. Evidently, the transistor density on the chip has been increasing two folds, every three years once a new technology parameter is innovated, for past thirty years. It is also presumed that small channel transistors switch quicker. The oxide thickness, channel length and channel width are the significant dimensions of the transistor. On scaling these down by equal factors, the resistance of transistor channel is not altered, but the capacitance of gate is shrinked by same amount and hence the RC delay (time constant) of the transistor. But our presumption is valid up to few micrometer technology parameters only.

In the proficient metal oxide semiconductor FETs, scaling the transistor dimensions down would not guarantee increased speed of operation in integrated circuit as the interconnection delay is more pronounced. The limitations witnessed by MOSFET Technology are lower output impedance, junction leakage increment, increased leakage through the gate-oxide, higher sub threshold conduction, process variations and interconnect capacitance. This is reported by Douglas A. Pucknell et al [24]

III. FINFET DESIGN AND TECHNOLOGY

CMOS Field effect transistors scaling shows linear variation with dimensions upto-submicrometer level, but this has attained saturation for technology parameter below-22-nm range, owing to non-uniform electrostatic distribution throughout the channel, which leads to pathetic short-channel behavior and alarming leakage through the substrate. “Multigate field-effect transistors” (MGFETs) subdue these problems at sub-22nm level because two or more gates, grasping its body provides desirable variation of the channel potential., FinFET are the most promising structures among multigate FETs from fabrication perspective, this is referred from E.J Novak et all [7]. The FinFET build is of thin doped silicon body held by the gates on two of its surface parallel to channel plane, conventionally on a “silicon-on-insulator” (SOI) substrate. FinFET operates in two modes namely: Shorted gate (SG) mk operation, the two gates are biased to same voltage to enable transistor in active region, providing maximum gate control. In the IG mode, the gates are at different voltage. The biasing of behind-gate modulates the threshold voltage (V_{th}) of the other gate, thereby controlling the off state-current (I_{OFF}) of the device. This is reported by W.Zhang et al[8]. I_{OFF} in SG-mode devices are in general more prevalent than that in IG-mode (in which the back-gate is held below the reference for n-type) because SG mode has unchangeable V_{th}, therefore its I_{OFF} cannot be controlled. Since V_{th} is altered by directly manipulating the gate work function. Thus, by setting same workfunctions for the two gates, they can be referred to as Symm-¢G FinFETs and vice versa.

Asymm-¢G SG-mode FinFETs possess fruitful characteristics of favorable steep sub-threshold gradient, negligible off-currents, and prominent high on-currents in comparison to Symm-¢G SG/IG-mode FinFETs and are reliable even at high temperature. This suggests that they could be utilized (with Symm-¢G SG-mode FinFETs whenever required) Symm-¢G SG-mode devices are used throughout the project.

IV. INTRODUCTION TO FINFET

On the advancement of ‘nanometer’ node technology, higher frequency of operation and more chips per unit wafer are consequent, thus power imparted to battery operated device is bone of contention. Increased packaging shoots up power loss also for non-portable electronic device. Thus, the design research in VLSI (very-large-scale integration) became power budget centric. Focus is now to enhance performance along with power efficiency. Here we have explored how the circuits based on FinFETs (fin-type body instead of bulk), which is likely to boost or substitute bulk transistors below 32nm node, offer an acceptable delay–power trade-offs.

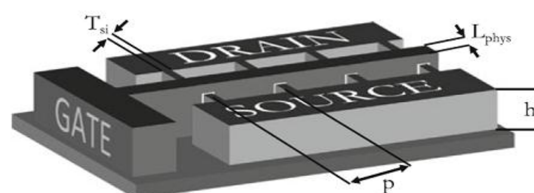


Fig.(i) Isometric view of FinFET with multiple fin

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 9, Issue 2, February 2020

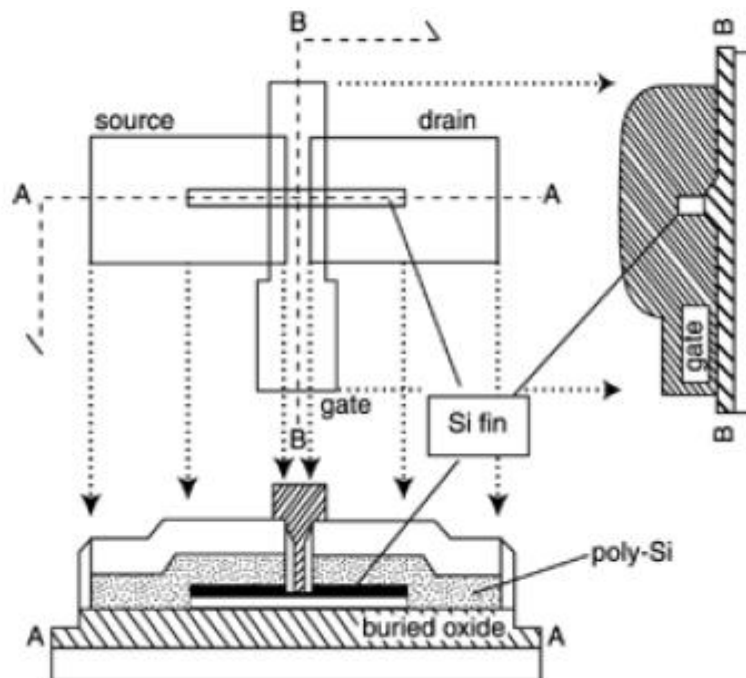
Below 22nm node, downscaling of transistors with bulk body and a channel is not achievable because of limitations in approximating dimensions of semiconductor material and deviation in habitual behavior of microelectronics. This is reported byT.J King et all [9]. Mainly two tasks are paved in this size reduction:

- Controlling the leakage current both in channel and at gate channel interface.
- Even minute variations in fabrication among devices leads to performance difference. This should be taken care of. This is reported by K.Bemstein et al [10].

FinFET is the most anticipated next generation technology combating the issues raised by constant scaling. Manufacturing of finFET and CMOS are nearly same as former is offshoot of latter. Fig (i) depicts the isometric view of a finFET with multiple fin. In finFET device, fin is the slender body instead of silicon bulk, clenched by gate region on two faces whose thickness is $\mathbf{T_{Si}}$. The width of this FET is 2nh, here n is total number of fins, refer fig.(i) for clearity. The current flow is along the wafer plane's direction, whereas the channel formation is orthogonal to the plane of the wafer. Hence finFET is a quasi-planar structure. The independent biasing of the anterior and posterior gates is provided by carving out the gate electrode at the head of the channels. Larger on current is expected through the channel on using multiple fins. The minimum distance between centres of two neighbouring fins is called Fin pitch(p), considering lithographic constraints

V. SHORT-CHANNEL EFFECT REDUCTION IN FinFET

As indicated by simulation results, size of finFET structure can be reduced upto 10nm node. The short channel effect in FinFET can be suppressed by incorporating ultra-thin fin as its body. The short channel effect arises due to deviation in electric field distribution throughout the channel and dip in the threshold voltage(V_T) due to channel length downscaling. The finFET design bounds short-channel effect and **the silicon film restrains off-state leakage in FET.** Its thickness should be at most one-fourth of the channel length, as reported by M.Shrivastava et al [13]. The desired Threshold Voltage (V_T) is established by: i.) smartly controlling the work function of gate by using poly-Silicon/Germanium or mid gap material. ii) material improvements by the use of high-dielectric constant gate and iii) straining silicon channel for improvement in current drive. This is reported by L.Zhang et al [14] .On advancing towards better technology node, an impact is there on performance. Many issues in the new circuit design may continue to persist. There may be new issues also.



Fig(ii) Schematic Explaining the parts of a finFET

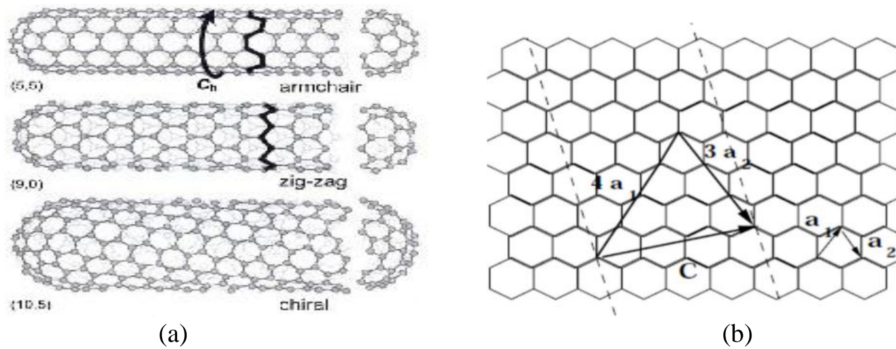
Vol. 9, Issue 2, February 2020

Table: Comparision of FinFET and MOSFET (P.C,Rajashree et a l[25])

MOSFET	FinFET
Major hurdle in prevention of current leakage.	Integrating multiple fins in FinFET reduces Leakage current
Maintaining high on current in the bulk MOSFET is a herculean task.	It is easier to obtain higher on current using multiple fins.
Higher power emission	Lesser power dissipation
It is a planer device. Channel is placed on plane of wafer .	It is a quasi-planer device. Channel is normal to the plane of thin substrate.
A single gate electrode coordinates the conduction in the channel.	Short channel effect is mitigated by employing 2 gates, which holds the fin from opposite sides.
I_{off} "The drain current when V_{gs}=0, V_{ds}=V_{dd}" becomes more pronounced on moving away from the gate.	I_{off} is regulated by increased gate capacitance due to double gates

VI.CNTFET TECHNOLOGY

CNTFET has potential to replace semiconducting channel transistors.the operation of "single-walled" carbon nanotube (SWCNT) was designed, fabricated and demonstrated at ambient conditions in 1991. CNTFETs are now considered as the probable futuristic device for nanoelectronics. Fig(iii)(a) depicts a uni-dimensional SWCNT. It can be of two types: semiconducting or metallic depending on the isotropy of carbon atoms defined by its **chirality, Ch**. It is "direction in which the graphite sheet is rolled".The designing parameter for CNT isdiameter(D_{CNT}), which controls threshold Voltage.



(a) (b)

Fig (iii) (a) Various chirality in nanotube (b) Chirality of (4,3) Carbon nanotube

In Equations (A) & (B), α is the lattice constant of Graphite (0.249 nm) and n_1, n_2 being positive-integers, on whose values the direction of wrapping of graphene sheet(chirality) to form the tube is defined. SWCNT is understood as a graphite sheet rolled about wrapping vector such that atoms at both the ends of sheet are bonded as per graphite's atomic distributions only, as evident from Fig (iii)(b), where a_1 and a_2 are unit vectors. if $n_1 = 0$, nanotube is called Zigzag. if $n_1 = n_2$, it is of Armchair type and Chiral in remaining cases. The nanotube is metallic if $n_1 - n_2 = 3i$ or $n_1 = n_2$, here i is an integer, else the tube is semiconducting. Reported by Tanisia posani et al [18] [27]

$$D_{CNT} = a\frac{\sqrt{n_1^2 + n_1.n_2 + n_2^2}}{\pi} \quad ..(A) \quad Ch = n_1 \cdot a_1 + n_2 \cdot a_2 \quad ..(B)$$

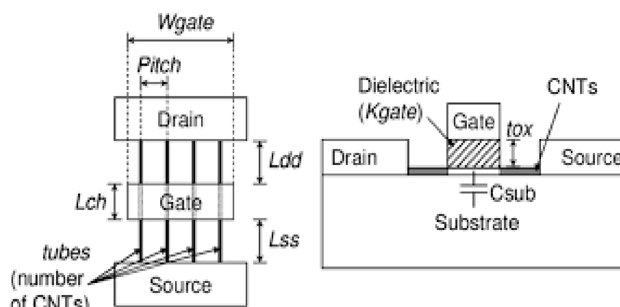


Fig.(iv): Important dimensions and labeling of CNTFETs

 DOI 10.17148/IJARCCE.2020.9214

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 9, Issue 2, February 2020

C_{sub} : "Coupling capacitance between substrate and channel"
T_{ox} : "Thickness of gate oxide dielectric"
K_{gate}: "Dielectric material between gate & CNT"
L_{dd} : "Drain side extension region length"
L_{ss} : "Part of doped carbon nanotube piercing into source"
L_{ch} : "Length of physical channel"

VII.BASIC DIGITAL ARITHEMATIC CIRCUITS

The digital arithematic applications that have been discussed in this paper are a 2 bit Multiplier and a Full adder. These circuits are implemented using all three kind of transistors using 32 nm technology.

a) 2-bit Multiplier

The multiplier plays a crucial role in arithmetic operations and in virtual signal processing programs. In fact, the leading area for the improvement of processor design is low energy of multiplier and also the low energy green circuit design is in trend. So, the urge for a low strength multiplier has accelerated. Typically, the computational performance of a DSP processor is catalyzed by the promptness of its multiplier. Therefore, performance of a processor is typically concluded from the pace and delivery voltage of its multiplier. For this reason, we should eliminate drawbacks of the multiplier using our design. Consequently, to speed up the processor, a parallel multiplier may be used in comparison to serial multiplier for better performance. If speed is not a constraint in multiplier design then partial merchandise can be summed serially to reduce the risk of layout complexity which may encourage limited power dissipation. Thus, velocity and occasional energy have a critical trade-off in designing processors. Here, the multiplier circuit which is worked upon is a 2 X 2 multiplier, which multiplies two 2-bit binary numbers and gives up to 4-bit binary product. It can be designed using four 2-input AND gates and two half-adders as specified in the gate diagram of fig.(v). The total delay in this multiplier is the delay of two half adders used.

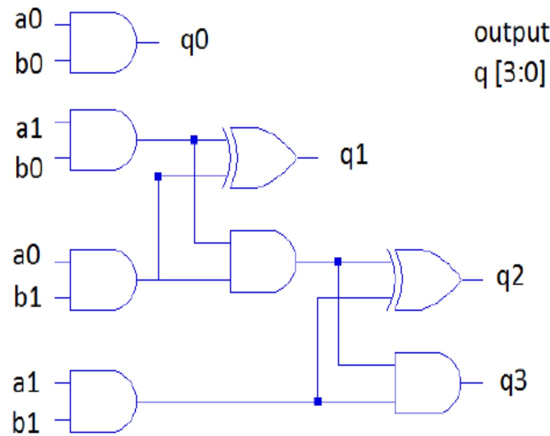


Fig.(v) AND and XOR gate based Multiplier circuit design

Comparison among Multipliers designed using different FET

The reduced short channel effects in FinFET and stronger grasp of channel by its gates improves the average energy emission-propagation delay in multiplier design. This is reported by Ajay N. Bhoj et al[23]. Replacement with CNTFET brings a ballistic transport of the charge carriers between the drain and source, resulting in increased current capacity and velocity- hence less delay which foremost requirement in multiplier is considering total delay. This is reported by Tanisia posani et al [18]

b) Full Adder

Smart logic manipulations can help in reducing the number of transistors. [17] It is encouraged to present an special logic between the carry and sum –a generation sub circuit in adder, until this does not slow down the generation of carry, which is the most critical part of this special circuit as stated previously. The original equations of full adder are in full compliance with the circuit considered in this project. The complementary FET based adder design is shown in figure (viii) and figure (ix) indicates the gate level implementation is shown in. Total 28 transistors are used in this design. This circuit is slow and consumes considerable area.

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 9, Issue 2, February 2020

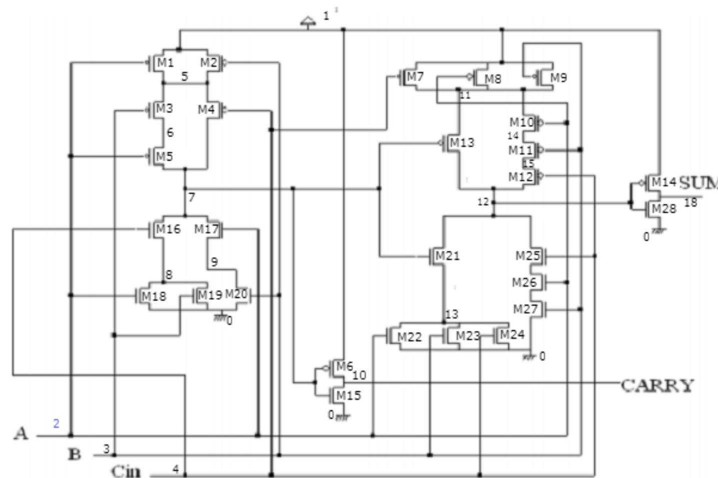


Fig.(viii) CMOS design of a full adder circuit using Twenty eight transistors

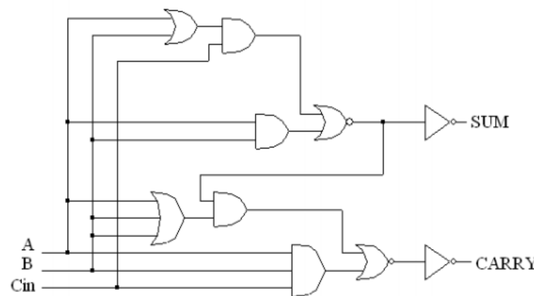


Fig (ix) Gate level circuit diagram of 28 Transistor full adder

Comparison among Adders designed using different FET

Lesser power dissipation was noticed in the CNTFET-based ternary logic circuits than the CMOS implementations. The CNTFET based full adder has lesser power dissipation than its FinFET counterpart when the supply voltage is varied by 10% because leakage power dissipation is less but dynamic is more in FinFET adder. CNTFET based full adder offers longer delay than FinFET structure this is due to its lower current driving capacity at nominal parameters. This is reported by Aminul islam et al[20]

VIII. 2X2 SRAM MEMORY

The 2 X 2 SRAM memory consists of two memory words each having a 2 bit size. Every bit is stored in a 6 transistor SRAM cell, which works in Read and Write mode [21]. Here we will perform the Write mode functionality, the prior condition for which is: Strength (W/L) of Pull-up transistor (XM3,XM4) << Strength of Access transistor(XM5,XM6)<< Strength of Pull-down transistors(XM1,XM2). For the Write operation to write '0', Word line (W) should be high, bit line (b1/b2) =1, complementary bitline (c1/c2))=0. Later when word line(W) is low, bit '0' stored in cell will be preserved at node Q[2]. This is illustrated combined by Fig.(xiii) and Fig (xiv). Here X1-X4 are the SRAM cells of fig (xiv)

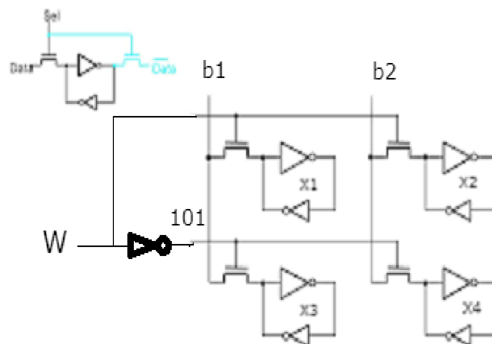


Fig (xiii) Memory unit using 2 X 2 SRAM cells

Copyright to IJARCCE
DOI 10.17148/IJARCCE.2020.9214

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 9, Issue 2, February 2020

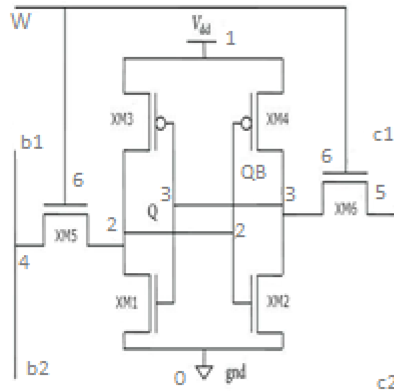


Fig.(xiv) SRAM cell with bistable latching and pass transistors

Comparison among SRAMs designed using different FET

6-Transistors based SRAM cell designed using CNTFET dissipates more power than FinFET based design. Power dissipation of a single bit SRAM cell is shown in Fig.(xiv).Performing Write operation in a cell involves charging or discharging the inverter inside the cell. Physical characteristics of the MOSFETs such as sheet resistance, drain current decide the speed of charging or discharging the cell. Different set of characteristics influence the delay encountered while reading from a cell. A carbon nanotube device shows a higher drain current than FinFET device for the same gate voltage and channel length. Therefore, a CNTFET based devices outperform the FinFET counterpart while charging the same capacitive load. On the contrary, while reading a '0' from the cell, the worst-case delay implies discharging an already charged bit-line here FinFET based cell performs better than CNTFET equivalent. This is reported by Abhijith. Bhardwaj et al[22].

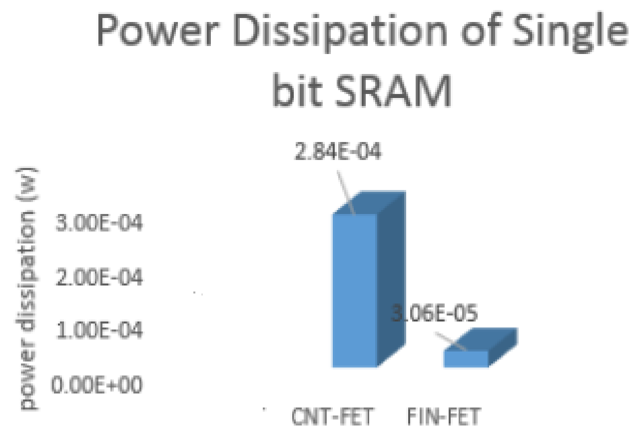


Fig (xiv): Power dissipation in both the designs

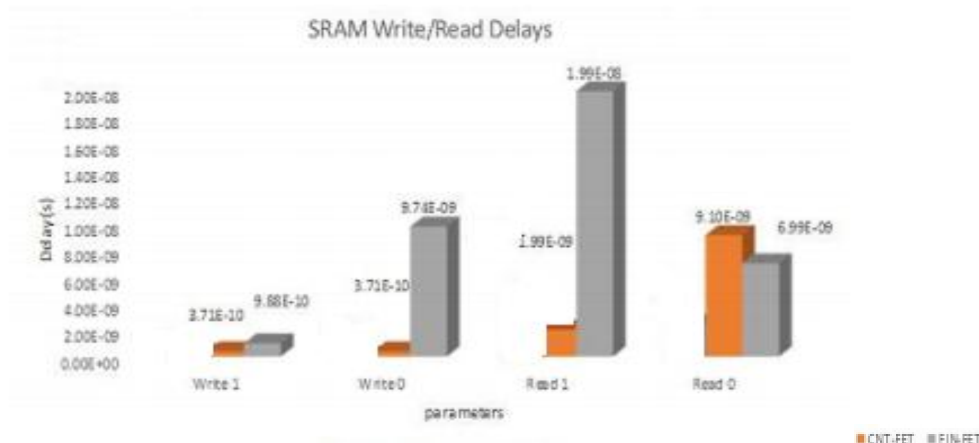


Fig (xv): Time delay in Read /Write operation of both designs

 DOI 10.17148/IJARCCE.2020.9214

VIII. CONCLUSION AND FUTURE SCOPE

Design in CNTFET is controlled by its chirality and diameter. Control of design in FinFET is granted by its back gate biasing structure which modulates its threshold voltage. Existing trade-off between FinFET, CNTFET on power delay performance, makes it difficult to predict dominant future technology below 32nm scaling. FinFET circuit simulation executes better response than the MOSFET and CNFET in terms of Gain, CMRR and Slew Rate, as reported by Satish Turkane et al[26].

REFERENCES

[1]. Deep Submicron 50nm CMOS Logic Design With FINFET P.C.Rajashree, Ancy Thomas, Rose Jaria, Jane Precilla, Alfred Kirubaraj Department Of ECE, Karunya University, Coimbatore , Tamil Nadu, India
[2]. Kaushik Roy; KiatSeng Yeo (2004). Low Voltage, Low Power VLSI Subsystems. McGraw- Hill Professional. Fig. 2.1, p. 44. ISBN 0-07-143786-X.
[3]. Kaushik Roy; KiatSeng Yeo(2004). Low Voltage, Low Power VLSI Subsystems. McGraw-Hill Professional. Fig.1.1, p.4. ISBN0-07-143786-X
[4]. DragicaVasileska; Stephen Goodnick (2006).Computational Electronics.Morgan & Claypool.p. 103.ISBN 1-59829-056-8.
[5]. "Frontier Semiconductor Paper" (PDF). Archived from the original (PDF) on February 27, 2012. Retrieved 2012-06-02.
[6]. Wai-Kai Chen (2006). The VLSI Handbook.CRC Press. Fig. 2.28, p. 2–22. ISBN 0-8493-4199-X.
[7]. E. J. Nowak, I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C.-T. Chuang, K. Bernstein, and R. Puri, “Turning silicon on its edge,” IEEE Circuits Devices Mag., vol. 20, no. 1, pp. 20–31, Jan.–Feb. 2004.
[8]. W. Zhang, J. G. Fossum, L. Mathew, and Y. Du, “Physical insights regarding design and performance of independent-gate FinFETs,” IEEE Trans. Electron Devices, vol. 52, no. 10, pp. 2198–2206, Oct. 2005.
[9]. T.-J. King, “FinFETs for nanoscale CMOS digital integrated circuits,” in Proc. Int. Conf.Computer-Aided Design, Nov. 2005, pp. 207–210.
[10]. K. Bernstein, C.-T. Chuang, R.V. Joshi, and R. Puri, “Design and CAD challenges in sub-90 nm CMOS technologies,” in Proc. Int. Conf. Computer-Aided Design, Nov. 2003, pp. 129–136.
[11]. P. Mishra and N.K. Jha, “Low-power FinFET circuit synthesis using surface orientationoptimization,” in Proc. Design Automation and Test in Europe, Mar. 2010, pp. 311
[12]. A.Muttreja, N.Agarwal, & N.K.Jha, “CMOS logic design with independent gate FinFETs,” in Proc. Int. Conf. Comp Design, 2007, pp.560–567
[13]. M. Shrivastava, M. Agrawal, J. Aghassi, H. Gossner, W. Molzer,T. Schulz, and V. R. Rao, “On the thermal failure in nanoscale devices: Insight towards heat transport including critical BEOL and design guidelines for robust thermal management & EOS/ESD reliability,” in Proc.Int. Reliab. Phys. Symp., pp. 3F.3.1–3F.3.5, 2011.
[14]. L. Zhang, J. He, F. Liu, J. Zhang, Y. Song, "A Unified charge-based model for symmetric DG MOSFETs Valid for both heavily doped body and undoped Channel," International conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2008), June 2 1- 23 pp.367-372, Poland, 2010.
[15]. Lin, Yu-Ming; Tsang, James C; Freitag, Marcus; Avouris, Phaedon (2007). "Impact of oxide substrate on electrical and optical properties of carbon nanotube devices
[16]. Ravi Kumar. K. I, Vijayalaxmi. C. Kalal, Rajani. H. P, Dr. S. Y.Kulkarni “Design and Verification of Low Power 64bit SRAM System using 8T SRAM:Back-End Approach”
[17]. http://shodhganga.inflibnet.ac.in/bitstream/10603/6521/9/09_chapter%204.pdf
[18]. Application of gm/ID Methodology for Analog Design Using Nanometer-Scale Devices.Tanísia Possani1 , Luiz Roberto Pavanato2 , Luiz Antônio da Silva Jr.3 , Alessandro Girardi4 Computer Architecture and Microelectronics Group, Federal University of Pampa – Campus Alegrete
[19]. Design Of Ternary Logic Arithmatic Circuits Using CNTFET
[20]. Energy efficient and process tolerant full adder in Technologies beyond CMOS.ACEEE Int. J on communicationVol. 02, No 02,July 2011
[21]. Fundamentals of digital circuits by A.Anand Kumar
[22]. Design and Performance Comparison of finFET, CNFET and GNRFET based 6T SRAM. International Journal of Science and Research (IJSR) ISSN (Online): 2319-7064
[23]. Ajay N. Bhoj and Niraj K. Jha, IEEE, 2013, “Design of Logic Gates and Flip-Flops in High-performance FinFet Technology” [24] Basic VLSI Design by Douglas A.Pucknell, Kamran Eshraghian
[24]. Deep Submicron 50nm CMOS Logic Design With FinFET P.C..Rajashree
[25]. Performance investigation of emerging nano devices for low power analog circuits.DOI: 10.1109/ICACDOT.2016.7877681
[26]. S.B.Sinnot & R.Andreys(2001) .”The Carbon Nanotubes : Synthesis, Properties and Applications” ,Critical reviews in Solid states and material science.