IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 9, Issue 7, July 2020

Simulation and Analysis of 3D Spiral Inductor on High Insulating Substrate

Kunal Banthotra[1], Ritika[2]

M. Tech Student, Dept. of Electronics & Communication Engineering, Sri SAI CET, Pathankot, India[1]

Assistant Professor, Dept. of Electronics & Communication Engineering, Sri SAI CET, Pathankot, India[2]

Abstract: Spiral inductors on semiconductor/insulator substrate play a crucial role in Radio Frequency Integrated Circuits (RFICs). For high frequency system circuitry, these components are realized using bond-wires or planar spirals. The Quality Factors (Q) of bond wires is higher than on-chip spirals, their use is constrained by the limited range of realizable inductances. The research presented here provides insight into some of the most pressing issues currently being addressed by the research community, and provides guidelines for designing these evolving heterogeneous Three Dimension (3D) systems. 3D spiral inductor integration is an evolving technology that will enhance the semiconductor roadmap for several generations. This dissertation provides insight into the 3-D inductor IC design process, with the goal of strengthening the design capabilities for 3-D integrated circuits and systems.

Keywords: Inductor, SiO_2, Silicon, Glass, PEC.

I. INTRODUCTION

Inductors and transformers are the fundamental building blocks of electronics, and they are found in every electronic device. Micro inductors and transformers are used in the field of radio frequency microelectromechanical systems (RF MEMS), micro actuators, and biosensors. Micro-inductors for power electronics is an emerging application in which inductors are used as energy storage elements for Switched Mode Power Supplies (SMPS). Miniaturization of SMPS has become the main focus for developing future generation power supplies known as Power Supply in package (Pwr SiP) and Power Supply on Chip (Pwr SoC). The Pwr SoC vision is to integrate all power electronics components on one chip. Higher integration lowers the cost and increases both efficiency and power density [1-8]. Therefore, one of the most important inductor requirements for Pwr SoC technology is the CMOS compatibility for on-chip integration. Other requirements are compact physical dimensions, a high-current capacity, and a high-quality factor for high efficiency. Switching at very high frequencies ranging from 30–300 MHz is one route toward Pwr SiP and Pwr SoC. In the VHF range, inductors with an air core or non-magnetic core are preferred, as suitable magnetic materials working at these frequencies are limited and the core implementation is very challenging [9-11].

The fundamental monolithic inductor is usually implemented as a spiral trace deposited on the passivation layer over a silicon substrate [12], as shown in Figure 1. The connection from the innermost turn can be taken out as a lead by an underpass or an air bridge. The design parameters are Number of turns (n), metal Width (w), Metal Spacing (s), Diameter of Outermost turn (do), Diameter of Innermost turn (di) and Arithmetic mean of inner and outer diameter (davg).

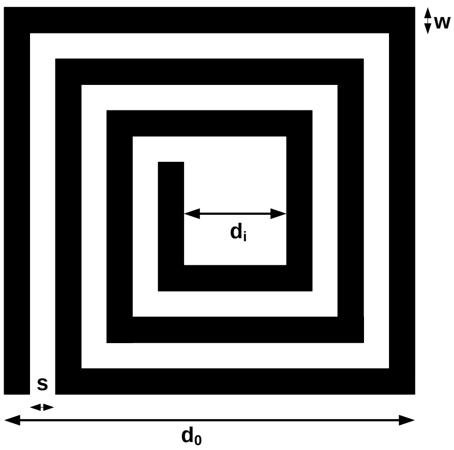

Fig. 1 Planar square spiral inductor.

The inductance [1] of the square planar coil is given by the equation.

$$L = \frac{9.375\mu_0 n^2 d_{avg}^2}{11d_0 - 7d_{avg}}$$

where μ_0 is the permeability of free space with a value of $4\pi*10^{-7}$ H/m.

II. SIMULATION PROCESS FLOW

The research work is formulated to simulate surficial spiral inductor and through substrate via based inductor. The proposed research simulation process flow chart is shown in Fig. 2.

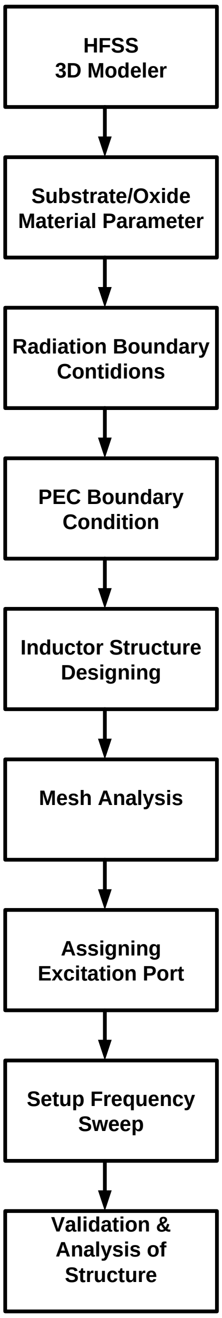

Fig. 2 Simulation process flow steps.

HFSS 3D modeler simulation tool is selected and active for the process. The first step is to select the appropriate substrate and oxide material for the designing of inductor. RF radiation is the main parameter which needed to be studied. Appropriate radiation boundary conditions are given to the design. The spiral of the inductors are made up of perfect

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 9, Issue 7, July 2020

electric conductor, hence PEC boundary conditions must be given to the coil structure. Thus the complete geometry of the structure is coupled together. Meshing of the inductor structure is carried out. The mesh parameter of the structure will depend upon the system computing power. Next step is to assign the excitation port to the inductor. For the design lumped port excitation technique is taken. Lastly the frequency sweep is given to the simulation process; further the structure is validated and analyzed in frequency domain. S parameters, impedance, and quality factor the inductor will be optimized for RF applications.

III. RESULTS AND DISCUSSION

The research work is carried out to simulate and analyse 3D spiral inductor. Highly insulating glass substrate is utilized having relative permittivity (ε) of 5.5 is used for simulation of 3D spiral inductor having 2.5 turn, width of 15μm shown in Fig. 3. Frequency domain analysis of the designed spiral inductor was carried out in the frequency range of 0-20 GHz. S-parameters i.e. S_{11} & S_{21} were computed for the frequency 0-20 GHz shown in Fig. 4. It is observed form the graph that minimum insertion loss is observed at 19.30 GHz.

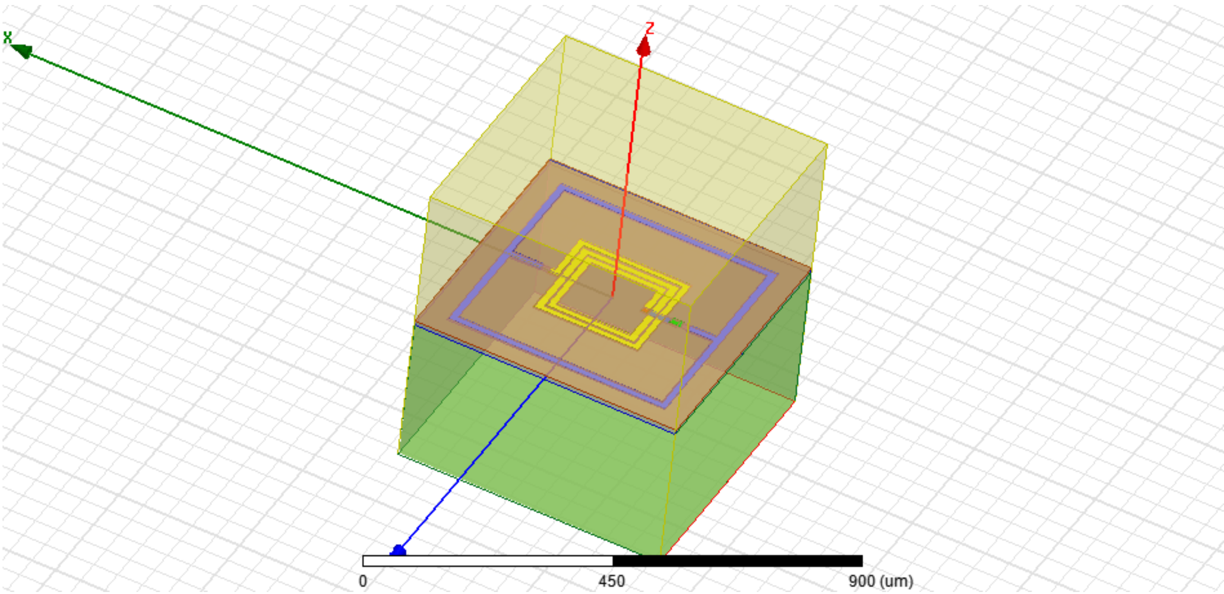

Fig. 3 Designed geometry of spiral inductor.

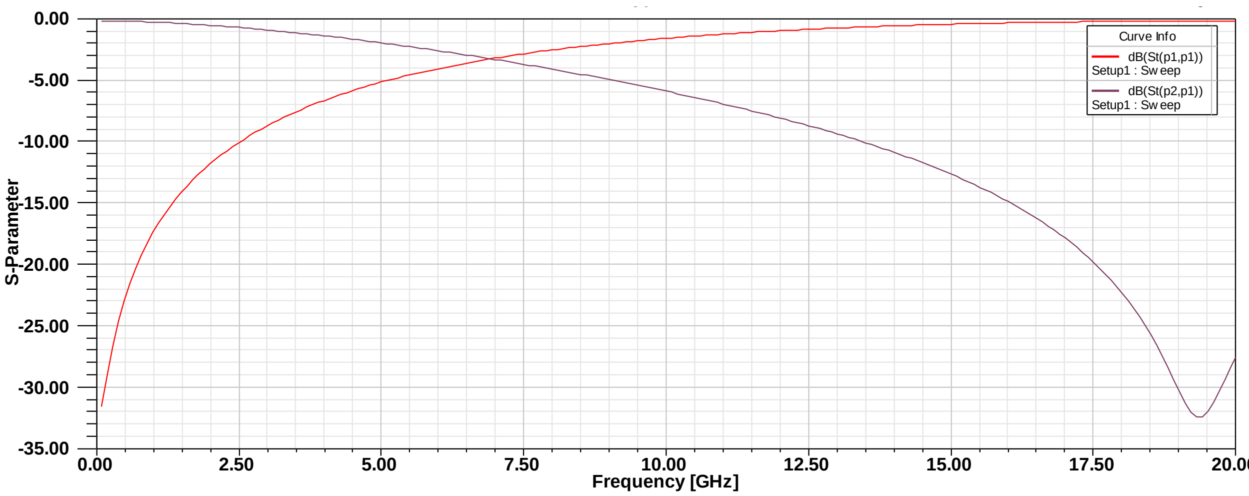

Fig. 4 S-parameter (insertion loss) of designed spiral inductor frequency ranging from 0-20 GHz.

Figure 5 shows the inductance of the designed 3D spiral inductor for the frequency ranging from 0-20 GHz. It is observed from the graph that maximum inductance of 1.30μH is obtained at 16.20 GHz. Also, Q-factor is computed for the designed spiral inductor shown in Fig. 6. Both input port Q-factor i.e. Q_{11} and output port Q-factor i.e. Q_{22} of the inductor are computed and plotted.

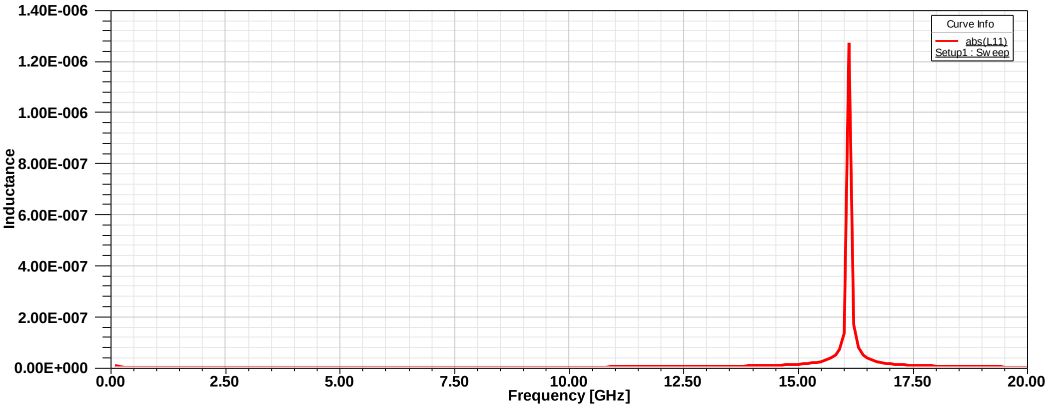

Fig. 5 Inductance of designed spiral inductor for frequency ranging from 0-20 GHz

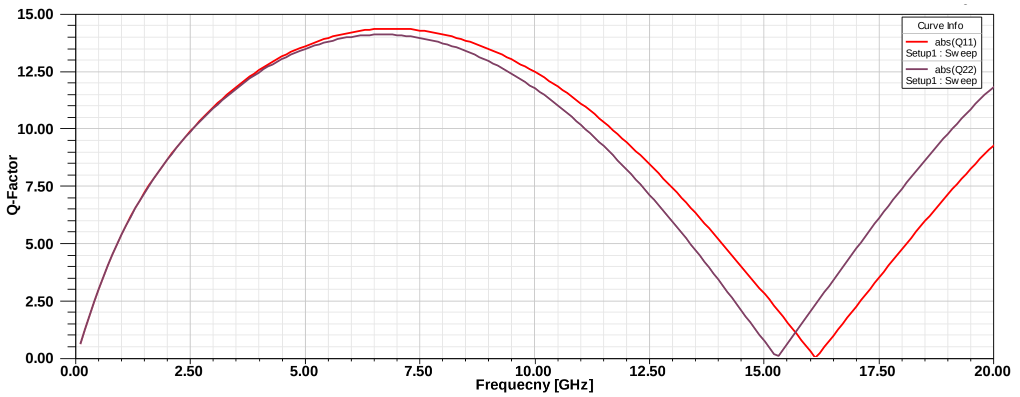

Fig. 6 Q-factor for designed inductor for frequency ranging from 0-20 GHz

IV. CONCLUSION

In this research paper, rectangular spiral inductor is designed and simulated using FEM based platform. Spiral inductors are critical for filtering and tuning purposes in telecommunication field. It is important that the inductor model predict the Q-factor of the inductor, and the resonance accurately. The simulated spiral inductor shows 1.30µH inductance at frequency at 16.20 GHz. The modelled device shows high Q-factor of 14.5. The result shows advantage of high insulating substrate over semiconductor substrate.

REFERENCES

[1] J. Bardeen and W. H. Brattain, “The Transistor, a Semiconductor Triode,” Physical Review, Vol. 74, No. 2, pp. 230 - 231, July 1948.
[2] G. E. Moore, “Progress in Digital Integrated Electronics,” Understanding Moore’s Law: Four Decades of Innovation, Chapter 6, pp. 61–66, 2006.
[3] L. Xue, C. Liu, H.-S. Kim, S. Kim, and S. Tiwari, “Three-Dimensional Integration: Technology, Use, and Issues for Mixed-Signal Applications,” IEEE Transactions On Electron Devices, Vol. 50, No. 3, pp. 601-608, March 2003.
[4] W. R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. M. Sule, M. Steer, and P. D. Franzon, “Demystifying 3D ICs: The Pros and Cons of Going Vertical,” IEEE Design and Test of Computers, Vol. 22, No. 6, pp. 498–510, 2005.
[5] C. R. King, D. Sekar, M. S. Bakir, B. Dang, J. Pikarsky, and J. D. Meindl, “3D Stacking of Chips with Electrical and Microfluidic I/O Interconnects,” Proceedings of the IEEE Electronic Components and Technology Conference, pp. 1–7, May 2008.
[6] T. Zhang, R. Micheloni, G. Zhang, Z. R. Huang, and J. J.-Q. Lu, “3-D Data Storage, Power Delivery, and RF/Optical Transceiver—Case Studies of 3-D Integration from System Design Perspectives,” Proceedings of the IEEE, Vol. 97, No. 1, pp. 161–174, January 2009.
[7] E. Bonizzoni, F. Borghetti, P. Malcovati, and F. Maloberti, “A 200-mA, 93% Peak Power Efficiency, Single-Inductor, Dual-Output DCDC Buck Converter,” Analog Integrated Circuits and Signal Processing, Vol. 62, No. 2, pp. 121–129, June 2009.
[8] K. Ishida, K. Takemura, K. Baba, M. Takamiya, and T. Sakurai, “3D Stacked Buck Converter with 15 µm Thick Spiral Inductor on Silicon Interposer for Fine-Grain Power-Supply Voltage Control in SiP’s,” Proceedings of the IEEE International 3-D Systems Integration Conference, pp. 1-4, November 2010.
[9] M.-J. Wang, C.-Y. Hung, C.-L. Kao, P.-N. Lee, C.-H. Chen, C.-P. Hung, and H.-M. Tong, “TSV Technology for 2.5D IC Solution,” Proceedings of the IEEE Electronic Components and Technology Conference, pp. 284-288, May 2012.
[10] I. Savidis and E. G. Friedman, “Electrical Modeling and Characterization of 3-D Vias,” Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 784–787, May 2008.
[11] M. S. Kim, M. R. Pulugurtha, V. Sundaram, R. R. Tummala, and H. Yun, “Ultrathin High-Q 2-D and 3-D RF Inductors in Glass Packages”, IEEE Transactions On Components, Packaging And Manufacturing Technology, 2018.
[12] S. Musunuri and P. L. Chapman, "Fabrication and characterization of PDMA inductors," in Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, 2004, pp. 4460-4466 Vol.6.