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Effect of Ambient Temperature on Transfer Characteristics of Nanowire FET

Sabhya Kandley[1] & Harish Dogra[2]

M. Tech Student, Department of ECE, Sri Sai College of Engineering & Technology, Badhani, India[1]

Assistant Professor, Department of ECE, Sri Sai College of Engineering & Technology, Badhani, India[2]

Abstract: The purpose of this research work is to describe the modeling of the performance of 2D material such as (WSe_2, $MoSe_2$, etc.,) nanowire FETs and to study their performance as parameter of the transistor's structure variation like diameter, gate dielectric thickness, and gate dielectric constant. Simulations of ballistic transport in the calculation of the current-voltage (I-V) characteristics for nanoscale single gate FETs. FET channel lengths are getting smaller and high-mobility channel materials are being used, near-ballistic models of FET device physics operation is being realized.

Keywords: Nanowire, FET, Semiconductor, Temperature.

I. INTRODUCTION

Complementary metal–oxide–semiconductor (CMOS) transistor evolution has been largely enabled by the continual reduction in the metal-oxide semiconductor field-effect transistor (MOSFET) size, particularly the gate length, typically L_g, through the application of Moore's Law. One important electronic property of FETs is transconductance (g_m), the ratio of the output current to the input voltage, which is inversely proportional to the gate length. Transistor speed is governing by the cutoff frequency parameter

$$f_T = \frac{g_m}{2\pi C_g} \approx \frac{1}{L_g^2}$$

where C_g, is the gate capacitance per unit area. Thus, as the gate length gets smaller, the MOSFET gets faster while providing higher gain. The challenges lie, however, with the limits to how small the RC time constant product can become (due to parasitic effects) as the gate length of the devices reduced [3] as well as the physical challenges posed by frequently fabricating smaller MOSFETs following the downscaling development and maintaining their normal functioning overcoming changes in the physics of device operation, scaling restraint factors, and short channel effects [4-6]. Nanowires are nanoscale structures which are frequently single crystal materials and are typically cylindrical in shape. They can be formed in a variety of materials including metals and insulators, but are most frequently fabricated using semiconducting materials. Since semiconductors are used in transistors, semiconducting nanowires are of the most importance. They have engrossed attention not only because of their extremely small size, but because their size causes new physics (quantum effects) to apply, that can cause changes in material properties. Nanowire FETs are important because they are potentially useful in low-power applications, have high packing densities, maintain high gate sensitivity, are capable of individual or bulk (arrayed)fabrication, are scalable, and have recently been investigated for ballistic carrier transport behavior for potential high-performance electronic devices [7]. Nanowire FETs even allow for bandgap engineering of the FET channel allowing designers to maximize device performance [8].There are several factors to consider when optimizing a FET device. Some of these include: low threshold voltage, high carrier mobility/speed, low leakage current, low power operation, low drive voltage operation, low series resistance, high transconductance (gate sensitivity), and good subthreshold characteristics.

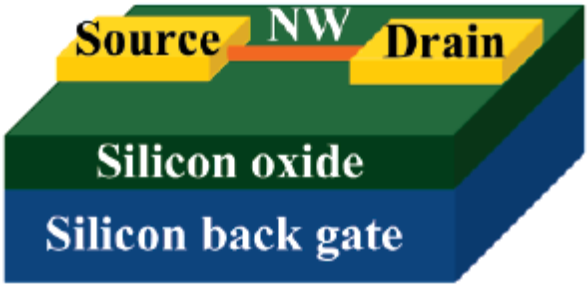

Fig. 1 Topology of nanowire FET.

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According to the theory of ballistic nanotransistors [6], a non-equilibrium mobile charge is induced between the source and the drain if electric field is applied. The positive charge densities in source, negative charge densities in drain and equilibrium charge densities are related to the density of states and Fermi-Dirac probability distribution. The induced drain current is given by

$$I_{DS} = \frac{2qkT}{\pi h}\left[F_0\left(\frac{U_{SF}}{kT}\right) - F_0\left(\frac{U_{DF}}{kT}\right)\right]$$

Here, F_0 is the Fermi integral of order 0, k is the Boltzmann constant, ħ is the reduced Planck constant, T is the temperature, U_{SF} and U_{DF} are the potentials induced by terminal voltages at source and drain respectively as defined by

$$U_{SF} = E_F - qV_{SC}$$

$$U_{DF} = E_F - qV_{SC} - qV_{DS}$$

Where EF is the Fermi level, VSC is the self-consistent potential and VDS is the induced voltage between drain and source [9-10].

II. SIMULATION PROCESS FLOW

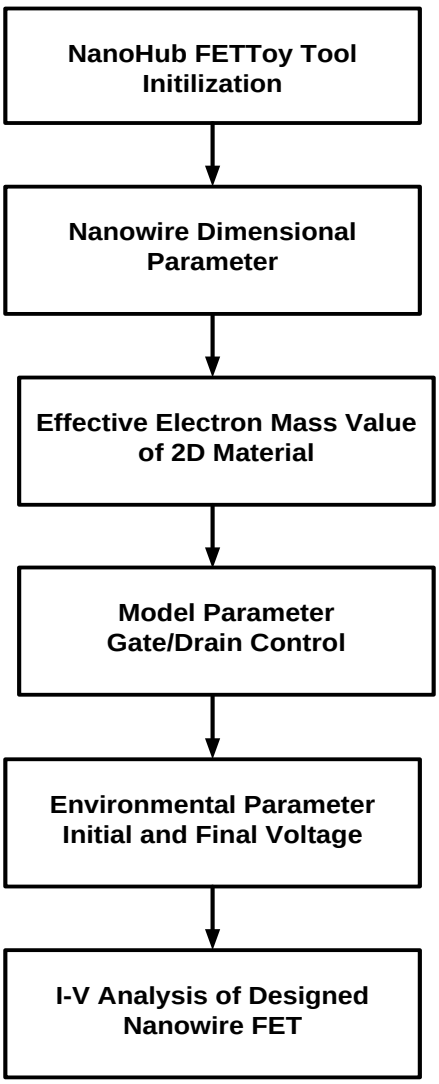

Fig.2 Simulation process flow.

Simulation is carried out to observe the effect of ambient temperature on nanowires-based FET. In the process flow ambient temperature from 350K to 600K with step size of 50K is varied for the simulation keeping 10nm diameter of the device and SiO_2 as dielectric material. The simulation process was carried out and electrical characteristics such as output

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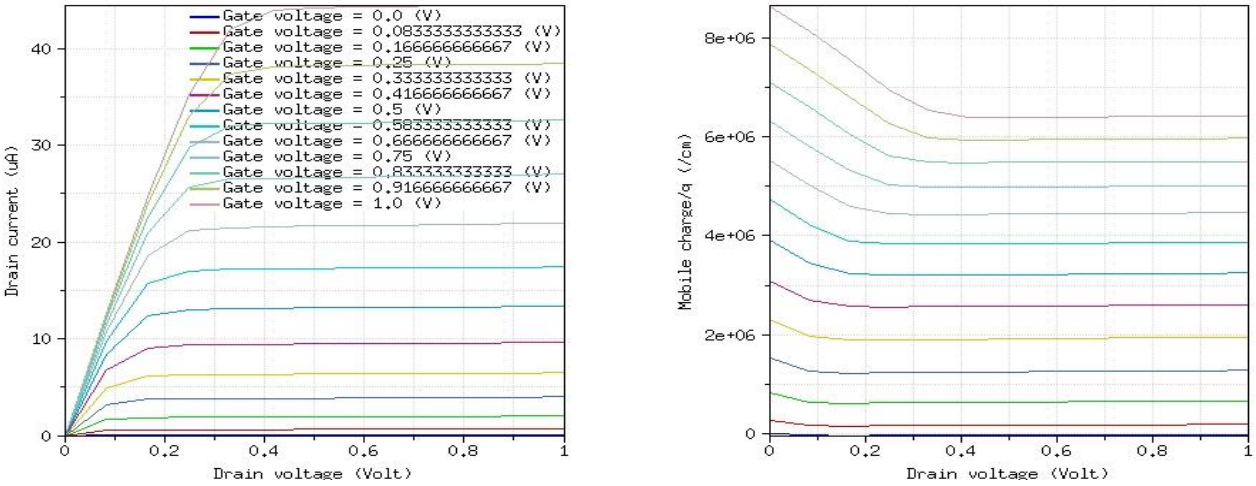
transfers characteristics, charge mobility, quantum capacitance, and transconductance of device were observed for various ambient temperature. The simulation process is shown in Fig. 2.

III. RESULTS AND DISCUSSION

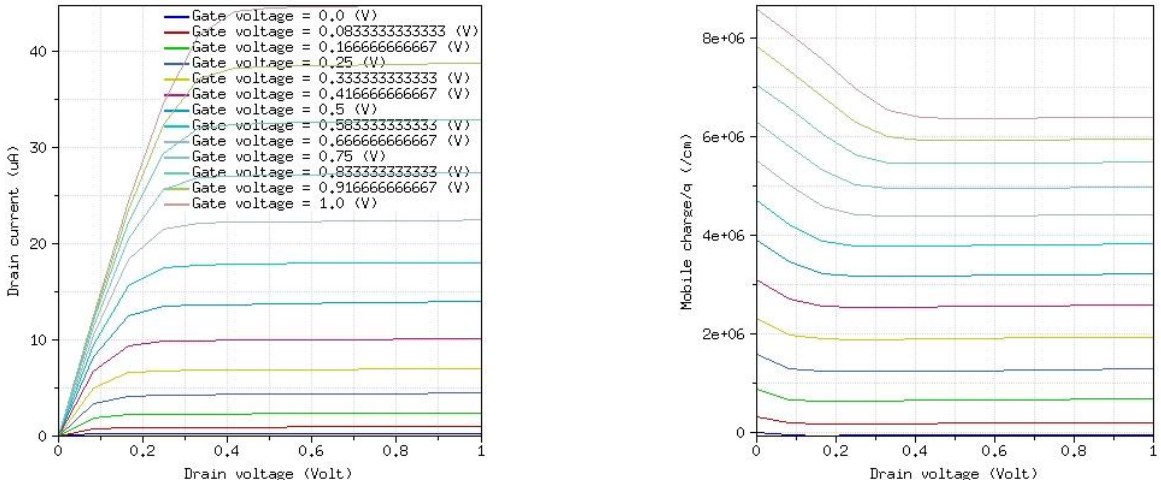
The simulated characteristics of WSe_2 nanowire based FET at 350K ambient temperature is show in Fig. 3. The maximum drain current I_d obtained with V_g is ~48µA. The charge mobility i.e. mobile charge/cm is ~$6.5x10^6$. Maximum value of quantum capacitance obtained for simulated device is ~$4.5x10^{-12}$ F. The transconductance curve shows the saturation after 0.5 V of drain voltage.



(a) (b)

Fig. 3 Simulated characteristics of 10 nm WSe_2 nanowire based FET at 350K ambient temperature (a) I_d vs V_g characteristics for various gate voltage (b) mobility of charge carrier with various gate voltage.

The simulated characteristics of WSe_2 nanowire based FET at 400K ambient temperature is show in Fig. 4. The maximum drain current I_d obtained with V_g is ~50µA. The charge mobility i.e. mobile charge/cm is ~$6.5x10^6$. Maximum value of quantum capacitance obtained for simulated device is ~$4.0x10^{-12}$ F. The transconductance curve shows the saturation after 0.5 V of drain voltage.



(a) (b)

Fig. 4. Simulated characteristics of 10 nm WSe2 nanowire based FET at 400K ambient temperature (a) Id vs Vg characteristics for various gate voltage (b) mobility of charge carrier with various gate voltage.

The simulated characteristics of WSe_2 nanowire based FET at 450K ambient temperature is show in Fig. 5. The maximum drain current I_d obtained with V_g is ~50µA. The charge mobility i.e. mobile charge/cm is ~$6.5x10^6$. Maximum value of quantum capacitance obtained for simulated device is ~$3.8x10^{-12}$ F. The transconductance curve shows the saturation after 0.5 V of drain voltage.

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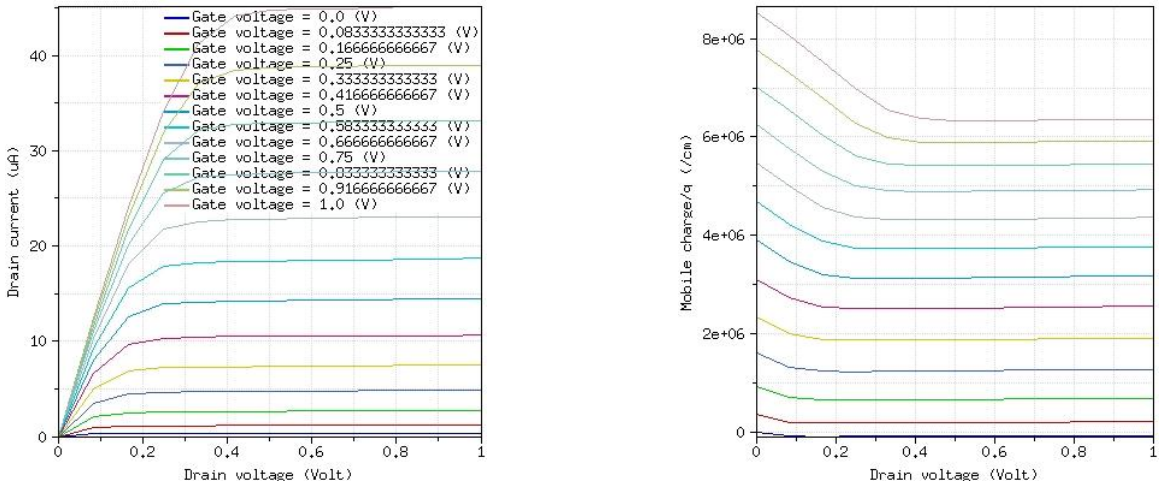
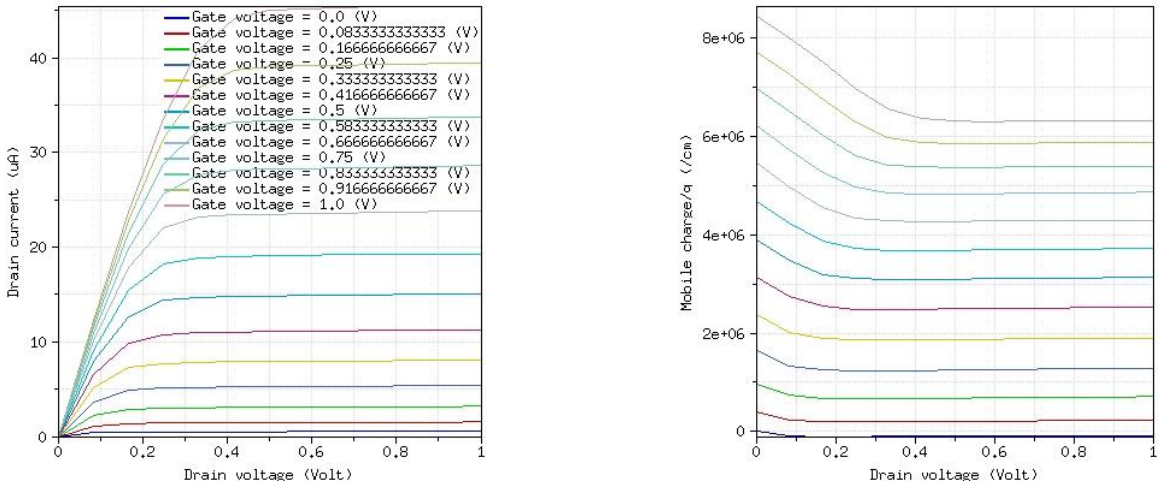


(a) (b)

Fig. 5 Simulated characteristics of 10 nm WSe2 nanowire based FET at 450K ambient temperature (a) Id vs Vg characteristics for various gate voltage (b) mobility of charge carrier with various gate voltage.

The simulated characteristics of WSe_2 nanowire based FET at 500K ambient temperature is show in Fig. 6. The maximum drain current I_d obtained with V_g is ~51µA. The charge mobility i.e. mobile charge/cm is ~$6.5x10^6$. Maximum value of quantum capacitance obtained for simulated device is ~$3.6x10^{-12}$ F. The transconductance curve shows the saturation after 0.5 V of drain voltage.



(a) (b)

Fig. 6 Simulated characteristics of 10 nm WSe_2 nanowire based FET at 500K ambient temperature (a) I_d vs V_g characteristics for various gate voltage (b) mobility of charge carrier with various gate voltage.

TABLE I SIMULATED MAXIMUM VALUE OF PARAMETERS.

Temperature (K)	I_d (µA)	Mobility (charge/cm)	Quantum Capacitance (F)
350	44.5	6.41 x 10^6	4.46 x 10^{-12}
400	44.8	6.38 x 10^6	4.18 x 10^{-12}
450	45.1	6.35 x 10^6	3.94 x 10^{-12}
500	45.5	6.32 x 10^6	3.74 x 10^{-12}
550	46.0	6.27 x 10^6	3.56 x 10^{-12}
600	46.5	6.22 x 10^6	3.40 x 10^{-12}

IV. CONCLUSION

Simulations were carried out to calculate ballistic I-V characteristics for nanowire MOSFETs based on the top-of-the-barrier approach. The models a cylindrical-shaped wire with source and drain contacts at the ends and agate that wraps around the middle. It is observed from the results that WSe_2 nanowire based FET device shows better performance as

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compared to Si nanowire based FET device. Improved transfer characteristic is seen in case of WSe_2 nanowire based FET device. It is observed from the result that with rise in ambient temperature the transfer current increases gradually where as mobility of majority carrier and quantum capacitance decreases.

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