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Design and FPGA Implementation of Binary Tree Different Node Topology Network on Chip

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Abstract: With the expansion in the interest for superior and fast VLSI frameworks, such as network Processors In networking or SOCs in communication and computing has shifted the focus from traditional performance Parameters towards the number of chips, LUT's etc. and frequency consumption. Paired tree topology s the one of the topology for system on chip plan in this proposition we have effectively structure the equipment chip for bunch size 2, 4, 8 and 16 separately. The capacity on recreation is done in Modalism programming the outcomes are checked on Spartan 3EFPGA. Our binary chip is optimization in terms of hardware parameters such as LUTand flip- flop. The system supports high frequency.

Keywords: VLSI, SOCs, FPGA, LUTs.

I. INTRODUCTION

In the ongoing couple of years, we have seen the IT business progressively grasp another worldview called System on a Chip (SOC) plan. This is a plan strategy wherein consistently unique framework parts, as ASICs, I/O gadgets, universally useful processors and DSP processors, are acknowledged on a solitary silicon chip. Advances in high-thickness creation, just as cost viability of the subsequent frameworks, have contributed a lot to this move. Accordingly, in any case, the plan of custom equipment, inserted processors and programming that go into them have turned out to be all around firmly coupled. Change in the usage of the parts influences the plan of different segments and, thusly, the exhibition of the framework. Thus, the conventional shrewdness of structuring and building up every segment as a different substance is never again proficient. A progressively coordinated methodology is required. This has prompted the idea of co-structure and co-check in equipment and programming.

Today, many incorporated circuits contain a few processor centers, recollections, equipment centers and simple parts coordinated on a similar chip. Such Systems are progressively utilized in high volume and top of the line applications, running from sight and sound and resistance applications. As the quantity of centers joined on a SoC increments with innovation scaling, 2-D chip creation innovation is dealing with part of difficulties in utilizing the exponentially mounting number of transistors. As the measure of transistors and the kick the bucket greatness of the chip developing, the length of the interconnects likewise degree. With littler element estimates, the exhibition of the transistors has expanded significantly. In any case, the demonstration advancement of interconnects has not kept skip with that of the transistors. With falling geometries, the wire pitch and cross segment likewise cut, in this manner expanding the RC remain of the wires. This combined with developing interconnect length insights to stretched timing looks out for worldwide wires. For instance, in advancements, lengthy worldwide wires could need up to 10 clock cycles for traversal. Another huge influence of improved lengths and RC qualities is that the power encouraging of worldwide interconnects become major, along these lines acting a major test for framework fashioners.

System on-a-Chip is a way to deal with plan the correspondence sub-framework between IP centers or framework on chip. System on Chip applies organizing hypothesis and technique to on chip correspondence and brings remarkable improvement over ordinary and interconnections transport. System on chip develops the adaptability of SoCs, and the power productivity of troublesome SoCs connected to different plans.. It was the economy that drove the "executioner small scale" and slowed down imaginative super PC structure in the mid-1990s. The economy is driving GPUs to get quicker and compelling a unification of GPU/CPU models today. It will be the economy that will drive vitality efficient registering and monstrous parallelism. This is mostly because of various essential physical constraints on consecutive handling, for example, the speed of light and the dispersal of warmth.

Despite the fact that the writing contains a few scientific categorizations of parallelism, one can discuss two major sorts of parallelism accessible for misuse in programming: information parallelism and assignment parallelism.

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The previous executes a similar guidance on a moderately enormous informational collection. For instance, component shrewd expansion of two vectors has spaces of information parallelism. Errand parallelism, then again, is accomplished by breaking down the application into various free undertakings that can be executed as discrete techniques. A multi-strung web server master vides a genuine model for assignment parallelism, where numerous solicitations of different sorts are taken care of in parallel. As a general rule, most applications utilize a mix of information and assignment parallelism, and hence, fall some place amidst the range. In spite of the fact that it is conceivable to revamp a few applications that were recently written in the information parallel design in an errand parallel style, and the other way around, this isn't constantly conceivable. By and large, one can talk about a connection between the present parallel structures and sorts of accessible parallelism. For instance, greatly multithreaded designs are superior to others when managing a lot of errand parallelism. On the opposite side, GPUs exceed expectations in information parallel calculations. Be that as it may, as most calculations can't be hard classified as having exclusively task parallelism or exclusively information parallelism, an extreme direct mapping of uses to models is probably not going to rise.

II. BINARY TREE TOPOLOGY:

Network on chip (NoC) is the network technology for interconnecting high-performance computers in parallel. The NoCarchitecture follows the topological structure. The NoC uses the wired link to interconnect and is shared by many signals. The links of the NoC work simultaneously with respect to different data packets' size, and high level of pipelined and parallel processing is required to execute the operations in faster way. The complexity of the integrated electronics systems and ICs is increasing day by day. NoC is the solution over complex integrated system that can provide the better performance and throughput. NoCprovides scalable architecture and good performance in comparison with tradition technique used for communication architecture such as shared bus, bridges, and segmented bus, point to point wires. The routing and addressing of the NOC can be done in such a way that it can support high level of parallelism, and multiprocessor system on chip (MPSoC) interconnections can be configured in scalable design.

The methods of networking and on-chip communication techniques are used to configure the specific NoC architecture. The topology of NoC defines the way of connecting the nodes. It can affect the NoC latency and bandwidth requirements. The global interconnection structure helps in reduction of signal latency and wiring of the design. There are many topologies existing for NoC design such as mesh, tree, ring, butterfly, and hybrid topologies. The selection of topology is based on applications and system requirements. The 2D mesh topology is simple and regular in nature and most applicable because of small length of wire among nodes. The NoC communication architecture is following the concept of message transfer among the transmitting and receiving end as response message. The transmitting node transmits the message in the form of packets. The packet data is small and uses small channels. That is why the resource utilization in packet data is small. The data packet is consisting of three main parts: header section, payload section, and tail bit. The information of the destination nodes is addressed by the header and creates the links between source and destination nodes, based on routing mechanism and addressing. The payload section is having actual data required to transmit from sender to receiver node. The tail bit indicates that the packet transmission is ended. The important and fundamental concern in the NoC is fault tolerance. The system failure during runtime and IC defects during the manufacturing and fabrication are inevitable and impossible to remove from the system. The packet data transmission improves the fault tolerance, and NoC follows the fault-tolerant routing mechanism to control the packet Transmission and avoids the faulty or defective areas instead of the whole system Considered as faulty.

Fat trees are the roundabout topology arrange by Charles E. Lesierson recommended in 1985 in which the switches are associated in start to finish as tree. The tree structure has the progression in its plan that the connections structure the through and through and base to top are equivalent. The structure depends on the parent (root) and tyke, sub Childs relationship as kin. The reason the connections are getting to be "fatter" towards the top side of the tree. The switch in the root heading is having a lot number of connections in contrast with the switch in the base side. The fat tree structure having 16 hubs in base is appeared in fig 4.12. In the stage first, the switch has two branches '1' and '0'. Two subunits (00, 01) are joined to the branch '0' and two sub units (10, 11) to branch '1'. In this four switches in stage two are tended to as"00", "01", "10" and "11".

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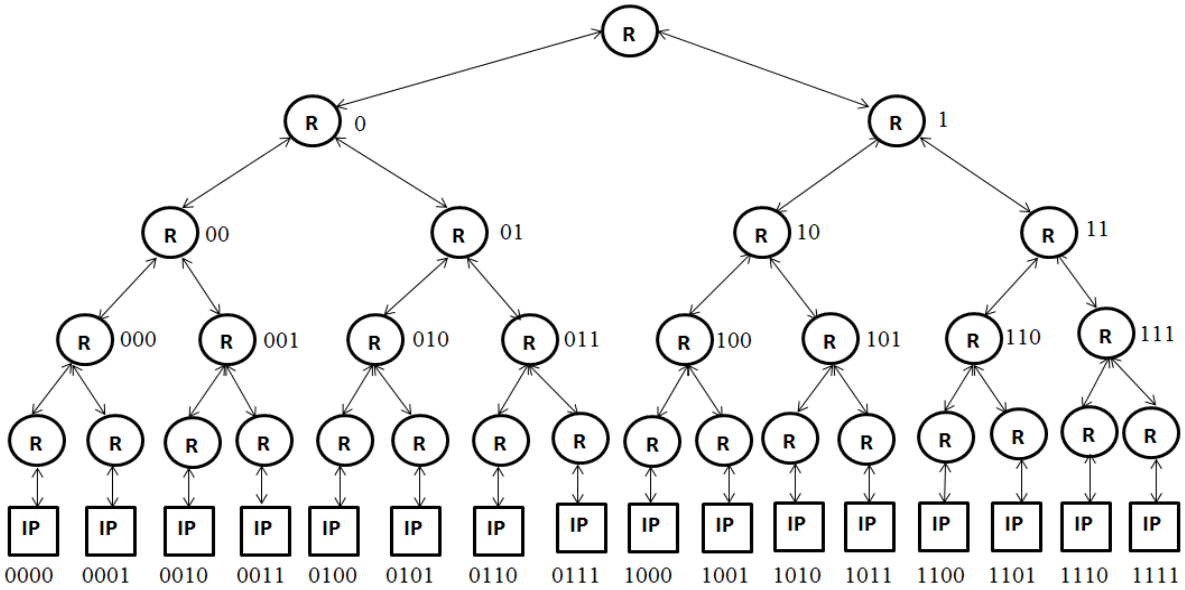

Figure 1: Structured tree NoC for 16 nodes

Similarly, every switch s related with third stage switches which are "000", "001", "010", "011", "100", "101", "110" and "111". In the last stage the sub switches are related with their IPs. The correspondence for the 16 hubs structure parent to kid hubs or switches is conceivable in circuitous manner in a similar tree the hubs are recognized as "0000" node0, "0001" node1, "0010" node2, "0011" node3, "0100 node4", "0101 node5", "0110 node6", "0111 node7", "1000 node8", "1001 node9", "1010 node10", "1011 node11", "1100 node12", "1101 node13", "1110 node14" and "1111 node15".

III.FPGA APPLICATIONS:

FPGAs have increased fast development over the previous decade since they are helpful for a wide scope of utilizations. Explicit utilization of a FPGA incorporates advanced sign handling, bioinformatics, gadget controllers, programming characterized radio, arbitrary rationale, ASIC prototyping, medicinal imaging, PC equipment copying, coordinating different SPLDs, voice acknowledgment, cryptography, separating and correspondence encoding and some more. More often than not, FPGAs are kept for specific vertical applications where the generation volume is little. For these low-volume applications, the top organizations pay in equipment costs per unit. Today, the new presentation elements and cost have expanded the scope of reasonable applications.

A. VHDL programming:

VHDL stand for very high speed integrated circuit hardware description language. It is used to model a digital system by dataflow, behavioral and structural style of modeling. It is firstly used in 1981by department of defense [7].

B. Entity declaration:

It defines the name of entity, inputs and outputs of system of hardware module. The entity direction will be input, output, or in out.

C. Architecture:

It can be describing by using structural, dataflow, behavioral or mixed style. we should have unique name of entity for which we write the architecture body.

D. Declaration: It defines the declaration of the results we get.

E. Front-end VLSI Design flow

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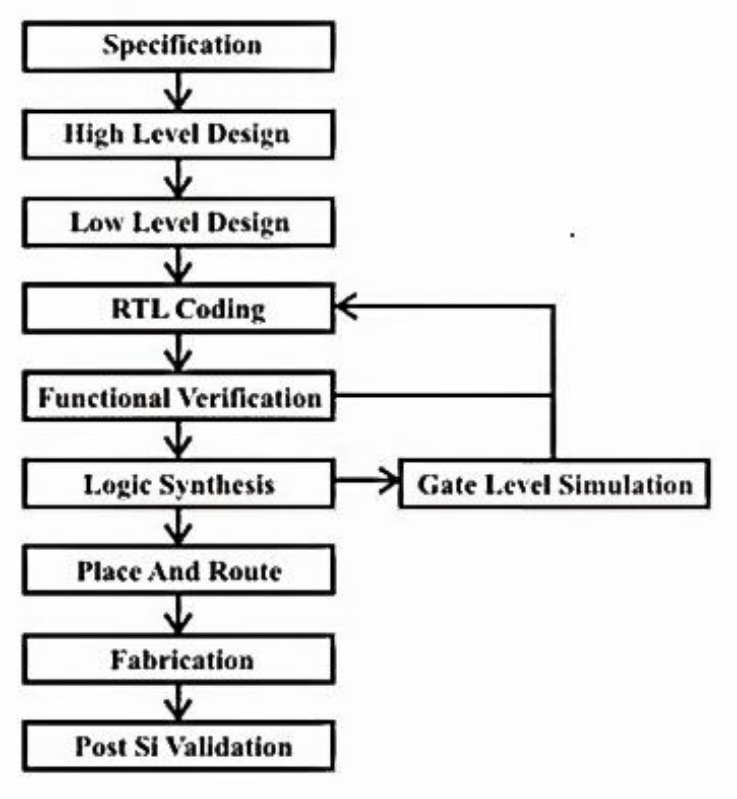

Figure 2: Front-end VLSI Design flow

IV. Results: Xilinx and Modalism Simulation of 2 Node Binary Tree Architecture

The Xilinx software simulation results for 2 node binary tree Architecture is shown in Fig 3 and Fig 4. The Fig 3 presents the RTL level view of the developed chip. The RTL provides the details of all the pins used for the design of the chip. The Figure 3 presents the internal schematics of the developed chip derived from the RTL view. The table 3 details about the functional use of the pins utilized in chip design of 2 node binary tree architecture.

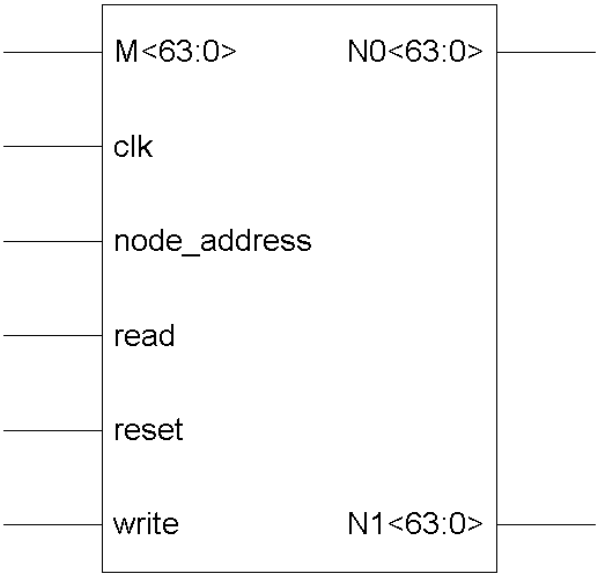

Figure 3: RTL view of 2 node binary tree architecture

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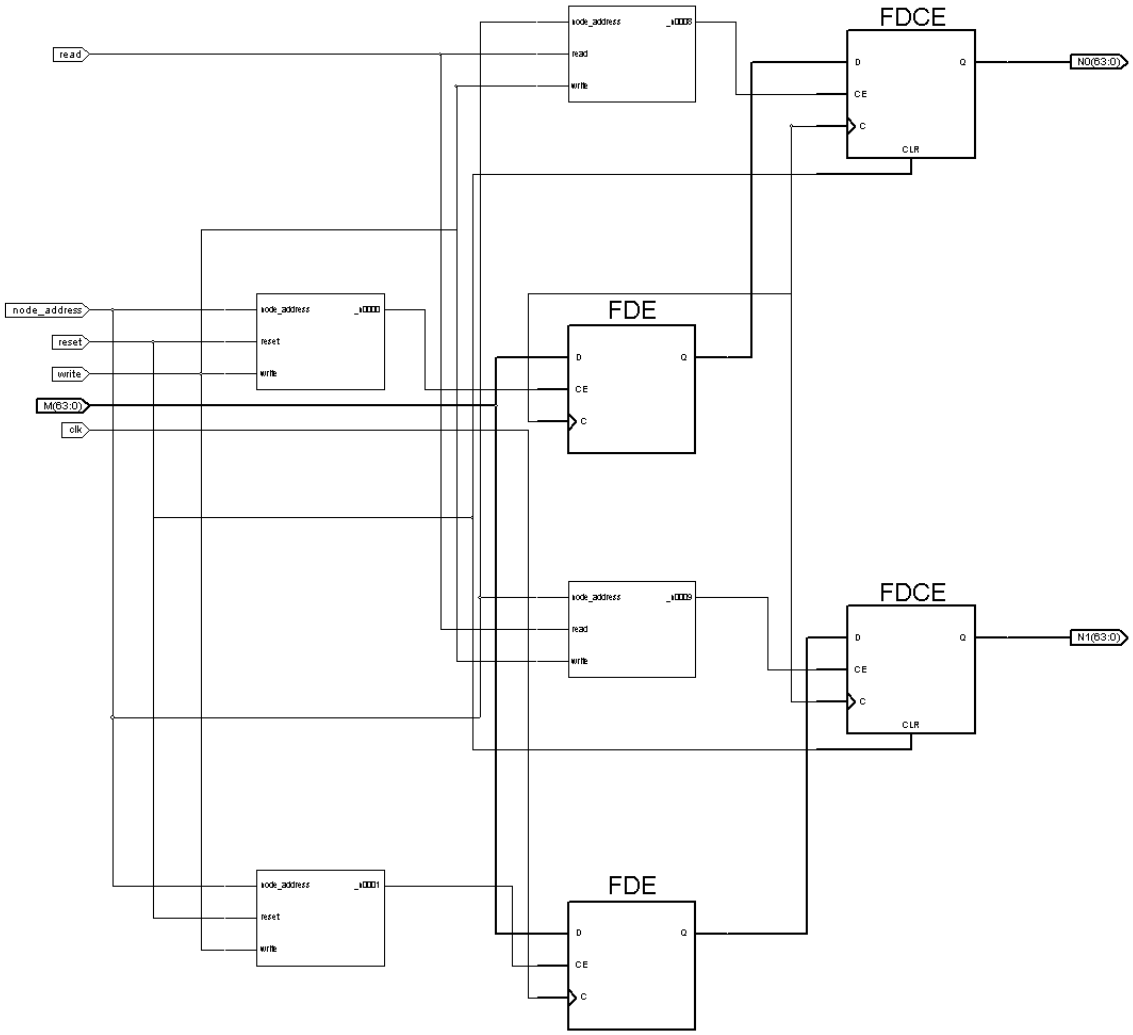

Figure 4: Internal schematic view of 2 node binary tree architecture

Table 1: Pin detail of 2 node binary tree architecture

Pin	Direction	Details
M (63:0)	Input	It the 64-bit data input of the binary tree NoC as the main processing element or node in the tree structure.
Node_address	Input	It is the input node address to assign the address of output nodes. Node_address = '0' for Node 0 and Node_address = '1' for Node 1.
Write (1-bit)	Input	It is the control signal input to write the Initial condition of the processing elements/ nodes. When Write = '1' then contents of the nodes are written to memory register.
Read (1-bit)	Input	It is the control signal input to read the data from the processing elements/ nodes. When Write = '0' and read = '1, then contents of the nodes are written to memory register.
Clk (1 bit)	Input	It presents the clock signal input to provide the positive edge of the clock with 50 % duty cycle.
Reset (1 bit)	Input	It is the reset input used to keep the data out of node 0 and node 1 as zero when reset signal is enabled.
N0(63:0)	Output	It presents the 64-bit output of the node 0 as node data output addressed by Node_address = '0'.
N1(63:0)	Output	It presents the 64-bit output of the node 1 as node data output addressed by Node_address = '1'.

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The functinal simulaion of the tree structure is done in Modelsim 10.0 software. The Modalism simulation input of 2 node binary architecture is given in Figure 4. The corresponding waveform with respect to binary input and ASCII data test cases is shown in Figure 5 and Fig 6. The simulation behavior is given in test case.

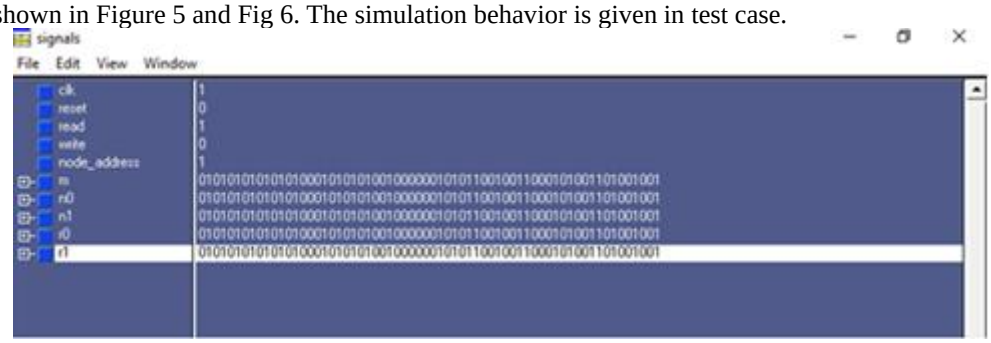

Figure 5 Modalism input for 2 node tree design

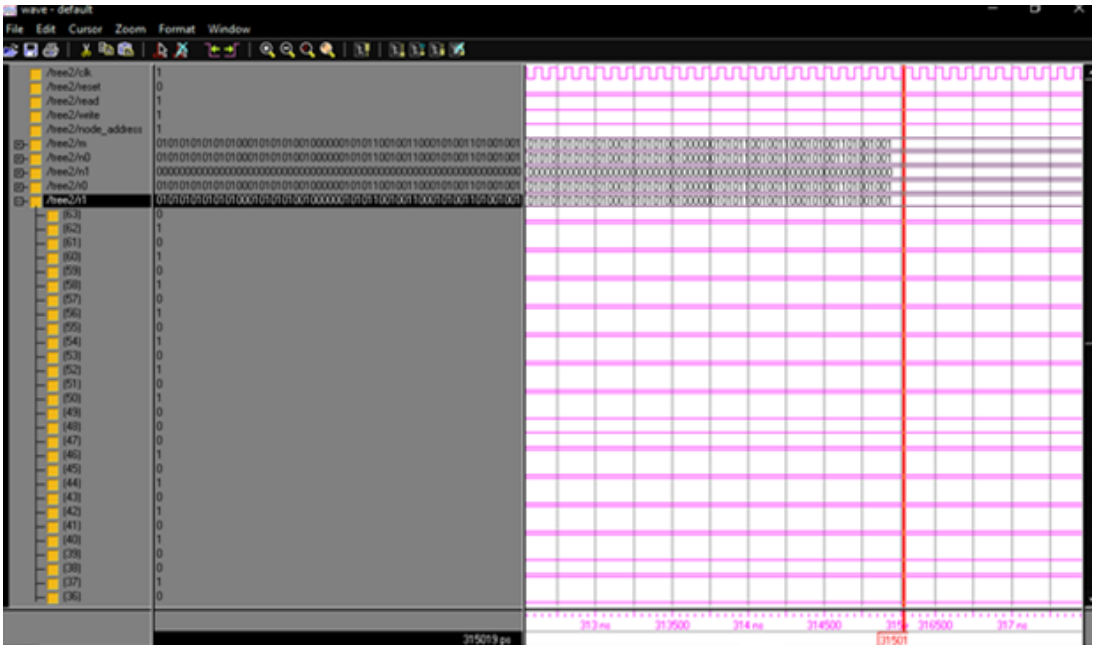

Figure 6: Modelsim Waveform simulation input for 2 node tree design in binary data

V. CONCLUSION

Binary tree topology is the one of the topology for network on chip design. In this thesis we have successfully design the hardware chip for cluster size 2, 4, 8 and 16 respectively. The function on simulation is done in Modelsim software the results are verified on Spartan 3EFPGA. Our research work is also compared with the existing work on reference design kizhappatVipin al (2019). The frequency supports the LUT utilization and FILOP-FLOP utilization as FPGA parameters are compared .The table 5.10. The refer design support 450 MHz ,407 MHz and 420 MHz for binary tree cluster size 2,4,8,16 respectively but our design supports 877.963 MHz which guarantee higher in FPGA. The LUT and flip-flop utilization in our design is less .our design is having 5, 21, 40,205 for cluster size 4,8 and 16 nodes. The reference paper utilization 522, 1616, 3603 LUT's. The flip-flop utilization in our design is 512, 1024 and 2048for cluster size 4,8,16 respectively. The reference design utilization 510, 1566 and 3726 respectively. Our binary chip is optimization in terms of hardware parameters such as LUT and flip-flop. The system support high frequency .our system is fastest in compared to existing work.

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BIOGRAPHY

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