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Simulation of 150W S-Band Solid State Power Amplifier

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Abstract: The emergence of new communication standards has put a key challenge for semiconductor industry to develop RF devices that can handle high power and high data rates simultaneously. The RF devices play a key role in the design of power amplifiers (PAs), which is considered as a heart of base station. This paper deals with the optimization of RF- LDMOS transistor and its evaluation in different PA classes, such as linear, switching, wideband applications. For accurate evaluation of RF-LDMOS transistor parameters, some techniques are also developed in technology CAD (TCAD) using large signal time domain computational load-pull (CLP) methods.
The amplifier design was done using a large signal model in ADS software. In 1 dB compression point for the simulated amplifier, 51.8dBm of output power, power added efficiency of 31.89% is achievedin class AB amplifier.

Keywords: AB Amplifier, LDMOS, ADS software

I. INTRODUCTION

From over 20 years, there has been an increasing demand for personal wireless communications. This has spurred competition among various providers for greater signal range, increased signal clarity and multimedia access. Therefore, there is a constant drive within the wireless communications industry to use the most advanced, yet cost-effective technology available. Several firms have risen to serve this need, among them is Infineon Technology. Infineon Technology designs and sells a wide range of products, including RF power transistors typically used in base stations. As part of their product development, Infineon Technology has introduced their sixth-generation dual gated Laterally-Diffused Metal-Oxide Semiconductor (LDMOS) transistor [6]. This transistor design has been used successfully in previous RF power amplifier designs, but for a 51.8dBm (150W) application it presents challenging design problems,

Particularly with respect to video bandwidth. It is therefore the goal of this project to analyse this new transistor and understand how it can be best implemented for RF power amplification. While the implementation will be designed to various specifications such as efficiency, gain and output power, the main objective will be to maximize the device's video bandwidth i.e. from 1.7-2.1 GHz.
The design must meet several exacting specifications, but of particular interest will be to maximize video bandwidth. Maximizing video bandwidth is best achieved by minimizing Third-order Inter-Modular Distortion (IMD3) products. A successful design will keep the magnitude of these products below -33dBc over a very wide carrier spacing. The IMD3 performance of the final design will be evaluated by providing a two-tone signal to the amplifier while it operates at an RF output power level of 51.8dBm (150W). The spacing between the two tones will be swept to a maximum of 75MHz. The maximum carrier spacing tolerated by the amplifier will be determined by the point at which IMD3 products exceed -33dBc (amplitude relative to that of the signal carrier). The final design must be able to operate in a MCPA configuration within a 75MHz spectrum between 1805-1880MHz. To this end, the project will follow a logical design process that divides a complete amplifier topology into sections, or "design blocks". Individual design blocks will be studied and optimized given ideal conditions. The design blocks will then be assembled around Infineon power transistor model, forming a complete amplifier prototype that can be further analyzed and optimized for the above criteria.

II. BLOCK DIAGRAM OF POWER AMPLIFIER& DESIGN STEPS

The input (IMN) and output matching networks (OMN) are parts of the amplifier to reduce unwanted reflections. Pin is input RF power to the amplifier while PL is the RF power to the load. Γin and Γout are the reflection coefficients at the input and output. Similarly, ΓS and ΓL are the source and load reflection coefficients respectively. DC biasing network is used to bias the transistor of an amplifier for a specific performance and class of operation.

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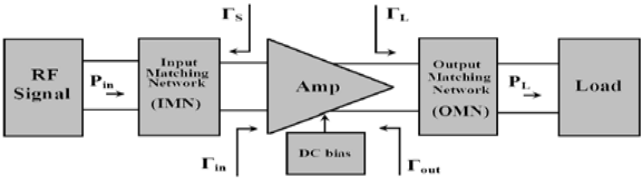

Fig-1: Block diagram of single stage power amplifier setup

So we have our amplifier IC to design 150-watt power amplifier. For development of any power PA the following steps are adapted, which we are going to done & discuss in detail step by step.

Step1: DC analysis of used LDMOS device for bias point selection.
Step2: Stability analysis of the amplifier.
Step3: Design input matching & output matching network with the help of smith utility chart.
Step4: Check the stability of complete amplifier setup i.e. with I/P& O/P matching network.
Step5: If found stable then start simulation for measurement of S-parameters.
Step6: If results are not up to the mark then we go through with tuning & optimization of design power amplifier.
Step7: For measurement of output power & PAE (power added efficiency) we perform single tone harmonic balance analysis.
Step8: Perform two tone harmonic balance analysis of design PA to see the complete harmonics Spectrum.

III. POWER AMPLIFIER SIMULATION

A. DC ANALYSIS:

An LDMOS transistor functions much the same way as any other MOSFET device in that it requires voltage at its gate terminal to effect a current though its channel. The objective statement defined earlier specified a quiescent drain current (IDQ) of 2.6 A. With this in mind, a DC analysis was required as a first step in characterizing the transistor assigned to this project. The purpose of the DC analysis was to sweep the bias voltage at the transistor's gate in order to identify its linear and nonlinear regions. The results of this analysis provided a better understanding of the bias voltage requirements of the transistor and how it operated at an IDQ of 2.6A. DC analysis of NXP's transistor model was performed in ADS.

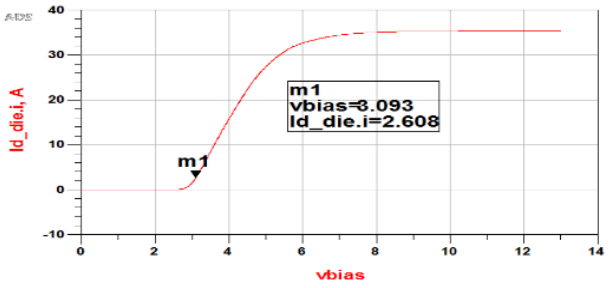

Fig-2: DC analysis result

B. STABILITY MEASUREMENT OF TRANSISTOR:

From result we have seen that stability factor is greater than one & stability measure consists positive value for all band i.e. from 1.7 GHz to 2. 1GHz.which is our desire result.

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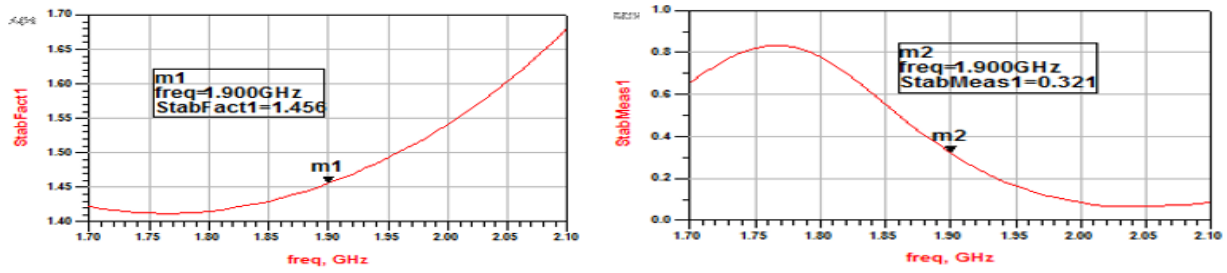

Fig-3: Stability measurement of transistor amplifier

C. DESIGN INPUT MATCHING NETWORK & OUTPUT MATCHING NETWORK :

We select Z source impedance & Z Load impedance from the given data sheet of Transistor Amplifier at particular frequency for which we have to design our Power Amplifier circuit. After that with the help of smith chart utility by using these source & load resistances we find our input & output matching schematic.

D. SMITH CHART UTILITY:

The Smith Chart Utility facilitates gain, stability, and noise analysis of devices characterized by scattering parameters. It also enables simple design of lumped and distributed element matching networks using an intuitive graphical interface.

Frequency	**Z Source**		**Z Load**	
MHz	**R**	**jX**	**R**	**jX**
1730	1.86	-4.25	0.55	-2.78
1768	1.77	-4.06	0.54	-2.66
1805	1.68	-3.88	0.53	-7.54
1843	1.61	-3.70	0.52	-2.43
1900	1.56	-3.53	0.51	-2.32
1918	1.51	-3.37	0.51	-2.21
1955	1.47	-3.22	0.5	-2.11

TABLE I. Source & Load Resistances

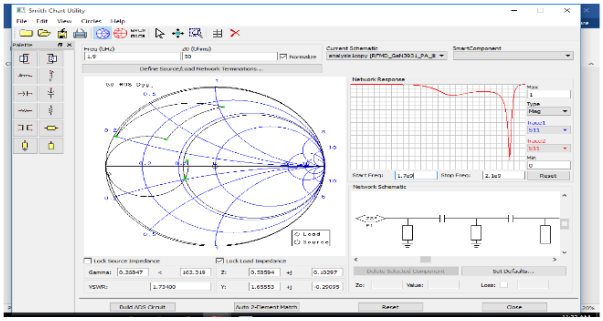

Fig:4 Smith chart utility

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E. STABILITY ANALYSIS OF COMPLETE POWER AMPLIFIER:

After designing gate bias network, drain bias network, input matching & output matching network we go for stability analysis of complete Power Amplifier setup by drawing sub-circuit network of all schematic.

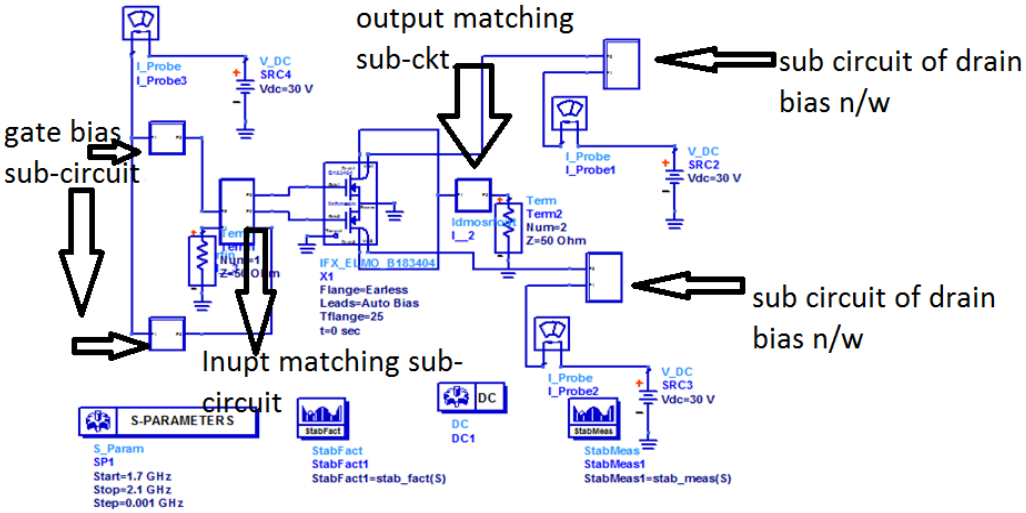

Fig-5: Stability analysis of complete Power Amplifier

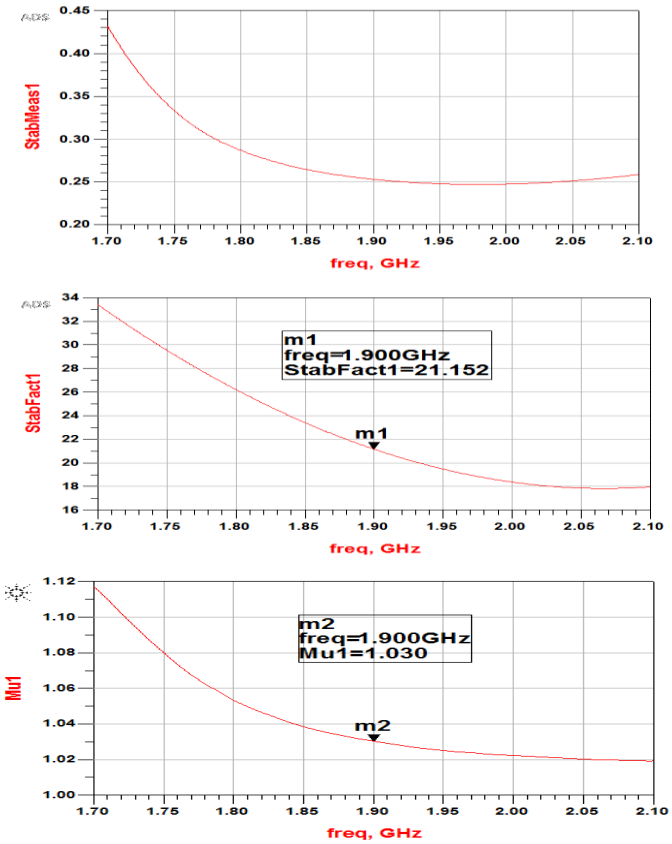

Fig-6: Result of Stability analysis of complete Power Amplifier

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F. S-PARAMETERS ANALYSIS:

After analysis of complete amplifier setup we found that our PA is stable for the range of 1.7 GHz-2.1 GHz. Now we look at scattering parameters of design Power Amplifier. These are the final result after optimization and tuning of complete amplifier setup.

[i] Optimization and Tuning:

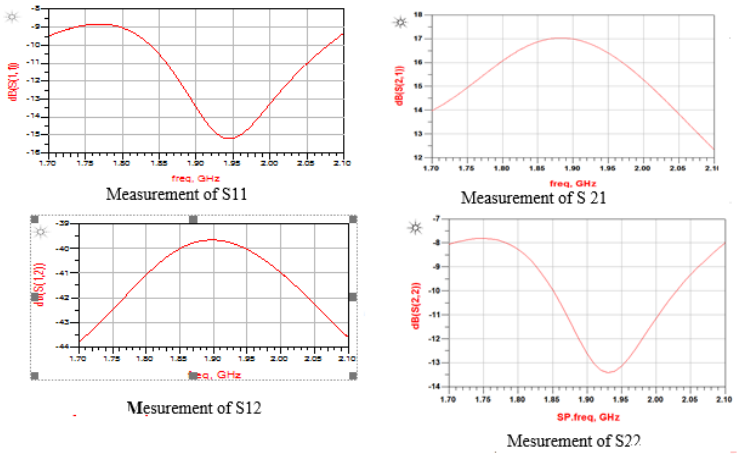

Fig-6: S-parameters

In simulation variable setup there is an option to optimize & tuning the Power Amplifier parameter. We can tune all the parameters but we generally tuned the input matching network & output matching network parameters & capacitors are also play a great role to get desired result. After many time tune the parameters of setup like W, L & values of capacitors used I got the following results.

G. HARMONIC BALANCE ANALYSIS:

When designing a circuit with non-linear elements, usually we are only interested in the integration of a couple of frequencies. This analysis takes into account the non-linear elements of the circuit and restricts the analysis to several important frequencies. This is usually faster than doing a complete transient analysis and then extracting the required information from the temporal signal by Fourier transform techniques. Harmonic balance analysis we perform here for single tone & double tone measurement. Single tone measurement gives us output power, complete harmonics spectrum, PAE (power added 5efficiency).This is ideal for obtaining an estimate for the IMD3 products by simulating two tone test measurements.

[i] Single Tone Harmonic Balance Analysis:

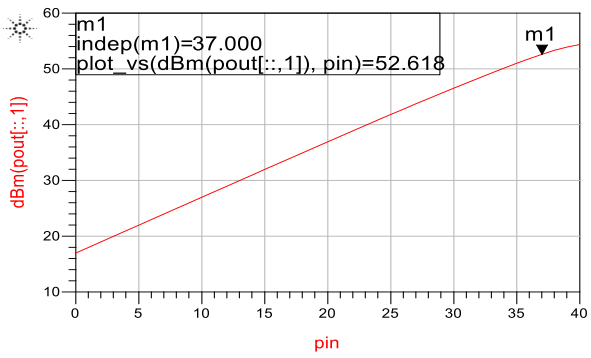

Fig-7: output power vs input power

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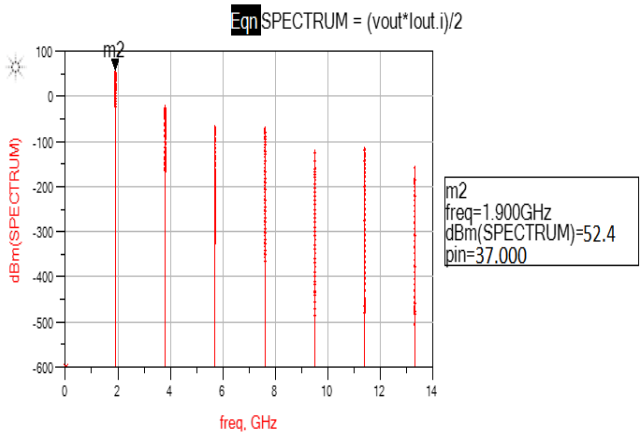

Fig-8: mesurement of frequency spectrum of Power amplifier

[ii] Two tone harmonics balance analysis:

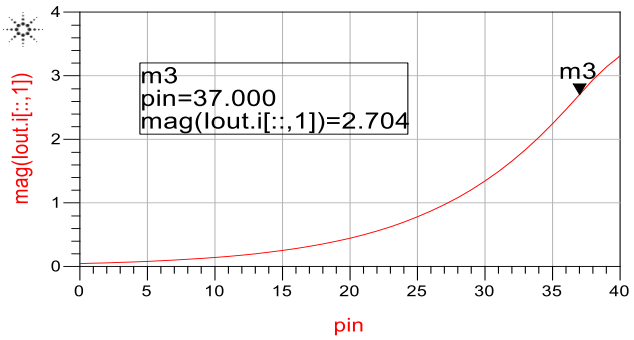

Fig-9: output current vs input power

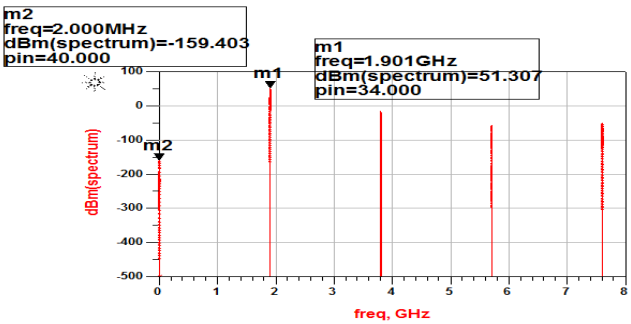

Fig-10: Two tone harmonics balance analysis setup result

IV. CONCLUSION

All LDMOS transistors are considered important device in wireless communication technology for power amplification. It will be remaining in future due to mature silicon technology, and cost-effective solution.

We optimized intrinsic physical structure of LDMOS transistor in TCAD, and obtained promising results to enhance the performance of LDMOS devices. The optimization was made by introducing the excess interface charges at the RESURF of LDD region, which is also compared with a famous dual-layer surface doping technique (other parameters and dimensions were the same). 60 % additional enhancement is observed in our optimized LDMOS transistor. The reason is surface doping technique needs an implanted dose with specific thickness according to Gaussian phenomena while in

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case of interface charges, a thin depletion layer is created at the RESURF. Thus interface charges are more effective than additional n-type implanted dose in LDD region

The CLP simulation technique in TCAD is a novel way to study the *RF* analysis of the transistor for PA design. It provides extraction of impedances of the active device without including any parasitic effects, and helpful for PA designers to match the device properly. Therefore, it can be used to design narrowband, tuneable and broadband matching networks. CLP simulation technique is extended to study the non-linear behaviour of *RF*- power transistors under a real large signal operation. Through this the nonlinear capacitances of the device are simulated directly as a load. The CLP technique is also further extended to understanding of transistor behaviour for high efficiency PA operations, such as Class-F. Through these, *RF*- transistor's response can be studied at different frequencies, and bias points for optimal performance. These CLP techniques provide an initial ground work to understand the mechanisms of new and fabricated *RF* transistors to improve over-all performance of the system.

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