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VLSI DESIGN OF A SQUARING ARCHITECTURE BASED ON VEDIC MATHEMATICS

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Abstract: In the modern world of digitalization, processing of data in real time requires an increase in the operating speed of a system. In digital epoch, the thirst for high speed is fulfilled by the accomplishment of digital multipliers. Multipliers play a fundamental role in many high-speed applications where the complex multiplications are carried out by squaring operations. Vedic Mathematics is a part of Atharva Veda which deals with the easiest methodology for all types of arithmetic calculations. Dvanda Yoga is one of the squaring algorithms of Vedic Mathematics. In this project, the design is simulated and realized with the help of Xilinx 9.2i.

Keywords: Multiplication, Squaring Architecture,Vedic mathematics, Xilinx 9.2i.

I. INTRODUCTION

In arithmetic operation Multiplication is an important fundamental function and operations which are based on Multiplication. The speed of calculations of operations are increase by so many operations which are based on multiplication like Multiply and Accumulate (MAC) and computation intensive arithmetic function (CIAF) , convolution, FFT, filtering and in microprocessor & microcontroller's arithmetic and logical unit. Vedic techniques are very fast and logical its Vedic mathematics approach is totally different and considered very close to the way a human mind thinks and works. Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.

II. PROPOSED SYSTEM

Multipliers being the key components of various applications and the throughput of applications depend on Arithmetic and logic units (ALU), Digital signal processing blocks and Multiplier and accumulate units. Vedic Multiplier has become highly popular as a faster method for computation and analysis. So that the latency of conventional multiplier can be reduced. The Multiplication of two numbers as shown in Fig 4.1 Formula Used (A) is First Number and (B) is Second Number. The Process (Right to Left) Vertical Multiplication of first digit and last digits of both the numbers are square and this two number with two multiplication.

III. WORKING PRINCIPLE

The Vedic algorithms are very useful in designing digital multiplier to reduce calculation time or to increase the speed of multiplier. Vedic multiplier makes the calculation of data very fast as compared to simple multiplier for complex

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multiplication. The conventional multiplication method generates partial products to produce output, in the technique of Vedic multiplier the number of partial products generated is less.

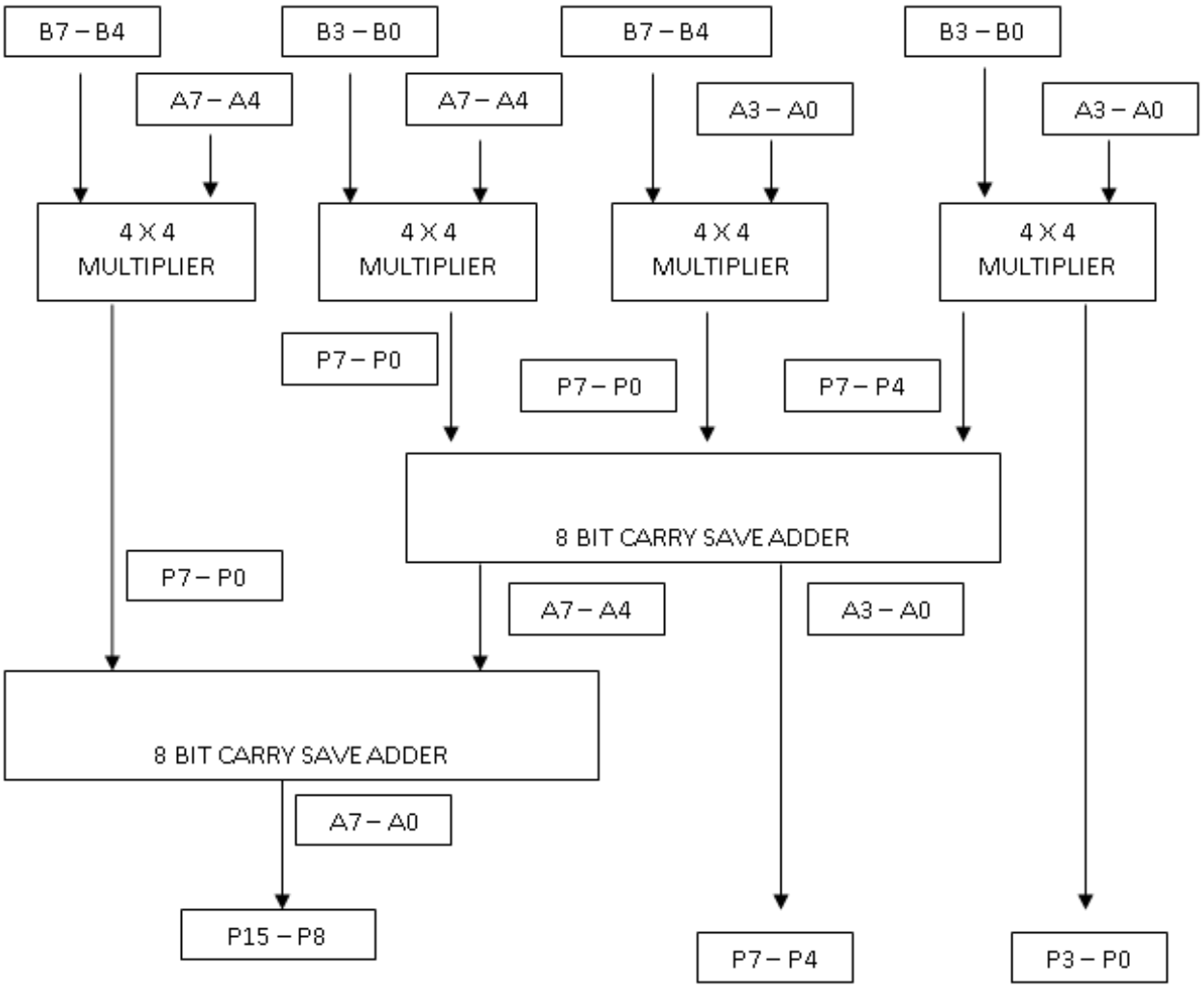

Fig. 1 Block Diagram of Proposed of Vedic Multiplier

IV. MATERIALS AND METHODS

Software used in this project are Xilinx 9.2i software

CARRY SAVE ADDER

Carry Save Adder The carry save adder seems to be the most useful adder for our application. It is simply a parallel ensemble of k full-adders without any horizontal connection. Its main function is to add three k-bit integers A, B, and C to produce two integers C 0 and S such that

$$C\,0 + S = A + B + C.$$

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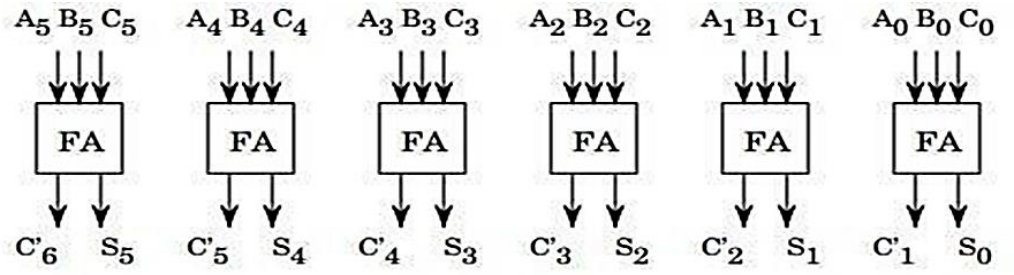

Fig. 2 Block Diagram of Carry Save Adder

V. RESULT AND DISCUSSION

INPUT

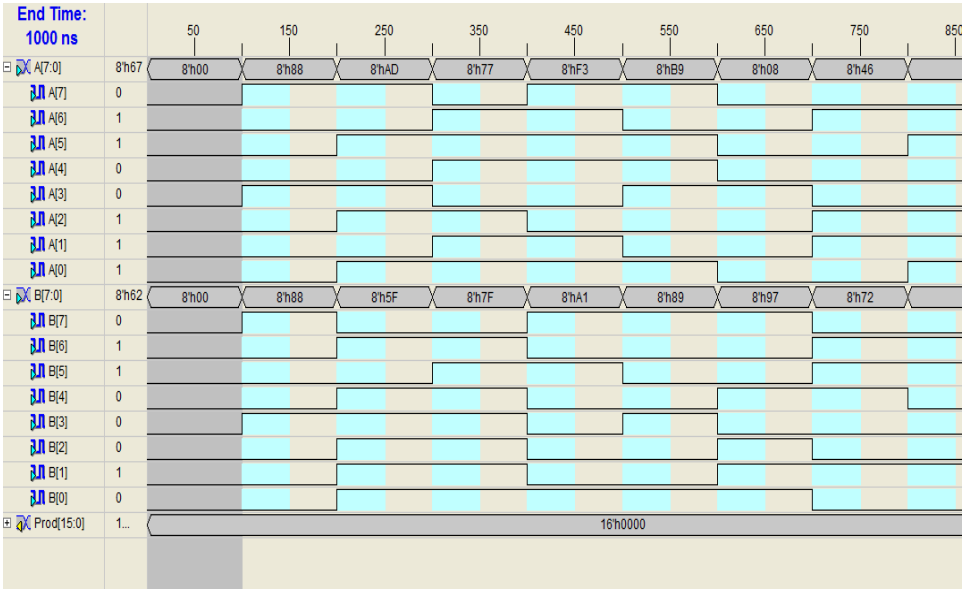

Fig. 3 Proposed Multipler input

OUTPUT

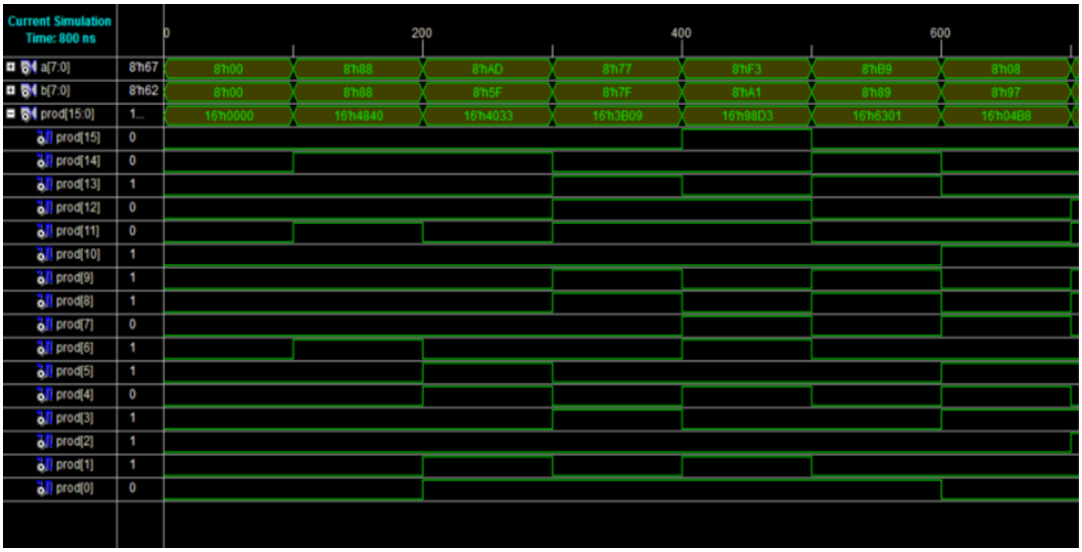

Fig. 4 Proposed Multipler output

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The designs of Proposed Multipler System Have were successfully simulated using Xilinx 9.2i software. The design of simple combinational circuits was acquired perfectly through gate behavior observation and considerations. As shown in fig. 3 Multipler input and fig. 4 Multipler output was also found out that practical results recorded were corresponding to theoretical results so every practical observation matched it is expectation thus the practical results were exactly the same as the theoretical results. The combination circuit connection was perfect and all the other connections that were made gave all the rights

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