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Comparative Analysis of Fast Adder Circuit

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Abstract: Digital systems are the most important part of VLSI industry. To ensure fast computation fast circuits are required. Adders are the key component of digital design. This paper refers to the comparative analysis of various Adder circuits based on the parameters like propagation delay, no. of Look up tables utilized, no. of Input Output Blocks required and total memory utilization of adder circuit. The adder circuits like Carry Save Adder, Ripple Carry Adder and Carry Look ahead Adders are designed & simulated for 4 inputs each of 4 bit addition operation using XILINX ISE 9.2i.

Keywords : Carry Save Adder, Carry Look ahead Adder, VHDL Simulation.

I. INTRODUCTION

Now-a-days, Digital Image Processing has wide application in day to day life. It has become key component in many consumers, communications, medical, and industrial products. Digital signal processing applications require high computational performance due to their real-time characteristics. Very high speed integrated circuit Hardware Description Language (VHDL) can be used to model a digital system at many levels of abstraction, ranging from algorithmic level to the gate level. The complexity of the digital system being modeled could vary from that of a simple gate to a complete digital electronic system.

The digital system can also be described hierarchically; timing can also be explicitly modeled in the same description. The VHDL language can be regarded as an integrated combination of the following languages; Sequential language, Concurrent language, Net list language, Timing specifications, and Waveform generation language. The high computational performance depends upon the basic components of the systems. Adder is mostly used as a basic building block in digital systems.

The rest of the paper is organized as follows: section II briefly describe about various adders and explains detailed architecture of different types of adder circuits, In Section III the simulation result and the performance of the circuits are shown. Finally, Section IV concludes the paper discussing the analysis of the circuit based on the performance parameters.

II. ADDER CIRCUIT

An adder is a combinational circuit that performs the arithmetic sum. A half adder circuit is used to perform addition of two bits and produces sum and carry as an output. But due to limitations on addition of carry input a full adder circuit is used which provides facility to add carry bit and produces sum and carry as an output.

Various other Adder circuits are:

ADDER CIRCUIT DESIGN

1. Carry Look Ahead Adder

In this section, the basic design structure has been discussed. The carry look-ahead logic uses the concepts of generating and propagating the carry bit [3]. The carry-look-ahead adder calculates the carry signals in advance, based on the input signals. It is based on the fact that a carry signal will be generated in two cases: (1) when both bits a_i and b_i are 1, or (2) when one of the two bits is 1 and the carry-in (carry of the previous stage) is 1.The basic idea of CLA is computing the carries simultaneously.i.e.all the carries in the same group are computed at the same time.

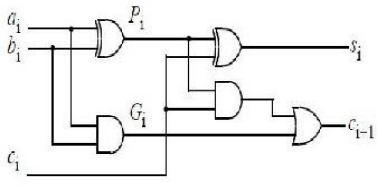

Fig1. Carry Look Ahead Adder ckt

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The expressions are :

SUM, Si=Pi ⊕Ci

Carry_out, Ci+1=Gi+CiPi

Carry Propagates, Pi=Ai ⊕Bi

Carry generates, Gi=Ai.Bi

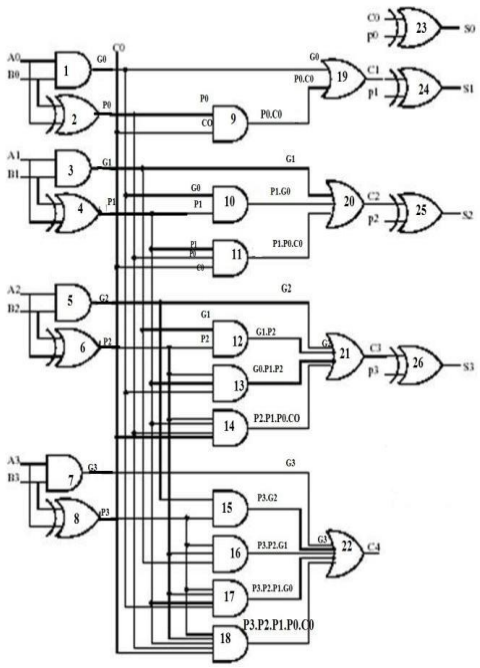

Fig.2. Gate level architecture of 4 bit Carry Look Ahead Adder

From above architecture it is seen that the carry out bit Ci+1 will be available after 4 delays.

2. Ripple Carry Adder

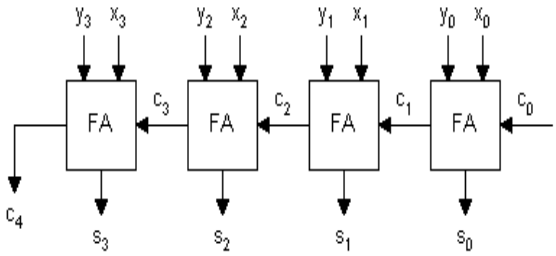

Fig.3.Ripple Carry Adder

Ripple Carry Adder can be constructed by connecting full adders in cascade. The carry output from each Full adder is connected to the carry in of each Full Adder in chain as shown in fig.3.Thus in RCA the carry ripples through the 4 full adders to appear at the output, while the sums are available after 2 XOR delay. The output is known after the carry generated by the previous stage is produced. Thus the sum of MSB (most significant bit) is available only after the carry signal has rippled through The stages of full adder i.e. from least significant bit to most significant bit. A considerable delay is measured when final sum & carry is available [2]. Figure 3 shows the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder. It is seen from Figure 3 that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits x0 and y0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits So-S3.

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3. Carry Save Adder

In situation where we have a lot of numbers to add like Multiplication (adding partial products) & accumulation loop, we can defer the propagation of carries until the last addition. There are many cases where it is desired to add more than two numbers together. The Carry Save Adder [6] reduces the addition of 3 numbers to the addition of 2 numbers. The propagation delay is 3gates irrespective of the no of input bits The straightforward way of adding together m numbers (all n bits wide) is to add the first two, then add that sum to the next, and so on. This requires a total of m − 1 additions, for a total gate delay of O (mlg n) (assuming look ahead carry adders). Instead, a tree of adders can be formed, taking only O (lgm · lg n) gate delays. Using carry save addition, the delay can be reduced further still. The idea is to take 3 numbers that we want to add together, x + y + z, and convert it into 2 numbers c + s such that x + y + z = c + s, and do this in O (1) time. The reason why addition cannot be performed in O (1) time is because the carry information must be propagated. In carry save addition, we refrain from directly passing on the carry information until the very last step [1].

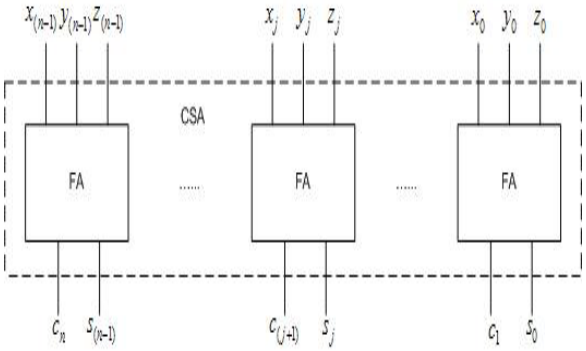

Fig.4 Carry save Adder

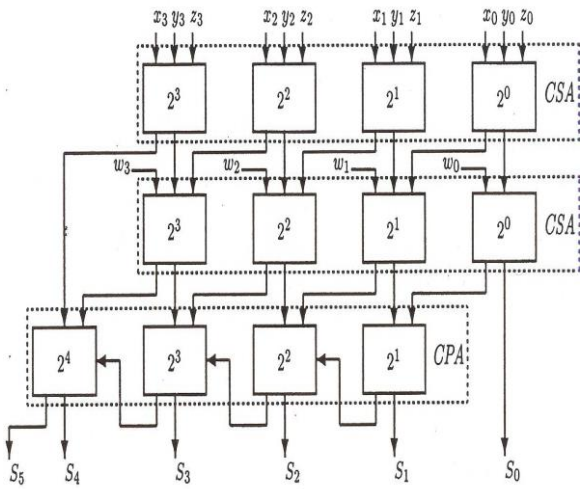

Fig.5. A 4 bit Carry Save Adder

The carry-save unit consists of n full adders, each full adder computes a single sum and carries bit based on the corresponding bits of the three input numbers as shown in fig 4. The entire sum can then be computed by shifting the carry bit left by one place and appending a 0 to the MSB (most significant bit) of the partial sum Sequence. This process can be continued indefinitely, adding an input for each stage of full adders, without any intermediate carry propagation [1][2]. These stages can be arranged in a binary tree structure, with cumulative delay logarithmic in the number of inputs to be added, and invariant of the number of bits per input. The main application of carry saves algorithm is, well known for multiplier architecture is used for efficient CMOS implementation of much wider variety of algorithms for high speed digital signal processing .CSA applied in the partial product line of array multipliers will speed up the carry propagation in the array.

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III. SIMULATION RESULT

For experimental simulation of the different adder circuits, the codes are written in VHDL and simulated using Xilinx ISE9.2i.

The 4 inputs x0 y0, x1 y1, x2 y2, x3 y3 is given to all types of adder. And sum results are observed .To carry out synthesis & simulation Xilinx ISE 9.2i is used. The FPGA used is Virtex 5 (xc5vlx50t-3ff1136).The simulation results are as follows-

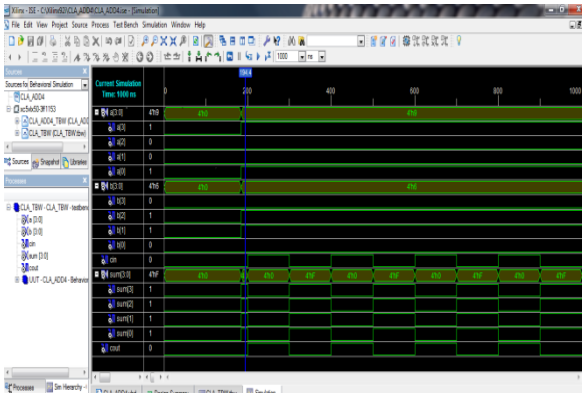

Fig.6.Addition result of 4,4-bit nos. using CLA

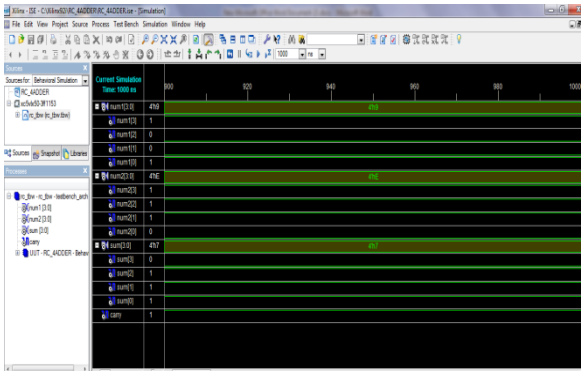

Fig.7.Addition result of 4, 4-bit nos. using RCA

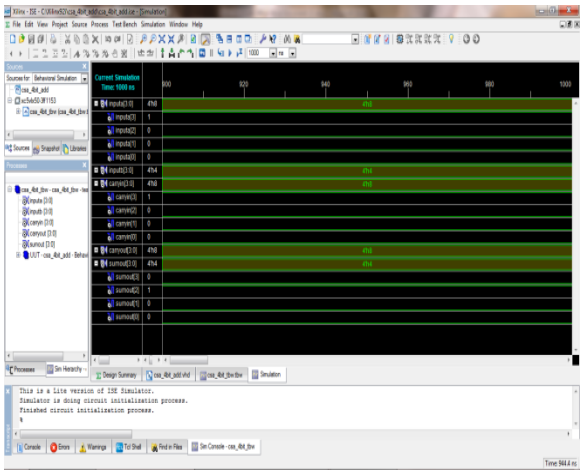

Fig.8.Addition result of 4, 4-bit nos. using CSA

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TABLE I: Simulation Result Analysis

Type	Parameter	% Utilization	% Delay	Total Memory Usage
CLA	LUT	6/28800=0%	4.065 ns	305808 kilobytes
	IOB	14/560=2%		
RCA	LUT	6/28800=0%	4.233ns	306000 kilobytes
	IOB	13/560=2%		
CSA 4 BIT	LUT	8/28800=0%	3.378ns	306000 kilobytes
	IOB	20/560=3%		
CSA 16 BIT	LUT	17/28800= 0%	5.405 ns	306256 kilobytes
	IOB	22/560=2%		

IV. CONCLUSION

For fast application, faster device is required. From above simulation results it is seen that Carry Save Adders are the faster adders as the % propagation delay for operation is minimum i.e. 3.37 ns compared to other adders such as Carry Look Ahead Adder which is 4.005 ns and Ripple Carry Adder i.e.4.233 ns. In RCA delay increases linearly with the bit length. Hence it is not efficient when large bit numbers are used. In CLA due to simultaneous computing of carry signal the carry delay problem is reduced. Also the utilization or memory for operation is similar for RCA & CSA i.e. 306000 Kb. A 16 Bit Carry Save Adder is designed for which delay is 5.405ns & memory utilization is 306256 Kb.

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