IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 10, Issue 6, June 2021

DOI 10.17148/IJARCCE.2021.10667

741 IC Based Low Power Operational Amplifier

Prof. Sandeep Mishra[1], Shanta Lakra[2]

Professor,Dept. Of ET & T, Kalinga University, New Raipur, Chhattisgarh, India[1]

PG Student, Dept Of ET & T, Kalinga University, New Raipur, Chhattisgarh,India[2]

Abstract- The operational amplifier is a fundamental building block for electronic devices and systems. The advancement of modern electronic technology has been setting more performance demand on the underlying integrated circuits including the operational amplifier. Reduction in power consumption and improvement in speed are some of the most important requirements. To address these concerns, this thesis presents a design of micropower Class AB operational amplifiers which has the ratio of gain bandwidth product to supply current higher than that of an existing IC. The design is in a 0.6pxm CMOS process. The input stage of the design has the folded-cascode architecture that allows the input common-mode range down to negative supply voltage. The Class AB output stage swings rail-to-rail and has the ratio of maximum current to quiescent current greater than 100. The bias cell of the operational amplifier is designed to consume only 6% of the total supply current. The thesis concludes the operational amplifier design with two frequency compensation options.(cont.) The one with simple Miller compensation has a unity gain frequency of 360kHz with 61.5 degrees of phase margin at 100pF load while consuming 20[mu]A supply current. The other with the hybrid of simple Miller compensation and cascode compensation offers an improved unity gain frequency of 590 kHz at the same loading and power condition.

Keywords - FET,MOSFET, 741 OP-AMPS,CMOS,COMMON- MODE RANGE,POWER-SUPPL REJECTION RATIO,CASCODE,SLEW RATE

I.INTRODUCTION

In the current digital market [1], the trend towards the development of bio-medical devices with portable batteries has recently increased. This phenomenon is because of progress and advancement in scaling of VLSI technology leading to more analog and digital circuit (ADC) creation in deep submicron size [2]. This condition has its own advantages where, at lower voltage supply, the circuit can be operated with lower power consumption

The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with vastly different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc . Generally an Operational Amplifier is a 3-terminal device. It consists mainly of an Inverting input denoted by a negative sign, ("-") and the other a Non-inverting input denoted by a positive sign ("+") in the symbol for op-amp. Both these inputs are very high impedance. The output signal of an Operational Amplifier is the magnified difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier.[3]

1.1 System Overview

For Op-amps used in many useful applications, rather a surprisingly large number of applications, the actual amplifier performance is closely approximated by an idealized amplifier model. Indeed quite frequently circuits are designed explicitly to insure acceptabilityof this approximation.Consider the 741 amplifier, an older but proven industry-standard device, which has a voltage gain exceeding 105 in normal operation. To cause an output voltage change between representative saturation voltage limits of ±15 volts. A basic op-amp consists of 4 main blocks

a.Current Mirror
b.Differential Amplifier
c.Level shift, differential to single ended gain stage
d.Output buffer

The general structure of op-amp is as shown in figure 1 below:-

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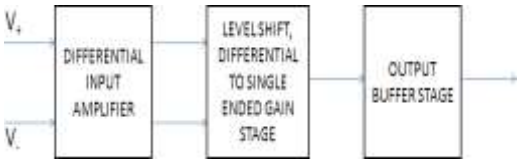

Figure 1: General Structure of op-amp

The first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The second stage performs Level shifting, added gain and differential to single ended converter. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).[11-12]

II.BACKGROUND AND LITERATURE SURVEY

Existing PLC Implementations:

The existing power line communication being implemented at various places and enumeration of standards evolved. In Europe PLC is termed as narrow band PLC because allocated frequency band for PLC is 3 KHz to 148.5 KHz, which is further divided into four sub-bands for different applications.

- CENELEC A (9 KHz to 95 KHz)
- CENELEC B (95 KHz to 125 KHz)
- CENELEC C (125 KHz to 140 KHz)
- CENELEC D (140 KHz to 148.5 KHz)

S.S. Rajput and S.S. Jamuar, "Low voltage, low power high performance current mirror for portable analogue and mixed mode applications." In Proc. IEE Circuits Devices and Systems, 2001, vol. 148, no. 5 pp. 273-278.
Schlogl, F.; Zimmermann, H. "Low-voltage operational amplifier in 0.12 μm digital CMOS technology" IET Journal 2004, Pages: 395 – 398.
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C. Zhang, A. Srivastava, P. K. Ajmera, "A 0.8 V CMOS amplifier design", Analog Integrated Circuits and Signal Processing, 47, pp 315-321, 2006, Springer Science.

III.METHODOLOGY

An operational amplifier is often called an op-amp. It is a DC-coupled differential input voltage amplifier with an rather high gain. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. Thus for an ideal op-amp the input signal is almost always a differential signal and hence a differential amplifier is generally used as the input stage of an Operational Amplifier. However, the infinite gain or bandwidth that characterizes an ideal operational amplifier is seldom found in a real Operational Amplifiers like the widely used uA741. Typically the "Open Loop Gain" of a real operational amplifier is defined as the amplifiers.

A.PRINCIPAL OF OPERATION

An op-amp has a differential input and single ended output. So, if we apply two signals one at the inverting and another at the non-inverting terminal, an ideal op-amp will amplify the difference between the two applied input signals. We call this difference between two input signals as the differential input voltage. The equation below gives the output of an operational amplifier.

$$Vout= Aol(V1-V2)$$

Where, V_{OUT} is the voltage at the output terminal of the op-amp. A_{OL} is the open-loop gain for the given op-amp and is constant (ideally). For the IC 741 A_{OL} is 2×10^5.
V1 is the voltage at the non-inverting terminal.V2 is thevoltage at the inverting terminal.
(V1-V2) is the differential input voltage.

B. ANALYSIS OF NON LINEAR IMPERFECTION

Output voltage is limited to a minimum and maximum value close to the power supply voltage. The amplifier's output voltage reaches its maxim slewing occurs, further increases in the input signal have no effect on the rate of change of the output. Slewing is usually caused by the input stage saturating rate of change, the slew rate, usually

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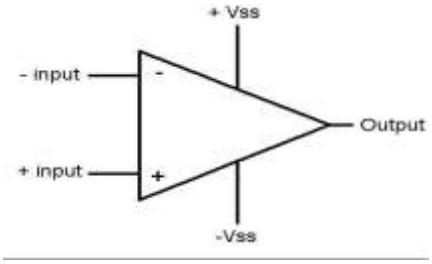
specified in volts per microsecond (V/μs). The output current must be finite. In practice, most op amps are designed to limit the output current so as not to exceed a specified level – around 25 mA for a type 741 IC op amp – thus protecting the op amp and associated circuitry from damage. Modern integrated FET or MOSFET op amps approximate more closely the ideal op amp than bipolar ICs when it comes to input impedance and input bias currents. Bipolar are generally better when it comes to input voltage offset, and often have lower noise. Generally, at room temperature, with a fairly large signal, and limited bandwidth, FET and MOSFET op amps now offer better performance.

IV.OPERATIONAL AMPLIFIER

The general operational amplifier symbol is as shown in Figure 2 below:-



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An operational amplifier is often called an op-amp. It is a DC-coupled differential input voltage amplifier with an rather high gain. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. For most general applications of an op-amp a negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output ("closed- loop") voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration.

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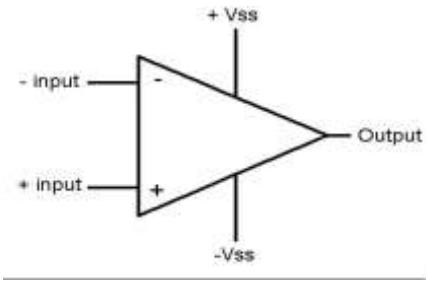

Equivalent Circuit Of An Op-AMP

An equivalent op-amp circuit is shown in the circuit below. It consists of two inputs often referred to as the inverting and non-inverting inputs. The input resistance or rather impedance is referred in the diagram as Z_{in} and the output impedance is given by Z_{out}. This is the basic block diagram of a op-amp which generally has a single output.

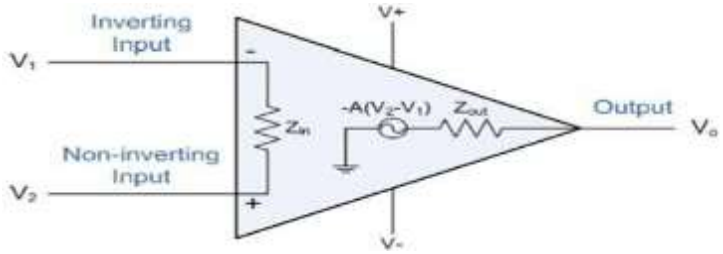

Figure 3: Equivalent Circuit for ideal operational amplifier

Idealized Characteristics

(a) Voltage Gain, (A) **Infinite**
(b) Input impedance (Z_{in}) **Infinite**
(c) Output impedance, (Z_{out}) **Zero**
(d) Bandwidth, (BW) **Infinite**

IJARCCE

ISSN (Online) 2278-1021
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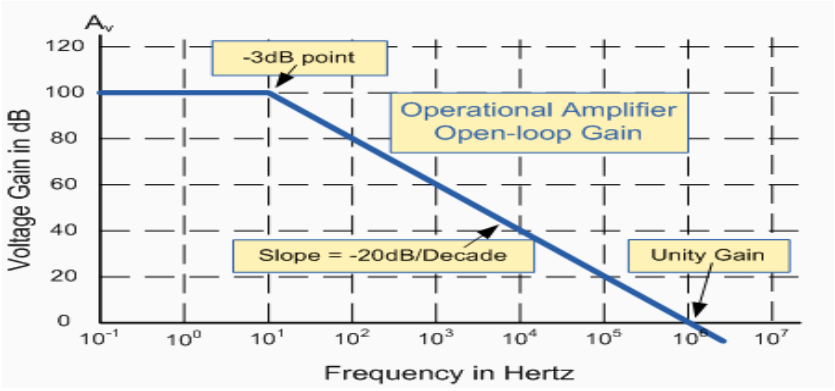
(e) Offset Voltage, (V_o) **Zero**

Open Loop Frequency Response Curve

V.RESULT & DISCUSSION



The designed op-amp was simulated to find the different characteristics of the designed op-amp. Further the layout of the designed op-amp was created and the parasitic capacitance and resistance was extracted. The extracted designs were then simulated with the parasitic values and compared with the schematic. Later in the chapter we also compare the obtained parameters of the device through simulation to the specifications for the device and with the post layout simulation results. The different results are presented here.

Offset Voltage

It is the voltage obtained at the output terminals, when the input terminals are connected to ground terminal, i.e., 0 volts. Here the offset voltage calculated for the op-amp is -603mv.

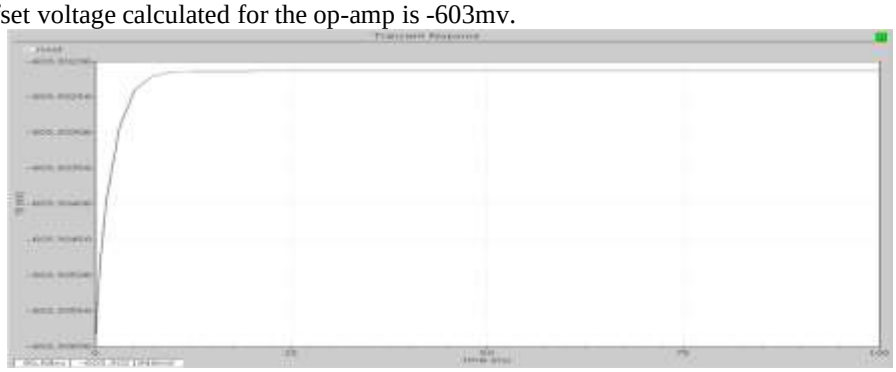


Figure 4: Op-Amp offset voltage

Slew Rate

It is the maximum rate of change of output voltage. Here the slope of the curve calculated as 12.5 v/µs.

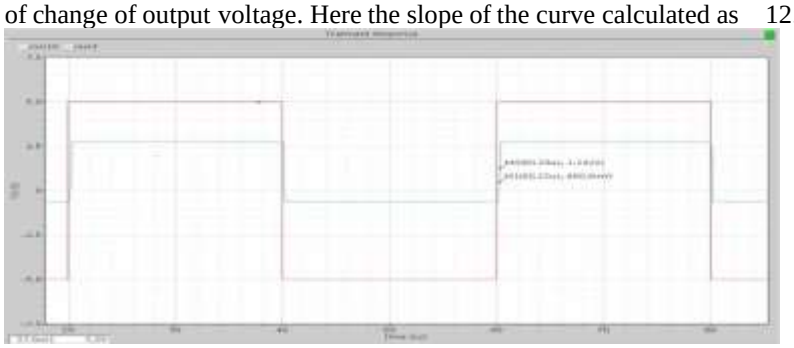


Figure 5: Op-amp slew rate

Gain

It is defined as the ratio of the output to the input. Here the input voltage given as 1 volts sinewave. Hence the gain is calculated as 10.4v/v.

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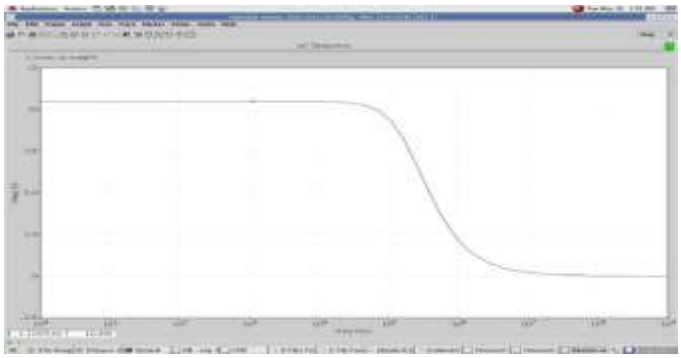

Figure 6: Op-Amp Gain

Bandwidth

It is the maximum allowable range of the frequencies. Here the bandwidth of this op-ampcalculated as 2.16 MHz for unity gain and 202kHz at -3dB.

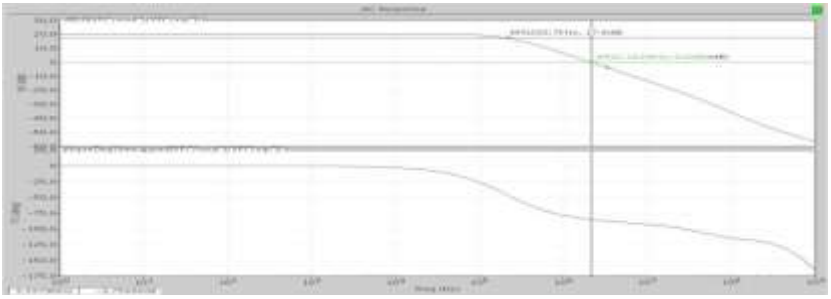

Figure 7: Op-Amp bandwidth

LAYOUTS AND RC –EXTRACTED VIEWS

Bias circuit for amplifier current sinks:

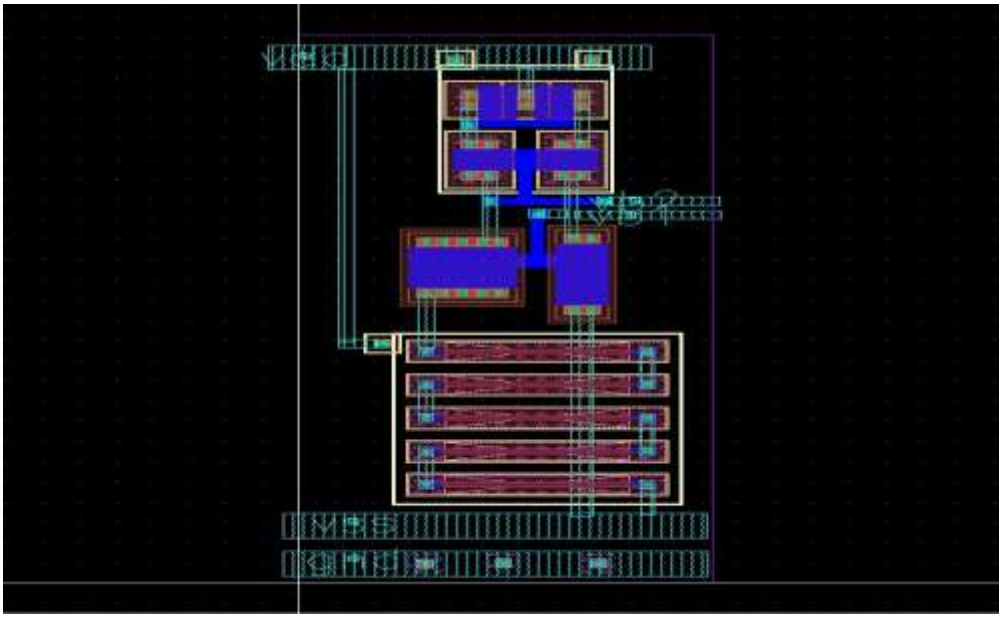

Figure 8: Op-Amp RC extracted view

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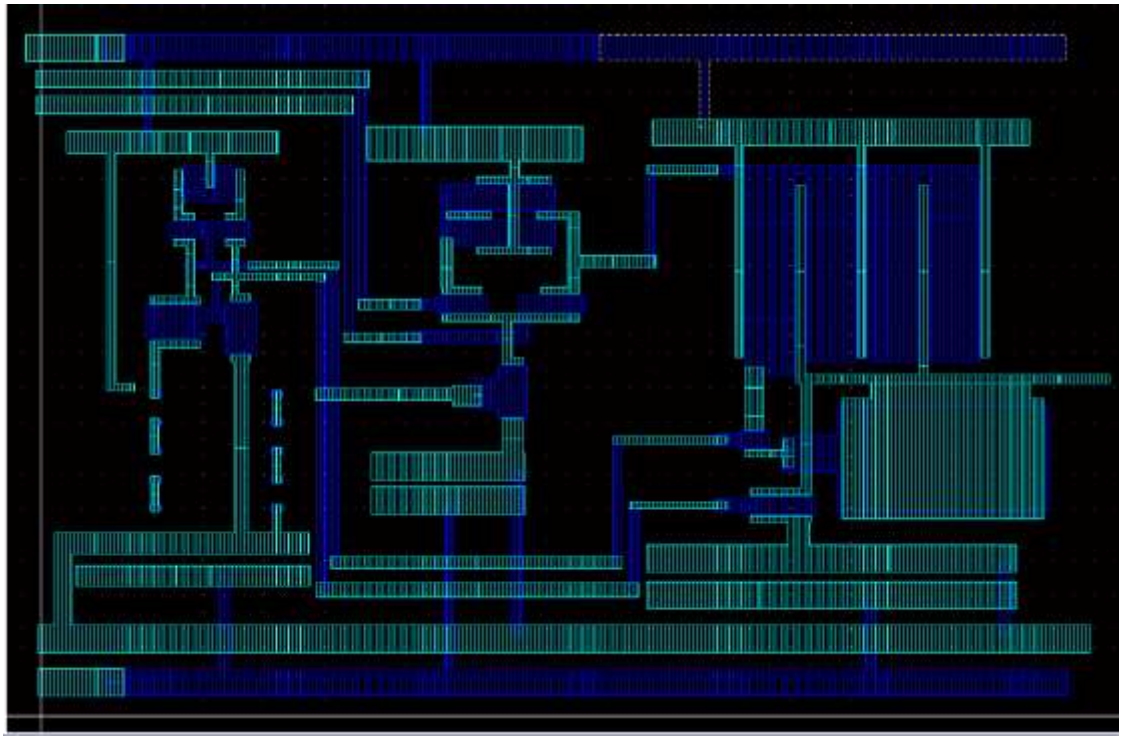

Figure 9: Op-Amp RC extracted view

VI.CONCLUSION

The proposed design has been able to satisfy most of the specifications provided for the op-amp. The proposed op-amp is a two stage single output op-amp. The input stage is a differentialamplifier and a common source stage forms the second stage of the op-amp. The layout of thedesign has been made and simulated. The post layout simulations abide by the given specification. The entire design has been done in UMC 180 nm technology. The gain of the op-amp can be increased further by the use of cascade device in the input stageThe voltage swing may be increased by using a double ended output.

Table 1: Observations for low power op-amp with supply 1.8v

Parameters	ecification	Simulation Results before layout	Simulation Results after layout
Gain	10 V/V || 20 Db	12 V/V || 22 dB	10.2 V/V || 20.4 dB
3-dB Bandwidth	20 kHz.	397 kHz.	200 kHz
UGB	N/A	4.6MHz	2.165 MHz
CMRR	>50 dB	80dB	64dB
PSRR	N/A	84dB|59dB	87dB|60dB
SLEW RATE	10 v/µs	25 v/µs	12.47v/µs
POWER DISSIPATION	1 mW.	0.9 mW	0.6 Mw
Output Offset Voltage	N/A	-600 mV	-600 Mv

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