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Machine Learning Integration in Semiconductor Research and Manufacturing Pipelines

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Abstract: Semiconductor manufacturing plays a critical role in modern industry. With the rapid growth of this field, semiconductor companies are challenged in both R&D and manufacturing domains. However, the increasing complexities of devices, structures, materials, processes, and even changing physical models pose great challenges for both modeling and computation. In addition, the growing amount of data and the large number of people involved in the R&D, design, and fabrication of semiconductor components complicated the production systems and slowed down the overall throughput. For the R&D and production of semiconductor devices with advanced technology nodes, the integration of Physics-based modeling, Computer Aided Engineering tools, parameter optimization, and Machine Learning methods constitutes a new vector for promoting innovation and productivity in the semiconductor industry.

Machine Learning methods empower automated, efficient, and intelligent solutions for semiconductor modeling by modeling data with Non-linear regression, Principal Component Analysis, clustering, classification, and generative methods. Physics-based regression methods such as Fourier Series expansion and Polynomial Chaos are established to establish neural networks for topology optimization, sensitivity analysis of processes with uncertainty quantification, inverse characterization of materials, and accelerated simulation. Reinforcement Learning tools have been successfully developed for the early-stage optimization of processes and design. Meanwhile, Deep Learning-based tools such as Generative adversarial networks and convolutional neural networks have been developed for the design of structures/gate layouts and the qualification of patterns.

On the other hand, modern semiconductor manufacturing consists of multiple departments with complex production systems. Significant efforts have been made on modeling layout storages and new equipment selection to optimize the bi-objective cost and yield in extreme scale layouts. Mathematical programming, agent-based models, and Reinforcement Learning methods have been proposed to optimize the scheduling of diverse wafer processing flows and streamline interactions at the Fab level between manufacturing equipment, input/output, and cost. Moreover, after a decade struggle, advanced Process control systems in conjunction with on-line monitoring monitors critical sensors and control actuators to solve quality issues on time. These large-scale systems save resources and improve quality at the cost of higher complexity. Process data analysis and fault detection methods such as Fourier analysis and kernel-based methods have been established to model non-linear propagation of disturbances and forecast machine states for predictive maintenance.

Keywords: Machine Learning, Semiconductor, Research, Manufacturing, Automation, Predictive Modeling, Process Optimization, Defect Detection, Yield Improvement, Data Analytics, AI in Semiconductors, Fabrication, Smart Manufacturing, Quality Control, Industrial AI

I. INTRODUCTION

The semiconductor industry is one of the most technology-evolving market sectors. Since the inception of the semiconductor industry in the past century, many era-defining technologies have emerged, from wireless phones to extended reality. To catch up upgrading technology and ensure product compliance, semiconductor manufacturers have to invest huge capital in new fabrication equipment or improve the process of existing equipment, which is a challenging task due to the complex production environment and investment risk. As the sizes of devices decrease, the results of manufacturing processes are dimming harder and harder. Even slight deviation is enough to complete the failure of devices and ruin billions of business losses. It is crucial but difficult to control the performance of the manufacturing processes and ensure the yield of production lines [1]. To improve the product yield and reduce costs, effective inspection and metrology are necessary to identify and eliminate defective products. Since constructing a perfect wafer model is theoretically possible but practically very difficult, many semi conductor manufacturing equipments are equipped with sensors. Those sensor data can be used to detect drill holes, where the fabrication process is malicious, without taking any additional cost in the expense of volume and time. Because of the high dimension and the nature of physical processing, it is a challenge how to effectively model, interpret and utilize the sensor data.

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Many analog and digital linear models have been proposed to detect holes, but the complicated structures of these models limit their performance and generalization. As a result, a mechanism that can model the complicated relationship between the sensor signal and the resulting inspection measurements is needed [2]. Thanks to its unparalleled strong ability in non-linear function approximation, machine-learning technologies have been successfully applied to detect holes. However, it is a pity that in traditional data-driven hole detection methods, the whole task works as a black box and the modelling process is unexplainable.

II. OVERVIEW OF SEMICONDUCTOR INDUSTRY

In terms of revenue, the semiconductor market was valued at USD 575.49 billion in 2022 and is expected to reach USD 1,000 billion in 2032, expanding at a 5.2% Compound Annual Growth Rate (CAGR) from 2023 to 2032. The semiconductor industry is one of the most capital-intensive and technology-evolving markets. As technology nodes shrink and new design technology pushes for higher yield and quality, the cost of inspection, metrology and computational resource continues to increase significantly [1]. The earliest era of semiconductor metrology utilizes laboratory tools and off-line measurements, which do not provide real-time process information. Instead, the industry turns to various types of in-line metrology to acquire real-time monitoring of the production, which is the key in keeping up with fast pace of semiconductor manufacturing. For example, various dimensional measurements are needed at the silicon fabrication stage to ensure the defect-free and robust devices. Measurements of etch depth in nanoscale FinFET or capacitance in dual work function MIM Cap is highly demanded in data exploration or yield improvement [2]. With technology advancement,

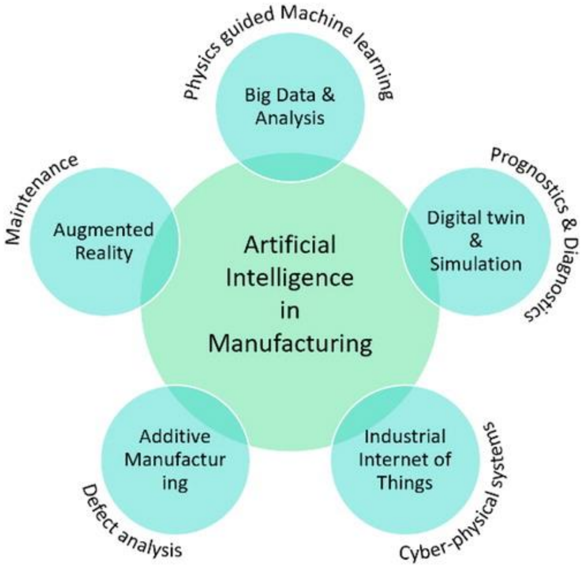

Fig: 1 Full article: Machine learning in manufacturing

metrology tends to provide footprint insensitivity rather than dimensional information. More information regarding masks and processes are fused into a single-measures approach. Effective inspection and metrology are critical to improve product quality, increase yield and reduce costs. Current physical-based approach needs ample parameter tuning and is not efficient for metrology. Moreover, there is a tradeoff between speed and accuracy. Machine-learning methods can address the visibility and speed issues. However, they either employ limited input data or have expensive prediction time. A soft sensing regression framework is proposed based on deep learning to predict metrology measurement based on sensor measurements which can help overcome the issues in fabrication testing scheduling. The framework consists of a sequence of steps including data collection, preprocessing, training and evaluation. The synthetic and real-world case studies show the effectiveness and efficiency of the proposed framework in predicting metrology with high quality.

III. MACHINE LEARNING FUNDAMENTALS

Machine learning (ML) is a zoom-in section of artificial intelligence (AI) methods. Traditional AI, which is rule-based, requires expert knowledge or engineering knowledge to identify specific models to describe the relationship. ML, which aims for a data-driven approach, learns the association from available data and spits out "black-box" models that are hard to interpret but are capable of accurate estimation of any range of value. The literature on ML applications in the semiconductor field has grown fast in the past few years [2].

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Various ML applications in chip design, manufacturing, and test flow have been reported. As for ML in semiconductor processes, modeling tasks that were previously done by experts are now being handled automatically without engaging human expertise and know-how [3]. This explains how ML promotes the development of manufacturing techniques, gives more insights into existing processes, and thus helps in fixing or improving them. These are all important steps to minimize the time to successful and accurate design and eventually manufacturing.

IV. APPLICATIONS OF MACHINE LEARNING IN SEMICONDUCTOR RESEARCH

With the advancement of technology, the complexity of modern designs is increasing at an exponential rate. The semiconductor industry's continuous race towards smaller feature sizes is facing significant challenges. Traditional model-based simulation and verification approaches often fail due to the underlying mathematical complexity of the add circuits. Hence, there is a pressing need to develop and deploy efficient ML algorithms for semiconductor design and manufacturing, such as layout and physical design prediction, analog circuit characterization, and fault detection and diagnosis [2].
ML has found its applications in every key step of design, viz. schematic generation, placement, and routing. Physics-aware neural networks trained using field equations and solvers are introduced for analog circuit layout prediction. With respect to semiconductor technology, ML utilizes different aspects of technology development time, such as the rapid development of meta-models to predict behavior of complex structures. Trained in the design space of oxide thickness, inner resistance, and gate capacitance, provides immediate signals without the need for time-consuming slow simulations.

Eqn.1:Support Vector Machine (SVM) Decision Boundary

$$f(\mathbf{x}) = \mathbf{w}^T\mathbf{x} + b$$

- Classification is determined by the sign of $f(\mathbf{x})$
- $\mathbf{w}$: Weight vector, b: Bias
- Used for defect classification or material property categorization

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Recent developments in ML methods for nondestructive semiconductor circuit fault detection and diagnosis by using information obtained from different sources like electrical signals. One of the challenges faced by the semiconductor industry is the increasing test time of integrated circuits. Adaptive test and machine learning methods to address the high test cost of complex circuits. In addition to its use in testing, which detects the product quality of a manufactured circuit. It can also be applied to a variety of semiconductor devices, in the area of wafer testing or in assembly testing. With the machine learning, methods can be applied to improve product reliability and yield directly as well as indirectly.

4.1. Data Analysis and Pattern Recognition

Wide analysis based on machine learning classification algorithms has been done in semiconductor wafer defect classification [4]. The defect maps produced by inspection tools indicate whether a defect has been detected. This quality assessment primarily aims to obtain optimal yields in the front-end of line (FEOL) process offerings in semiconductor fabs. As the most mature applications of machine learning in semiconductor wafer defect classification [1], especially addressing advanced technology nodes, this refers both to input defect map representations and machine learning-based classifying algorithms. This survey has presented a detailed framework for categorizing wafer defects algorithms and includes empirical evaluations to measure the effectiveness of different machine learning approaches on public defect datasets. This survey focuses on empirical works on machine learning-based classification of defect patterns on wafer maps in this field review.

Experts have designed multiple machine learning classification techniques to identify defect patterns in wafer maps based on those features. To evaluate the strength of different algorithm categories, three selection techniques of all algorithm categories have been examined on both the IEEE and AIM 2015 datasets in this survey. It has been found that the Convolutional neural network (CNN)-based classification is superior to others on both datasets. This research has also revealed that a larger dataset provides more representative samples and enhances the performance of machine learning. Hence, it is suggested to create a larger dataset by involving domain knowledge for better classification accuracy.

The results demonstrated that deductive approaches achieved more accurate and robust inspection results than the inductive ones. The non-linear enhancements adjusted more promising inspection thresholds than their linear counterparts.

The maximum deviation still indicating a consistent yield projection was improved, in equivalent visual inspection time. This paper is potentially relevant to the field since it examined the state-of-the-art approaches in machine learning applications to semiconductor wafer defect classification, identified opportunities for future work and experimental findings, and advocated for developing a tool to assess existing data-labeling algorithms, detailed workloads, and impacts.

4.2. Predictive Modeling for Material Properties

The understanding and manipulation of material properties is essential for addressing grand challenges in semiconductor research. Recent advances in the field of Machine Learning (ML) have produced predictive models of material properties on the basis of chemical structure. Consequently, there is wide interest in applying such ML models in the semiconductor domain. Semiconductor materials exhibit unique electronic and optical properties that stem from the material's local atomic structure. Importantly, this rapid predictive model agrees with traditional physics-based models within the limits of partition function approximation. By varying model degree and kernel width, computer prediction accuracy can be fit to within 20% of classical approaches on the bulk of the test set. Moreover, the ML approach can be cast into Local Density Approximation (LDA) formalism and incorporated into traditional semi-empirical methods of molecular orbital theory for quantum dynamics. Where necessary, the KRR concept can be readily generalized to a range of standard ML techniques and further adopted for prediction of other materials properties including organic photovoltaics and thin-film transistors (TFM) [5].

4.3. Simulation of Semiconductor Processes

The semiconductor manufacturing process involves many steps, sequentially changing the physical and/or chemical characteristics of a silicon wafer for the formation of integrated circuits. During the CMOS (complementary metal-oxide-semiconductor) device fabrication process, various physical and chemical processes, such as oxidation, thermal treatments, etching, doping, dielectric deposition, and photo-lithography, occur repeatedly and in a complex manner. Continuous reduction of the scaled CMOS technology node enhances the chip's capability but causes severe manufacturing and yield issues [6].

The difficulty lies in the fact that there are many chemical reactions and multidisciplinary knowledge is necessary in semiconductor manufacturing procedures. To use analytical approaches in chemistry and physics to model semiconductor processes and their relation to device characteristics, the results are often away from experiments. With the rise of machine learning, it becomes more feasible to use algorithms to describe the complex relations between semiconductor processes, such as etching, deposition, oxidation, wafer cleaning, and lithography, and semiconductor device characteristics.

Electrostatic compatibility of nMOSFET and pMOSFET in a complementary structure is an overall criterion for the well-functioning of a transistor at full process yield. It is desired that the electrical characteristics of a MOS (metal-oxide-semiconductor) device should be controlled by the bulk, not by the interfaces. By analyzing undesirable charges present in the interface, capacitance-voltage characteristics help in determining stability and overall performance. Thus, it becomes important to study the process parameters influencing the electrical characteristics of devices. As transistors shrink and the process becomes more complex, there are more process steps in semiconductor manufacturing, making it difficult without regression or machine learning. The best modeling technique for the semiconductor industry is to mix the idea of ideal physics with machine learning algorithms. The efficacy of supervised learning is very high but comes with the requirement of a large amount of labeled data.

V. MACHINE LEARNING IN SEMICONDUCTOR MANUFACTURING

The rise of machine learning (ML) in semiconductor manufacturing is fueled by the industry's movement toward "smart manufacturing" (SM) and the proliferation of tools that generate large volumes of manufacturing data. In semiconductor foundry processes, to be data-driven using advanced ML/AI methods, one has to answer many questions and select suitable methods based on the data structure, data characteristics and distribution, and process understandings [7]. Otherwise, existing classical methods can often be more effective. With the introduction of the open-source libraries in Python, it is easy to apply advanced methods to solve problems but can also lead to disasters when results are misinterpreted. Thus, the balancing of suitability and effectiveness has broad academic and industrial appeals.

Deploying ML methods at a fab/technology node level faces hurdles, including extensive data preparation tasks, method selection and parameter tuning, and the fast turnaround time required for most applications. There are numerous choices of ML methods, corresponding parameters, and data preparation methods available in the open-source libraries. The search space for data preparation and modeling methods can grow exponentially or even beyond.

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For managers, especially not data scientists, it is practically impossible to explore a plethora of methods and make informed decisions in a timely manner. This creates a substantial barrier that hinders the use of ML and prevents rapid exploration of new modeling methods or features that result from technology node improvement. Tutorial and education materials can help, but they cannot fully mitigate the issue. The current practice is to hire more data scientists, compromising the “smart” aspect of SM. Another challenge is that most of the current ML methods lack explainability. Supply chain consideration can complicate the privacy of the data and the decisions based on it. Even if one adopts expensive-to-build complex methods, their decisions can possibly be a “black box” to the distribution owner, preventing their adoption in the industry and worse, resulting in distrust [2].

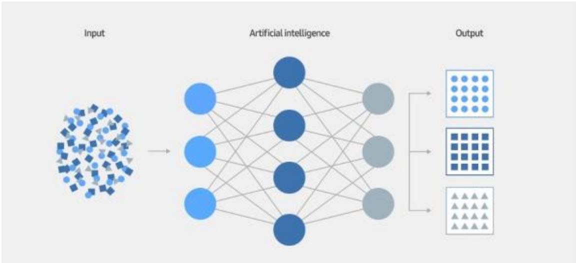

Fig: 2 Machine Learning is Revolutionizing Semiconductor

5.1. Process Optimization

The semiconductor industry is characterized by fierce competition, with extreme pressure in yield enhancement. For example, a 1% increase in yield in an advanced logic wafer fabrication facility (fab) could result in an estimated 150 million USD additional net profit. With extremely high gate counts in integrated circuits, there are hundreds of process steps designed to avoid defects in chips. However, sophisticated and expensive process steps, coupled with variation in materials and machine states, can lead to defects, so it is critical to analyze the contribution of process steps to the overall yield loss [7]. These additional processes could later be fine-tuned in lots deemed problematic for yield enhancement, before further probing the first-principles nature of the mismatch.

In tackling yield enhancement problems, machine learning (ML) techniques are being increasingly adopted. Basic techniques, such as regression techniques, correlation analysis and tree-based feature selection, can be used to analyze critical process steps in terms of their contribution to overall yield loss, and as initial inputs to yield enhancement strategies. In another sense, data mining techniques, such as k-means and hierarchical clustering, can be used to assist process scientists in troubleshooting and process optimization, by developing a better understanding of the data and the relationships in data space [8]. Most important in yield monitoring are anomaly detectors that can be used in conjunction with a myriad of standard ML algorithms to detect, with a high detection rate, potentially problematic process steps in complex manufacturing processes, and to minimize false alarms, often due to common causes affecting multiple sites. There are attempts to automatically classify or classify defects detected in earlier inspections, while avoiding the tedious work of manually categorizing the defect types.

5.2. Quality Control and Defect Detection

Quality control is an essential focus in the semiconductor manufacturing industry as some defects on a Wafer (WFR) may affect yield and functional quality of Integrated Circuit (IC) during measurements of post-processing. Wafer defect detection and monitoring of foundries are currently performed manually. This paper surveys existing methodologies which utilize completely supervised ML classification techniques for identifying and classifying WFR defects in Semiconductor fabrication. From the engineering perspective, WFR defect detection is an issue of designing a computer-aided system that is able to classify defect types and to distinguish defective WFR images from non-defective ones. However, from a pure computational perspective, the problem is regarded as a given set of dataset consisting of N sample images of WFRs, where each image is represented as a feature vector $\in$ 134*134 with each dimension representing a pixel from the 134x134 grayscale image. Then decoding the embedded information and meaning from the given dataset, to classify the images into K different categories is a challenging yet interesting task in the field of AI. A holistic view of computer-aided approaches for WFR defects classification is presented including defect classification fundamentals, defect templates with wafer defect and classification algorithms.

Machine Learning (ML) is widely adopted in manufacturing as the fabrication of ICs is increasingly automated. Process equipment, Automated Material Handling System (AMHS), and many other tools collect an enormous amount of data. Data generated at each step can be historical, real-time, semi-structured, or unstructured, increasing the need for advanced data intelligence applications.

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Failure events that result in rework and/or production loss account for billions of dollars, and significant engineering efforts in the semiconductor manufacturing industry. Data-driven failure analysis has been essential in understanding the root causes of key defects. This paper proposed a novel quantile online learning approach screening and analyzing failures that can be adapted to chips of different technologies. The proposed approach has established quantile representations of features through recursive computation and learned from aggregated data efficiently. The results of four different case studies are affirmed that wide-scale deployments of the approach are feasible. Moreover, the proposed approach outperformed existing approaches, and great efforts can be made toward failures' root cause analysis [9].

5.3. Yield Improvement Techniques

In the semiconductor industry, yield enhancement is a pivotal concern, with direct consequences for cost efficiency and market competitiveness. The chance to enhance yield has emerged as a pivotal lever to curtail costs and amplify financial returns. In advanced logic wafer fabrication facilities (fabs), a mere 1% increase in yield can translate to a substantial $150 million in additional estimated net profit [7]. Hence, considerable efforts have been devoted to yield improvement knowledge in the field, including yield modeling and process optimization.

Machine learning (ML) has been increasingly employed to augment yield enhancement strategies in recent years, such as analyzing critical process steps by feature selection, assisting in troubleshooting and process optimization by data mining, detecting the potential cause of anomalies by clustering algorithms, and automatic defect classification. There is an opportunity to fundamentally improve product yield by partially or fully replacing expert knowledge and labor-intensive data analysis work with ML models. Unfortunately, despite the exhaustive development of these ML techniques, the exploitation tends to be uneven. Much of the methodology exploration is relegated to internal machine learning teams, while front-end users remain largely unaware of the cutting-edge ML techniques developed in-house and hitherto employ only traditional statistical methods.

Eqn.2:Neural Network Layer Output (Feedforward Layer)

$$\mathbf{a}^{(l)} = \sigma\left(\mathbf{W}^{(l)}\mathbf{a}^{(l-1)} + \mathbf{b}^{(l)}\right)$$

- σ: Activation function (e.g., ReLU, sigmoid)
- $\mathbf{W}^{(l)}, \mathbf{b}^{(l)}$: Weights and biases of layer l
- Used in modeling nonlinear processes in semiconductor fabrication

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There is an inherent trade-off in semiconductor smart manufacturing (SSM): how to speedily adapt findings to ever-more-challenging throughputs while constantly striving to architect R&D models for accuracy. On top of that, even though the essence-derived objectivity knowledge in the form of ML models might be transferrable across similar problem domains, this widespread "knowledge" transferability cannot guarantee consistency between the inter-domain SSMs where the deployment can be too complex to comprehensively model. Hence, it is crucial to develop measures to quickly adapt to changes, improve product yields, and optimize resource utilization to enable intelligent, efficient, and responsive operations.

VI. CHALLENGES IN IMPLEMENTING MACHINE LEARNING

ML models require a large amount of training data to learn the underlying structure of the data. This data needs to be collected exclusively from specific manufacturing processes to identify some previously unseen parameter sets. However, data is not always feasible to collect for these processes. Therefore, combining this with the availability of new fabrication processes and tools, the community has accepted the transferability of ML models trained on small amounts of synthetic data as much more logical and efficient job assignments compared to the task and data-based transfers [2]. Moreover, ML has gained prominence in the semiconductor industry with the proliferation of smart devices. In the industry, there is an exponential growth of text data generated from recalls, replacement parts, and technical documents, along with the advancement of various ML techniques. Novel technologies in graph-based deep learning, NLP have emerged to make sense of this massive volume of data. The data are rich in discovery and decision-making in future products under new conditions, roles and utilizations of graph and text data, engineering challenges in exploiting new data forms, and data-driven methods. At a semantic level, the relationships between semiconductor technologies and fabrication processes are described as attributed graphs obtained from correlation tests. The parameters of chips data correspondence to functions are additionally encoded into two kinds of text attributes. The detailed recovery map is presented, including nodes, edges, and attributes of multiple semantically well-defined data items in heterogeneous forms and different characters.

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Data cleaning stores the acquired semantically rich data into a graph and text store. On top of the storage system, data-driven methods are proposed. As a result, semantic graph and text mining methods are applied to enable the recovery of semiconductor technologies and processes. This method is a novel approach to multi-modal semiconductor data processing, which can provide the data to structure for future studies in intelligent chip design and test. This also can be extended to other industries dominated by heterogeneous data for decision-making and discovery.

6.1. Data Quality and Availability

Current highly advanced chips are increasingly being fabricated on a few nanometer technology nodes due to a plethora of computing and processing applications in artificial intelligence, machine learning, deep learning, Internet of things, etc. To keep pace with technology development, conventional semiconductor manufacturing processes and inspection methodologies have stretched their limits and require breakthroughs. Process engineers and yield teams are virtually flooded with huge amounts of high-speed multi-modality data related to manufacturing equipment and processes, as well as outputs. A special infusion of smart manufacturing in semiconductor manufacturing through the frontier of artificial intelligence (AI) techniques, particularly machine learning (ML), will hasten the pace towards manufacturing democratization and sustainability [9].

Machine learning (ML) applications in semiconductor manufacturing have been referred to as an emerging interdisciplinary field. Specifically, academic research and industrial applications of ML/AI techniques in semiconductor equipment, processes and yield advancement, and the ensuing challenges and opportunities are discussed. The paradigms of ML techniques, problem formulation, data requirements, and model interpretability and explainability in manufacturing settings are reviewed. State-of-the-art designs and practical value-added solutions in manufacturing within ML/AI frameworks are then presented. It is broadly categorized into five groups: defect detection, classification and recognition, process control, monitoring and predictive maintenance, and yield prediction improvement. New frontiers and new normative benchmarks for broader and deeper intelligence in chip factories and surrounding supply chains are discussed.

6.2. Integration with Existing Systems

Integration with existing systems can benefit from machine learning techniques for improving testing and diagnostics of integrated circuits (ICs) and boards. A defect in an IC is normally detected using prescribed test vectors, the test outcome (pass/fail) is analyzed and many test approaches exist. However, as integrated circuits evolve and the test patterns increase, it has become a tedious task to analyze these test outcomes to diagnose the faulty nodes. Various ML-dedicated studies present methods to enhance the test accuracy and efficiency for ICs on a die and ICs on a circuit board [2].

A matrix-based method that can classify the good devices from the defective devices with high accuracy. The developed method, named Adaptive Test Pattern - Class Based Approach (ATPCBA) is trained over a small fraction of good and defective devices to extract the fault-free response and fault-response patterns respectively. It has observed high levels of diagnosed non-faulty devices with less than 2% of the un-classified devices over other matrix-based ML methods. A device may be faulty too but the test input set may not be adequate to excite a fault or the single fault is masked, then the device appears as the good device (false-non-faulty device). A low-cost multi-stage ANN based ILT method to achieve high test quality on semiconductor chips, even with a reduced test set beyond the full observability condition has been developed.

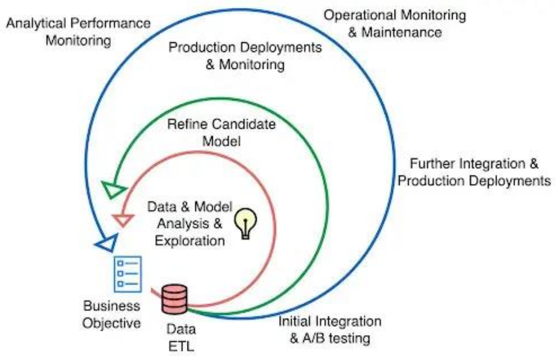

Fig: 3 Build an End to End ML Pipeline

Prior studies employed different Machine Learning or Deep Learning based approaches to enhance quality of scan chain diagnostics as well as the overall testing quality of semiconductor components.

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In general, design-for_test capabilities make use of different scan methodologies to aid test generation under the assumption that the device under test (DUT) has been designed for testability.

6.3. Skill Gap in Workforce

There exists a risk that introduction of automation will lead to elimination of jobs, and that AI will substitute the workforce entirely. Although automation has already taken over many jobs in manufacturing, reasoned position must be taken. Certainly there is a threat at lower human interactivity tasks. However, likewise IT, AI is an enabler of new use cases and reveals vast job opportunities in fields related to AI. Need for competent workforce is soaring; capabilities such as engineering, ability to analyze/interpret big/complex data, and creativity are vital assets in the wake of AI deployment. Even now, there is a strong shortfall in AI-related experts and professionals worldwide [8].

Demands for re-skilling and up-skilling are ubiquitous and must be pursued on multiple levels. Creating basics of programming must be compulsory in all education systems (including elementary school), even if just to understand how automation, IoT, machine learning, etc., work. Hand-on practices must be preferred over mere theoretical lectures. Formation of a domain-specific development ecosystem to get engineers vs. unaware IT-people along with consortiums of semiconductor, AI, cloud-IoT mentors must be facilitated. In the industry, educational channels access to expandable resources must be offered to employees on their own account to widen their expertise. Combine these resources with topic-explicit booklets and online community boards, and give public recognition to experts building the ecosystem to establish career development for volunteer experts. It is also extremely important to successfully pursue the same goal as the public education system for general public. Which would help tackle the upcoming labor market shift beneficially.

VII. CASE STUDIES OF SUCCESSFUL INTEGRATION

The integration of Artificial Intelligence and Machine Learning brings both opportunities and challenges, with successful case studies demonstrating the potential for innovation, product development, and improved performance. Notable advancements have been made in manufacturing, inspection, and test equipment, semiconductor fabrication processes, and design automation during early research and construction phases. These successes showcase a variety of methods applied to historical problems in every stage of semiconductor technology scaling, as well as new issues targeting post-CMOS technologies. This survey identifies many examples of successful and widespread implementations that continue to provide significant cost and performance improvements [2].

These success stories involve various AI/ML methods, including but not limited to supervised learning with deep neural networks for highly accurate pattern recognition or regression, unsupervised learning with generative adversarial networks to produce and label signals or images, reinforcement learning for task-oriented control and optimization, and heuristic search to guide existing procedures. There are success stories at both system and algorithm levels, involving pure AI/ML applications as well as traditional modeling and optimization approaches that incorporate AI/ML components to improve performance. The case studies are categorized by semiconductor design and technology domains, with each category broadly grouped by supply chain stages. The foundation domain covers design technology and EDA tools applicable to both IC circuit design and semiconductor fabrication process design [7].

A pivotal concern in semiconductor manufacturing is yield enhancement, which has direct and linear consequences for cost efficiency and market competitiveness. The cumulative investment for semiconductor manufacturing by the 15 largest semiconductor foundries exceeds $200 billion annually, and the cost of fabrication equipment consumes 56% of wafer fabrication cost. Equipment, material, and tool makers achieved a record-high gross margin of 26.9% in 2020. For logic wafer fabrication facilities (fabs), a 1% increase in wafer yield can generate an additional estimate net profit of $150 million other than die yield improvement. There is great interest from both industries and academics on yield enhancement. It is a study field of signal process, data acquisition, and applied statistics which pedagogically reveal nature properties of wafer processing under profiling.

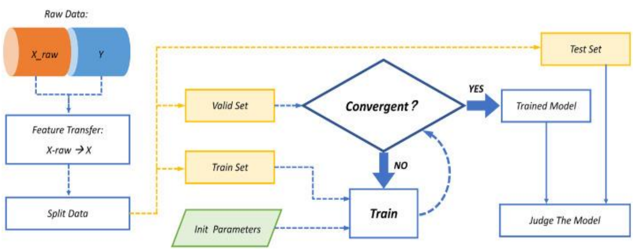

Fig: 4 Machine learning for semiconductors - ScienceDirect

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7.1. Leading Semiconductor Manufacturers

This chapter introduces a few leading semiconductor manufacturers and delves deeper into the state-of-the-art achievements of machine learning in semiconductor fab research and manufacturing. The most powerful semiconductor researchers worldwide are conglomerates with diverse imaging. Intel, founded in 1968, is headquartered in Santa Clara, California. It is the largest semiconductor manufacturer and a highly advanced chip designer worldwide. However, Intel is struggling to solve its simulation model as simulation efforts have become extremely difficult. Simulation efforts are too large, with too many components, inputs, and parameters, and cannot be maintained based on first principles alone. A global best for the simulation model does not imply local bests, and small perturbations in inputs or parameters lead to drastically different outputs, further complicating the solution process of working with neural networks. Taiwan Semiconductor Manufacturing Company (TSMC), founded in 1987, is headquartered in Hsinchu City, Taiwan. It is the first foundry to separate manufacturing facilities from design firms. As the technology leader of foundry services, TSMC has been more successful than its competitors in the past years. Achievements include collaboration with substrate suppliers to make the manufacturing process of the 2.5D package more cost-effective, fast-changing demand patterns in early 2022, extended lead times in procuring silicon manufactured on older generations of technology, and a record of 22 weeks of wait per order in October 2021. Samsung Electronics, founded in 1969, is headquartered in Suwon, South Korea. It manufactures semiconductors and memory. Samsung Electronics is a leading company in DRAM and flash memory fabrication. Recently, it has expanded investments in logic fabrication and is now regarded as TSMC's fiercest competitor. Samsung is a pioneer in 3D memory technology and asserts to fabricate a 3nm FinFET Logic Process by the end of 2022 [8].

7.2. Innovative Startups

A number of innovative startups are also carrying out research on applications of machine learning in semiconductors by targeting design, process, and test, some of these include:Lattice, Inc. is an automation software provider that widely employs AI techniques in semiconductor development and manufacturing across design, DFM, and DFT. Case studies presented include outlier screens, fault library generation, fault simulation acceleration, and model gain and verification [2].Cerebras focuses on building chips and systems, highly optimized for deep learning that leverage existing deep learning libraries.Tellyn also develops IC verification software and framework employing AI technique. Case studies include automatic generation of gate-level formal verification assignments and automatic generation of standard-cell library abstraction views.Perception and AI is engaged in semiconductor failure analysis employing ML techniques such as video processing and classification.Nabto is described which provides machine learning-based software built on an edge-first approach for rapid AI acceleration, and solutions for deployment at the edge.Sorcera also works on ML-based software in IC R&D. Applications include training failure prediction for foundry manufacturing and AI acceleration across test engineering gate-repair and answer database.

VIII. FUTURE TRENDS IN MACHINE LEARNING FOR SEMICONDUCTORS

The semiconductor sector is constantly changing. Semiconductor manufacturing goes through several phases, from design to development. All data is transformed into various artifacts. As a result, defining a cleaning standard is tough because various artifacts employ varied data types and wheel formats. Such disparate data becomes a challenge in correlating and drawing conclusions. This issue is resolved through enterprise-level data cleaning. Rather than data cleaning, it is still being discussed at the boardroom table. In addition, data cleaning leads to information suppression, making it difficult to explain decisions. To address information suppression, this section briefly discusses explainability issues.

Wireless communication, autonomous driving, and augmented reality are the three popular topic challenges in the development community. That is because they require a comprehensive understanding of adjacent and long-range correlations, and classification is another critical task for these deep neural networks to identify and mask relevant nodes. In this regard, under-training, small data, and bias problems are significant.

Deep models, like other land-cover predictions based on satellite data, rely heavily on datasets with varied dates and times. They are limited to coarse patterns because different data undergo standard processing, which eliminates fine adjustments. The objective is to let machine learning learn raw data over various time intervals based on physical models and chip designs to detect unknown process patterns. That is very challenging, particularly when confronting fewer pre-trained data-type considerations. Otherwise, a small amount of data must rely on the task's corrective process by reconsidering its ingredients. There is a need for more discussions on standardization, inheritance, and language in the community. This area needs more forum discussions to raise awareness of its importance.

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8.1. Advancements in AI Algorithms

The evolution of machine learning (ML) and AI research is bringing far-reaching changes to many fields of science and technology, including semiconductor research and manufacturing. Advanced AI algorithms and tools are being employed in semiconductor research and development (R&D) to optimize processes. Some of the state-of-the-art deep learning techniques, together with their applications, are summarized here. To improve chip reliability and yield, each design is optimally tuned to consume and dissipate low power, occupy a minimum area, and achieve high throughput with a high-driven topology. Accurate and fast estimation techniques are required during circuit design and modeling to estimate and verify the impact of the process variations on the circuit output accurately. This problem is more pronounced in the nanometer regime with the increased complexity of digital design, where thousands to millions of VLSI components are present in a circuit. Surrogate ML/AI models provide solutions to this circuit design and modeling problem [2]. These models forecast the device performance based on the lookup table created by running the TCAD simulations. Surrogate models can be easily extended to circuit-level and system-level design and analysis. Hence, to improve the turnaround time and yield of ICs, surrogate AI/ML models with industry-specific input features are trained using the internal SPICE and Verilog-A models. Generic surrogate AI/ML models are derived to predict the technology-independent performance of the components based on the process nodes. Surrogate models can predict the circuit performance with comparable speed and accuracy to traditional EDA tools. Various potential risks in advanced silicon nodes can be estimated and analyzed using ML algorithms. ML algorithms can better capture the complex electrical behavior of advanced technology nodes than the traditional EDA tools [10]. Estimation and analysis of the proper behavior of the subsystems are also crucial in IC technology. Learning algorithms can significantly improve the end-to-end performance of the IC technology, promoting a high utilization ratio and high data bandwidth. Memory-based designs on nanometer technology nodes have been becoming increasingly challenging because they are the smallest devices on the chip and are thus affected the most in terms of functionality and yield. AI/ML learning strategies have been extended to the high-level SoC designs. To implement a dynamic high-level digital circuit onto the hardware, a vast network of AI as hardware acceleration is employed to optimize the data path of the design after its initial high-level RTL verification.

8.2. Increased Automation in Manufacturing

Healthcare facilities are looking for AI-based solutions to achieve advanced automation and be more efficient in the fast-creation, high-quality data-driven modeling, exploration, and discovery. AI/ML can be effectively incorporated at several semiconductor research organizations to widen the spectrum of modeling and exploration in the automaton and discovery of newer semiconductor process recipes and materials. In semiconductor applications, ML has already been adopted to create highly automated processes to extract correct circuit behavior and model CAD tools. Over the last few years, the ambition of semiconductor ML has been steadily increasing, expanding its ability to operate on multi-dimensions and wider processes and materials while fulfilling an ever-growing demand. Semiconductor ML is currently dominated by the following research areas.

Robust and Reliable Modeling: Accurate modeling of dependencies is critical in semiconductor manufacturing as essential design specifications can be missed. This can be caused by poor model initializations or parameters or slow drift during fabrication or relays. A robust and reliable model should accurately quantify uncertainties in inputs and outputs and ensure purity and consistency across entire space while enforcing positive values.

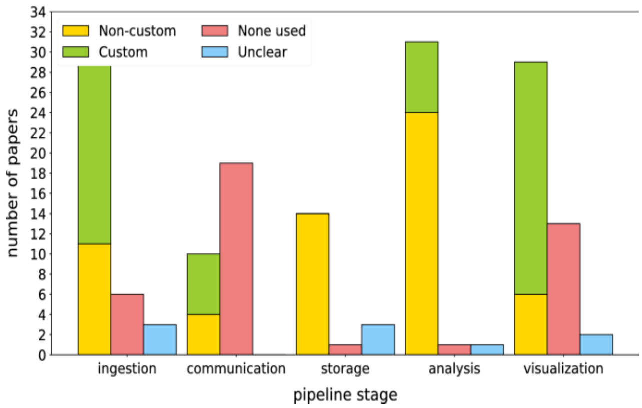

Fig: Manufacturing process data analysis pipelines

Multi-Physics Multi-Domains Modeling: The complexity of semiconductor device and system characterization arises from the unmodeled physical phenomena or coupling between different signal domains. Various model-based detection and diagnostic techniques have been proposed to address the locations and root causes of failures.

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Physics-guided ML and Data-driven Timescale Reduction: Ever-growing circuit complexity has led to the need for acceleration of circuit performance extraction in the simulation signoff flow. Replacing the traditional circuit extractor with ML could cut extraction time from minutes to seconds with equal accuracy.

Parallelism and supereven-RecTablebased Logic Simulators: Supereven-Recurrent Neural Network (SRNN) captures the intrinsic parallelism and time-constraint iterative behaviors of both dynamic threshold logic gates and feed-forward circuits, allowing ultrafast and high-efficiency VLSI. Data augmentation techniques are asserted to mitigate the imbalanced data issue, which is challenging to meet the real-world sensor specifications ([2]).

IX. ETHICAL CONSIDERATIONS

Inherent bias plagues all steps of the machine learning lifecycle, from data sourcing to training to inference. Each of the three machine learning paradigms—supervised, unsupervised, and reinforcement learning—presents its own ethical problems. Supervised learning's challenges involve issues of bias and classification in training data. There is a great deal that is now understood about best practices and ethics for gathering, curating, and classifying labeled data [11].

Well-known examples of ethical breaches in training data range from the questionable provenance of ImageNet and the biases inherent to gender classification systems, both involving large-scale crowdsourcing platforms. Ethical concerns persist post-training in collection and use of inference data, but these are less quantifiable and understood in terms of algorithms and metrics. Finally, a few general-purpose representation and deep learning systems raise novel ethical problems in their vast and widely-used collections of training data. To address these enormously diverse problems, much remains to be done in identifying the key ethical principles and formulating actionable technical and legal precepts.

Bias in unsupervised learning occurs due to the unknown provenance of the training data and an absence of human guidance in interpreting the results. There have been a number of high-profile instances where the outputs of auto-encoders have been discovered to be biased or otherwise objectionable, triggering a controversial realignment of ethical oversight across various organizations.

In reinforcement learning, ethical issues arise due to unknown biases in the environment and rewards, and the need for humans to provide training data as complicated environments and rewards become burdensome. Such approximations can introduce their own biases, leading to ethical problems regarding games designed by companies that may obscure incentives for a player's consumption habits or employing a publicly-traded company to provide the reward for a system that plays its ads.

9.1. Bias in Machine Learning Models

Bias is known to be an impediment to fair decisions in many domains such as human resources, the public sector, health care etc. Bias can stem from various sources such as social bias, cultural bias and bias within the data gathering process. At the same time, machine learning experts warn that machine learning models can be biased as well. Companies have commonly acknowledged that biased training data can lead to biased machine learning models, which in turn may lead to biased decisions being taken [12].

A straightforward definition of bias states that a model is unbiased if it meets some criteria equal to or better than randomly guessing. Although this is a simple definition, it is insufficient as it does not cover all types of bias, nor does it clarify the notion of fairness. For instance, it does not provide a metric to compare different models in terms of fairness. Therefore, it is easy to construct biased models that still meet this definition, provided that one's model of the world is sufficiently simple.

Despite all the known issues, bias testing and auditing instruments are still very rudimentary. Consider for instance the task of auditing an automatic resumes screening system currently employed by a large company. To make such system fair, one has to define fairness metrics and provide a model of the world of further usage. The first fairness metric recommends that, amongst all selected resumes, there should be equal share of both old and young resumes. The model of the world asks for resumes later surfaced to the hiring process to have more standardized layout or some identifying features. With these tools in hand, one can easily check whether results of the initial screening returned an equal share of resumes with respect to age. One can also check whether redundant encodings are present in the text of the resumes returned. The next step then is to consider what role the proprietary machine learning model builds in such process, and how to further inspect for test inputs that deviate from those returned resumes.

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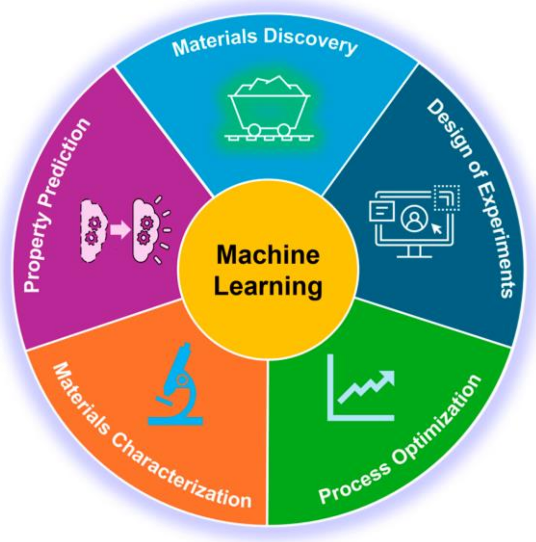

Fig: 5 Machine Learning

Model risk management (MRM) of decision-support models has recently gained traction with the emergence of ML models as decision-support tools [13]. In this domain, the self-governed development and deployment processes of non-bias decision support models are slowly being constructed. However, many of them still rely heavily on abstract modelling languages and do not focus on auditing existing proprietary ML models. Utility Level-Of-Detail-Approaches (ULOD) that describe all decision and machine learning processes by rules, have been presented as enabler of auditing of all arbitrary decision-support advice procedures.

9.2. Impact on Employment

Recent advancements in artificial intelligence and, more specifically, machine learning make it feasible for ML to be leveraged to improve semiconductor research and manufacturing processes and tools. ML will likely lead to significant improvement in performance, cost, and efficiency across a wide variety of tasks throughout both semiconductor design and manufacturing [2]. Machine learning is powerful when dealing with large data sets that are unwieldy, time-consuming, or impossible to analyze by traditional algorithms. Content-Based Image Retrieval and deep learning provide avenues for rapid analysis of images that will likely have useful applications for semiconductor inspection.

Just with other major tech innovations, the introduction of ML will come with disruption. Many jobs will disappear or become drastically redefined. However, just as with the previous examples, new jobs will come into existence, both in quantity and complexity. For jobs that become obsolete or devalued, applicable skillsets will likely become portable to positions in novel high-tech industries, who will be waiting with open arms. Hope is cited that people will find careers that are fulfilling in ways unencumbered by menial and dull tasks.

X. REGULATORY FRAMEWORK AND COMPLIANCE

This paper presents an investigation into AI and ML trends in semiconductor research and manufacturing focusing on applications in semiconductor device and IC design, fabrication and manufacturing, design, process and parametric yield prediction, and in-line process monitoring and defect detection. It concludes with a summary of current regulatory framework and compliance requirements that govern the use of AI and ML in semiconductor research, product design, and qualification [1]. Inclusion of machine learning in IC design environment. Artificial Intelligence & Machine Learning (AI & ML) have been an integral part of business and lives for the past several decades. However, its applicability, usability, and deployment for Semiconductor Research and Manufacturing (R&M) is still being developed.

1. Although design of Information Systems (IS) & technical systems has been with CAD tools and simulators for decades, AI & ML based solutions to speed up the design process has only been explored and applied in recent years. Options of self-learning, self-training, and self-behaviour are not prevalent.

2. First adoption of AI & ML is expected to be in research space on development of Finfets; hence, only later to foundry and turn-key customers. Although AI & ML based design is only recently being discussed, its peer technology of Generative Design has been used from.

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3. Self-learning additionally requires the need for maintaining history and tracks of design decisions, which simplifies huge amounts of data capture and repository needs. Therefore, easy portability with query options from one system to another also adds to complexities. Most importantly, for fully autonomous system even the tool developers do not know how the design worked, making it difficult to understand or troubleshoot failures.

4. Therefore, policies on appropriate areas to apply AI & ML models, information systems, and data capture and maintenance protocols need to be developed and effectively communicated.

10.1. Global Standards for Semiconductor Manufacturing

The expected increase in the number of transistors with a gate length of 10 nm and beyond in the MIPS and the projected ultrahigh-density three-dimensional NAND flash memory having more than 1024 layers call upon the semiconductor industry as a whole including IC and test companies to take into consideration the test time and cost reduction in addition to the signal integrity. The architecture of such new chips is so complicated that the verification of the semiconductor devices and automatic test program generation require a tool kit and EDA applications, but only those are not enough to secure the quality and reliability of the chips within the target cost and time of the IC manufacturers. Furthermore, the advent of artificial intelligence (AI) and machine learning (ML) is expected to significantly impact semiconductor production test and reliability screening in combination with this expecting diversity of the new devices.

Recent research works of universities and test companies on AI/ML algorithms and applications for semiconductor research, IC test, quality assurance, and reliability screening are presented. Trend of machine learning applications and results are organized based on the job types and each application is introduced and explained, while a research and development strategy based on the knowledge and ideas acquired by these collaboration works is also proposed. It is believed that both collaborations and competitions among the hardware and software developers and AI/ML engineers would accelerate the development of devices and applications for semiconductor technologies as well as their convergence onto final applications.

AI/ML algorithms were developed to analyze the results of a test for edge coupled differential signaling (ECDS) signal integrity signal to noise ratio (SNR) for a DDR3 I/O chip. When there is no bit error from the test result, the SNR of more than 20 dB is required. Otherwise the effective input threshold is strongly affected by the output jitter increased from the test board or the chip. The ECDS test result, SNR, is a good data for discriminate IDDQ-tran faults induced by gate oxide breakdown but other stuck-at faults cannot be detected based on the SNR data only. For a defect-free chip, SNR between input and output of the PCB is dropped down from about 31 dB to less than 20 dB for a voltage divider board, which was designed due to the fear of the input HSTL elements being damaged by large values. For the failures detected but not diagnosed, contact timing mismatch and board bounce are believed to be the causes. This can be improved with more state-of-the art test system and such timing fault model [2].

10.2. Data Privacy Regulations

Machine learning is transforming the state-of-the-art in research and manufacturing across several fields and applications. However, the deployment of ML models for these tasks might lead to the collection and processing of private data, triggering the privacy regulations that have been introduced in several countries in the last decades. In particular, the most prominent regulation in this space is the GDPR, which outlines the framework of privacy rights in Europe and imposes several obligations on the data holders. The most relevant regulation for this work is the Data Protection Impact Assessment (DPIA), which must be performed in advance of any processing operations that are likely to result in a high risk to a data subject’s rights and freedoms [14]. In particular, in the case of ML workflows, the regulation explicitly mentions a DPIA where the data being processed is special category data. Moreover, guidelines emphasize that ML models pose a privacy risk, and recommend that such risks are estimated to comply with data protection regulation.

Eqn.3:Loss Function (Mean Squared Error for regression tasks)

$$\mathcal{L} = \frac{1}{N}\sum_{i=1}^{N}(y_i - \hat{y}_i)^2$$

- Measures prediction error during training
- Common in yield or performance prediction models

In this context, a privacy tool named ML Privacy Meter, which helps with compliance with privacy regulation, is discussed. In particular, it is proposed a tool that quantifies the privacy risk to data from ML models by estimating the likelihood of membership inference attacks. The ML Privacy Meter implements several algorithms to estimate the membership inference risk to data from a ML model.

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The metric it returns represents the likelihood that the data used to train the model could be inferred from its outputs, and a higher score indicates a higher likelihood of successful inference. Moreover, as membership inference risk to training data largely depends on the model architecture and training procedure employed, it is recommended to deploy different versions of the model and run the tool on each one. These scores would indicate the ML Privacy Meter's results are model-dependent, and it is hence necessary to keep this into account prior to deploying an ML model [15].

XI. COLLABORATION BETWEEN ACADEMIA AND INDUSTRY

Research collaborations between semiconductor industries and academic or research institutes are encouraged. MoUs can be signed to jointly carry out R&D projects, develop models and methodologies for upcoming devices/technologies, explore ML applications with focus on semiconductor domains, design custom data generation, and testing flows for new devices and technologies, etc. This momentum needs to be continued to explore ML applications in semiconductor domains [2].

Major semiconductor industries in India can create ML/AI R&D Centres of Excellence to sponsor targeted projects at academic/research institutes for focused research addressing specific issues, effectively discarding the noise from diverse ML projects. Successful completion of such projects need to be further promoted for translation to the industry with partner industry personnel's involvement. To ensure smooth project executions, institute staff ailment with respective industry partners should be encouraged. This has a double-pronged impact; it leads to the transfer of valuable knowledge in both sectors, thereby decreasing the R&D gap between them, while also ensuring that the project is executed within the company's expectations.

Research applications of ML in semiconductor domain must percolate at the engineering/DFT engineer level. To achieve this, research findings must be presented in such a way that the layman in the field of ML understands the value proposition for the respective industry. Businesses need to trust the performance of ML applications and this will increase with ML's adoption in everyday applications across different sectors, possibly addressing foundational issues. Success stories from diverse domains need to be elaborately presented to industries for knowledge transfer on exploring ML applications.

11.1. Research Partnerships

The semiconductor ecosystem is large, highly interconnected, and very diverse with broad global participation in research, development, design, and manufacturing. Semiconductor components and systems have had a major positive impact on human life and technological evolution over the past 60 years. S2C provides a set of insights into the engagement between the AI/ML community and the semiconductor ecosystem, including machine learning in semiconductor research, manufacturing, and education, as well as practical actions to extend and improve this engagement. Engagement opportunities in semiconductor research, manufacturing, productization, and education/execution are envisaged. Practical strategies to extend current AI/ML in semiconductor partnerships along with considerations, resources, and development status are also provided. The semiconductor ecosystem involves many stages, e.g. design, fabrication, assembly, test, and packaging. Levels include device, transistor, circuit/architecture, design system, and integration/platform. Today's semiconductors process billions of transistors and go through 20-30 stages before being packaged and shipped. Industry standards provide a common interface for inputs and outputs. At multiple levels, research schools explore foresight, digital twins, and new architectures. Similar to the semiconductor community, AI/ML research is also diverse and multi-leveled, with opportunities at multiple levels of the semiconductor research ecosystem. A successful initial collaboration centered on exploring early-stage design of FPGAs using deep reinforcement learning. Tens of companies joined the European Digital Innovation Hubs with many universities designing AI-based tools for companies. This early work on neural architecture search drove a major program within EDA. Efforts are needed to continue collaborations at both levels (i.e., industry and research). For example, the EDA Action Plan will sponsor hackathons to encourage and fund AI/ML method development on open EDA data sets based on real-world problems posed by companies. The AI atop 2024 proposal seeks collaboration among 21 universities and over 20 industry participants to develop new AI/ML methods, benchmarks, and design challenges at multiple levels of semiconductor design for ongoing mentorship and usage at companies [2].

11.2. Knowledge Transfer Initiatives

Knowledge transfer is defined as the act or process of moving knowledge from one place, person or group to another. Transferred knowledge can be inherently understood and applied to the new context or may require a certain level of refinement to achieve a similar level of understanding and applicability in the new context [16]. It is a process which involves not only the initial transfer but also the refinement steps to complete the transfer process. Inside a large organization, it is common for research teams in different divisions and locations to focus on similar problems.

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With thorough analysis of both the old and new contexts, the data-driven research on the "old" context can be adapted to the "new" context. Researchers who are seeking or implementing knowledge transfer can benefit from the understanding of how data-driven knowledge can be transferred. If automated, this understanding can also be integrated into platforms to allow intelligent recommendation of transferability between existing works and new contexts.

The knowledge transferability analysis framework is proposed to analyze and implement the adaptation from one data-driven research work to another case with consideration of both the similarity and difference in the two contexts. The knowledge transferability analysis framework is proposed and applied to the case study of a general knowledge transfer analysis in Additive Manufacturing disciplines. A three-step target knowledge preparation process is proposed to transform inputs and models into a transferable format. The knowledge transferability test evaluates the adaptability of each component in a new context. The process of knowledge transformation and transferability testing is then automated into a pipeline. It has been applied to a case study in the AM field and successfully transferred a model to the process with successful adaptation of both the data and the model architecture at different levels. The pipeline completion suggests the importance of the proposed implementation and future prospects of similar studies.

XII. CONCLUSION

The integration of knowledge and machine learning into semiconductor research and manufacturing will be beneficial from a number of perspectives. There are plentiful considerations and challenges regarding the rapid advancement of the semiconductor industry, to the extent that semiconductor manufacturing is becoming a new science domain. The immense challenges arise from a missing understanding of new physical phenomena, device requirements, and process variations, and from the need to build new insights and theories for backend fabrication steps, to achieve smart and trustworthy chips, and to accelerate technology innovation.

The consistent and disciplined integration of AI/ML techniques into semiconductor research and manufacturing alongside computations, physics, algorithms, and heuristics can not only improve the traditional perspectives but also help accelerate learning and discoveries. The applications of knowledge and data-centric AI/ML methods to semiconductor processes, research, and industries may deepen the understanding and accuracy of the physics models. The unsupervised, supervised, and semi-supervised AI/ML methods may improve the yields and data-driven understanding of the semiconductor manufacturing processes and tools, help shorten the imaging time in the CT understanding, and accelerate new materials, devices and process development.

Additionally, there remain opportunities to develop more reliable AI/ML methods for real-life semiconductor research and manufacturing tasks. The uncertainty, nonlinearity, concurrentness, incompleteness and repeatability of the machine data and knowledge are believed to be common issues leading to wrong results and reliability concerns in the data-centric methods. Proper treatment of the modeling uncertainty, physics in the AI/ML, and novel computational architectures to accommodate machine knowledge and data in a concurrent and sequential way may be novel perspectives for further investigation.

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