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Analysis of Test Data and Test Data Volume by using EDT test compression for Multiple Configurations

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Abstract: As the Technology changes testing of a integrated circuits should be simpler, easier and faster to complete the process, according to the Design For Testability (DFT) process, testing of the integrated circuit becomes complex depending upon the number of flip flops present in the design. To make the testing simpler we are going to compression up to 20x and 25x depending upon the input configuration. It will be simple to find the input/output test channels for test coverage. In this paper we have defined to make test time and test data volume very simple and easier for multi users at different input. Scan insertion and compression can be done easily but EDT Compression is a tool used to make for multi configuration depending on the multi-input and multi output configurations. In this process of testing the integrated circuits and ATPG (Automatic Test Pattern Generation) setup can be done for the multi configuration. Experiments are done based on the multi-channel configuration for multi users at different compression Ratios, Serial and parallel Patterns can be generated according to configuration level

1. INTRODUCTION:

Design for Testability is a Techniques that reduce the difficulty of the test and cost associated with testing in an integrated circuit. This results in a decrease in the time spent on a tester, a decrease in cost associated with generating the test vectors or in the design iterations necessary to achieve acceptable test coverage or yield.

Design for Testability (DFT) is basically meant for providing a method for testing each and every node in the design for structural and other faults. Higher the number of nodes which can be tested through the targeted number of patterns, greater is the test coverage of the design. For this to be possible, every node in the design has to be controllable and observable. We can consider these as the two basic principles of DFT which are to be followed in order to have the maximum test coverage possible through minimum number of patterns.

A node can be made controllable by inserting control points. If the test coverage target is not getting met through target number of patterns, control points are inserted to increase the test coverage. A control point is an alternate path supplied to a node to let a particular value propagate to it and observability is the ability to measure the state of a logic signal. When we say that a node is observable, we mean that the value at the node can be shifted out through scan patterns and can be observed through scan out ports.

Scan chains are the elements in scan-based designs that are used to shift-in and shift-out test data. A scan chain is formed by a number of flops connected back-to-back in a chain with the output of one flop connected to another. The input of first flop is connected to the input pin of the chip (called scan-in) from where scan data is fed. The output of the last flop is connected to the output pin of the chip (called scan-out) which is used to take the shifted data out. The figure below shows a scan chain. Scan terminology, before we talk further, it will be useful to know some signals used in scan chains which are as follows:

- Scan-in: Input to the flop/scan-chain that is used to provide scan data into it
- Scan-out: Output from flop/scan-chain that provides the scanned data to the next flop/output
- Scan-enable: Input to the flop that controls whether scan in data or functional data will propagate to output

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The test data volume increases exponentially with increase in circuit size. For large circuits, the growing test data volume causes a significant increase in test cost because of much longer test time and elevated tester memory requirements to store the test data.
Embedded Deterministic Test (EDT) is One of the most common hardware test compression technique is EDT, is the tool that can generate the decompressor and compactor logic at the RTL level logic.
ATPG tool generates a pattern, it targets a group of faults as a result only a small number of scan flops need to take specific values. And it would use random values to fill up the unspecified scan flops that cannot improve targeted fault detection.

1. Literature survey:

In [1], they have presented a reconvergence-aware testability measure that is intended to improve the ATPG justification process and Experiment results show that it is very effective for circuits with deep logic structures. They have investigated the efficiency of the proposed testability measure when integrated with more advanced ATPG algorithms and they have tested with only few algorithms still work can be extended to many advanced algorithms.
In [2], the average pattern count reduction factors for LOS and LOC closely match. It can be conclusively said that LOC ATPG engine has matured enough to completely replace LOS scheme from all types of deigns and for all types of at-speed testing needs. However, the silver lining for LOS scheme is if used together with LOC scheme, for slower designs the best test coverage with least pattern count can be achieved without adding any test points.
In[3], In this paper, they studied an effective and practical transition and path delay testing methodologies. This paper also conveys the basic understanding of LOC, LOS and LOES transition delay testing techniques along with their comparison. The main goal of this paper is to give brief about benefits and difficulties, of these three methodologies, we need to consider during delay testing and automatic test pattern generation.
In [4], they propose a test pattern generation flow for stuck-at faults, static bridging faults, transition faults and transistor stuck-open faults. All of these faults are converted into constrained stuck-at faults in a proposed circuit model which supports test generation for DC faults and AC faults using either LOC or LOS test scheme and experimental results show that their method can achieve much less test application time with smaller test sets compared to conventional methods using either the LOC or LOS test scheme.
In [5], LFSR based BIST circuit showed poor performance and is only recommended for less number of input bits. We observed a high dynamic power consumption due to this factor and can be reduced by using other two ATPGs techniques. Though an area overhead was detected but is worth using these techniques for low power dissipation, lesser transition count, efficient fault coverage in reduced time samples. BS-CFSR based BIST decreased the transition count by 25% and architecture did not show any critical path violations. For CA based design, we achieved essential vector in shorter span of time which in turn in increased the fault coverage.
Future work includes implementing the same architecture for other more complicated benchmark circuits and analyse the results for the same. Another possible approach can be implementing these architectures on FPGAs and collect the results to analyse the actual hardware faults and compare them with the predictions made here. Hardware sensitized faults in the CUT will be deliberately achieved by programming the FPGAs likewise.
In [6], proposed two novel methods to generate and compress test patterns for probabilistic circuits. A novel ATPG maximizes the difference between EP of a fault-free circuit and EP of a faulty circuit so that the pattern repetitions can be reduced and in addition, for a given fault, they proposed to accumulate pattern contribution among different test patterns to further reduce the number of pattern repetitions.
In [7], a new method of transition fault testing, referred as enhanced launch-off-capture, has been proposed which provides better controllability than the conventional launch-off-capture method. LOC testing is known to provide fewer quality results, both in terms of pattern count and fault coverage, but design teams may not use launch-off-shift due to the challenge of routing the scan enable signal.
In [8], they characterized the behavior of RSFQ cells under process variations, and addressed its characteristics by developing a completely new ATPG paradigm for generating test patterns for DTV and path delay fault testing of RSFQ circuits.
In [9], they characterized the behavior of RSFQ cells under process variations. A completely new ATPG paradigm for generating test patterns for path delay fault testing of RSFQ circuits is presented. their approach can certify chips at considerably lower clock periods, and hence preserve the key performance advantage of RSFQ. It also enables high quality delay testing and timing verification without astronomical overheads of full-scan.
In [10], The proposed AE method significantly increases fault detection and improves the TC. The TC is very critical to enhancing the yield of the product and to reduce the DPM. The AE method combines the merits of scan compression and scan. Hence it improves the controllability and observability of the scan cells those need to be specified most of the times in scan load test patterns. The AE method increases TC when total care bits density of the scan cells excluded from the compression technique is in the range of 12% to 43%.
From this survey we found that still lot of work need to be carried concerned to the circuit design patterns, fault detection,

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power consumption, quality and delay test need to be improved.
In [11], in this methodology configured for single compression selection, although test compression techniques significantly reduce test costs, they also complicate the DFT planning by introducing more design parameters. In general, to implement an EDT architecture, one needs to determine the following three parameters: 1) how many scan chains are to be inserted into a design, 2) how many input channels to the EDT from the tester are to be used, and 3) how many EDT output channels, Test cost is determined by the required test time and storage for test data on the automatic test equipment. The work presented here can be applied to a single design core as well as to an SoC system. In a modern SoC system, hundreds or even more design cores equipped with respective EDT hardware are integrated.
In [12] according this author he use to take different inputs/outputs it is critical to understand the different the impact of using different numbers input/output test channels on test coverage, test channels on test coverage, test cycles and test data volume and in this paper there are two approaches to predict the test data volume and test pattern count are presented by using the compression tools we can achieve the scan channel patterns and without compatibility, configuration that results in the smallest and nearest data volume

2. Research Gap Identified:

As per the literature survey of the several authors were discussed only on the EDT compression architecture for single configuration but there is small gap for the multi configuration for EDT Compression,
Then we can able to find test time and test data volume for multi configuration, behavior of the Scan Chain and Length according that configuration

3. Objectives of the proposed work:

Effective EDT compression for multiple configurations for ATPG test Pattern Generation.
Analysis of Test data volume and Test Time for EDT compression each configuration with automatic test pattern generation.

4. Methodology to be followed:

Effective EDT compression for multiple configurations for ATPG test Pattern Generation.
- ✓ compression of the combinational or sequential logic circuits by using EDT architecture.
- ✓ setting of Multiple configurations depending upon the primary input provided.
- ✓ Pattern Generation for each of the configuration.
- ✓ Simulate the Test pattern generated.

2 Analysis of Test data volume and Test Time for EDT compression each configuration with automatic test pattern generation.
- ✓ Analyse the constraints of the EDT test compress of each configuration.
- ✓ Analyse the test data volume and test time for each configuration.
- ✓ Pattern generation and Simulation.

5. Expected outcome of the proposed study:

We use to get the multi configuration of the architecture for different input users.
Distribution Scan chains and Chain length for the different users.
ATPG (Automatic Test Pattern Generation) setup for multi configuration.
EDT architecture for Multi configuration level.
Modification for different input size of architectural flow
Simulation and Debug Level for Multi configuration

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