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Analysis, Design and implementation of Low Power and delay of 10T Full adder at Different technology

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Abstract: Power consumption has emerged as a primary design constraint for today VLSI integrated circuits (ICs). AS per reducing Technology, mostly Nanometre technology regime, leakage power has become a major component of total power. Full adder is the heart of any central processing unit that is a core component employed in all the processors. Full adder is the basic functional unit of an ALU. The power consumption of a processor is lowered by lowering the power consumption of an ALU. In this paper we introduced low power consume & Propagation Delay of one-bit full adders by using 10T. The analysis of the developed full adder design is done at room temperature CMOS 45nm,90nm and 180nm technologies using Cadence virtuoso tool. The result shows the comparison between different CMOS technologies in 45nm,90nm and180nm using Cadence virtuoso tool on the design in regards of power dissipation, propagation delay and power delay product. The simulation has been carried out on a Cadence environment virtuoso tool using a 45nm,90nm,180nm Technology.

Keywords: VLSI, CMOS, Full adder, Power, Delay, Transmission gate

I. INTRODUCTION

In VLSI such as video processing and microprocessors, digital signal processing, microprocessors, extensively use arithmetic operation. Addition, subtraction, multiplication, and accumulate are examples of the most commonly used operation. In this paper we present a novel 1-bit full-adder cell which offers faster operation and consumes less power than standard implementation of the full –adder cell. The one-bit full adder has a three-input two-output building block. The inputs are the two bits to be summed A and B and the carry bit Ci, which derives from the calculations of the last stages digit. The outputs are the result of the sum operation S and the resulting value of the carry bit Cout. More expressly the sum and carry output are given by

S = A⊕ B⊕ C in----------1
C out = AB + BC in + C in A--------2

From (2) it is evident that if A=B the carry output is equal to their value. If A≠ B we have C out = C in (the full adder is said to be in propagate mode), and hence, the full adder has to stay for the computation of C out.

II. POWER CONSUMPTION IN CMOS VLSI CIRCUITS

There are three main components of power consumption in digital CMOS VLSI circuits.
1) Switching power: consumed in charging and discharging of the circuit capacitances during transistor switching.
2) Short-circuit power: consumed due to short-circuit current flowing from power supply to ground during transistor switching
3) static power: consumed due to static and leakage currents flowing while the circuit in a stable state.
4) The power consumption for CMOS circuit is given by the following equations:

$$P_{AVG} = P_{DYNAMIC} + P_{LEAK} + P_{SHORT\text{-}CIRCUIT}$$
$$= CLV_{DD}V_{FCLK} + I_{LEAK}V_{DD} + I_{SC}V_{DD}$$

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III.IMPLEMENTATION OF FULL ADDER ON MOSFET AND CMOS

Full adder is a unit that adds two numbers and the carry and generates sum and carry. The full adder circuit adds three one-bit numbers (A, B, C in) and outputs two one-bit numbers (S, C out).
The logic circuit of full adder is shown in Fig 1. and the truth table is shown in Table 1.

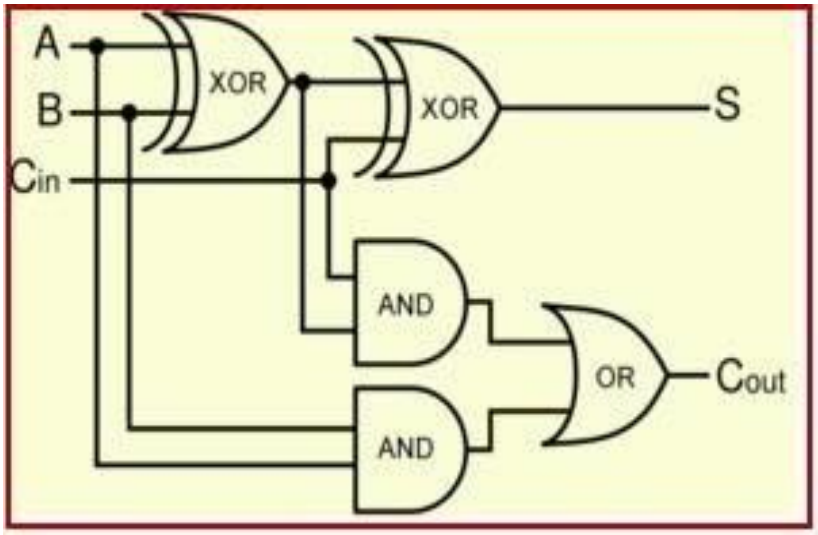

Fig 1: Logic Circuit of Full Adder

Input bit for number A	Input bit for number B	Carry bit input C_{IN}	Sum bit output S	Carry bit output C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth Table of Full Adder

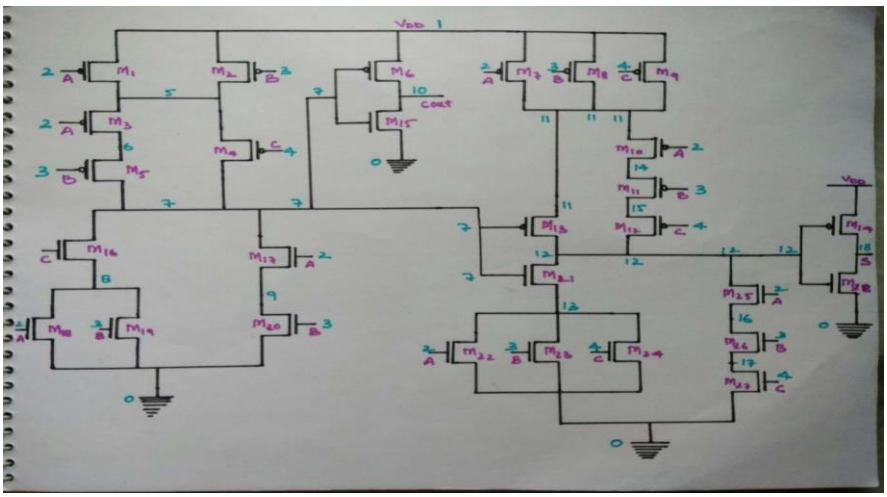

Fig 2: Realization of Full Adder using MOSFETs

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The simulated output of full adder is shown in Fig 2. In the Fig 3. given below, the first three waveforms represent two inputs and carry which is zero here. The fourth waveform gives the carry out and the fifth waveform is the sum obtained. The simulated output of the full adder satisfies the truth table given in Table 1.

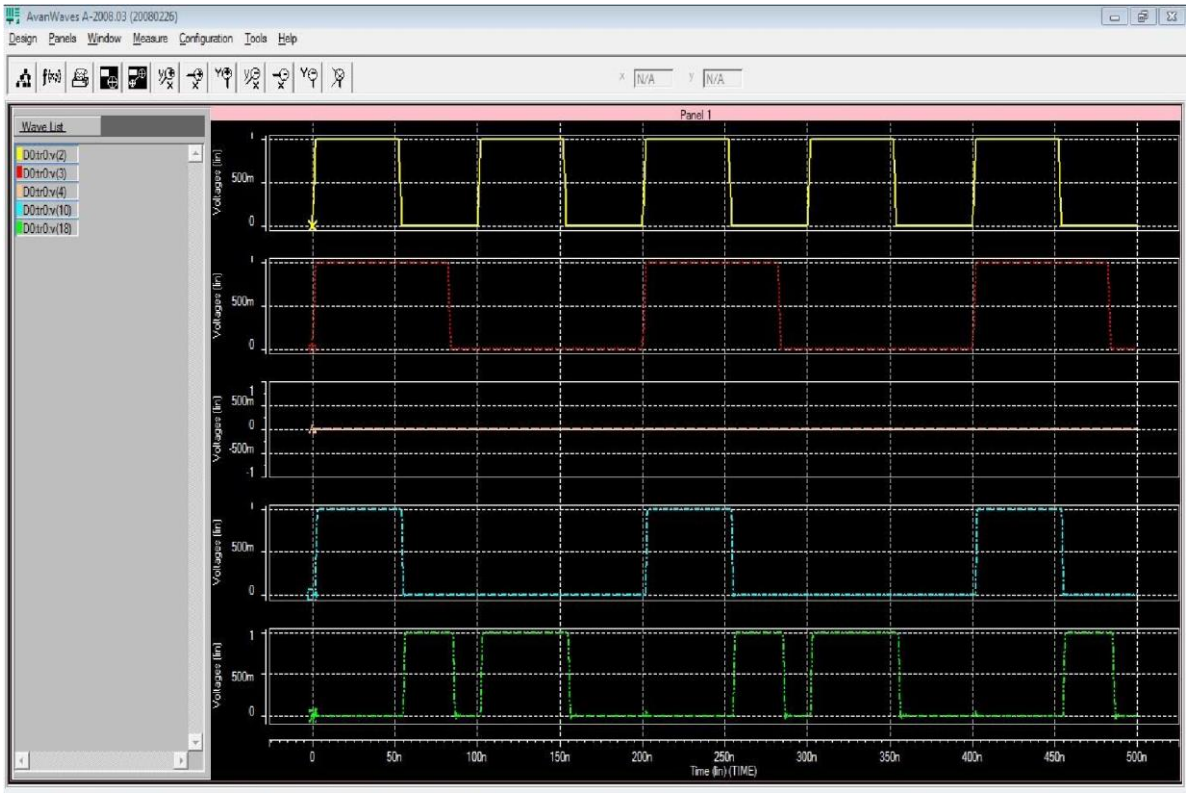

Fig 3: Simulated Output of Full Adder

10T 1- Bit Full Adder circuit

In this section one bit 10T smallest size lowest power consume Full Adder circuit is designed Fig 4. shows the10T full adder circuit. It is the essential element of full adder cell and it generates the basic addition operation of adder cell. Output waveform of 10T full adder is shown in Fig 5.

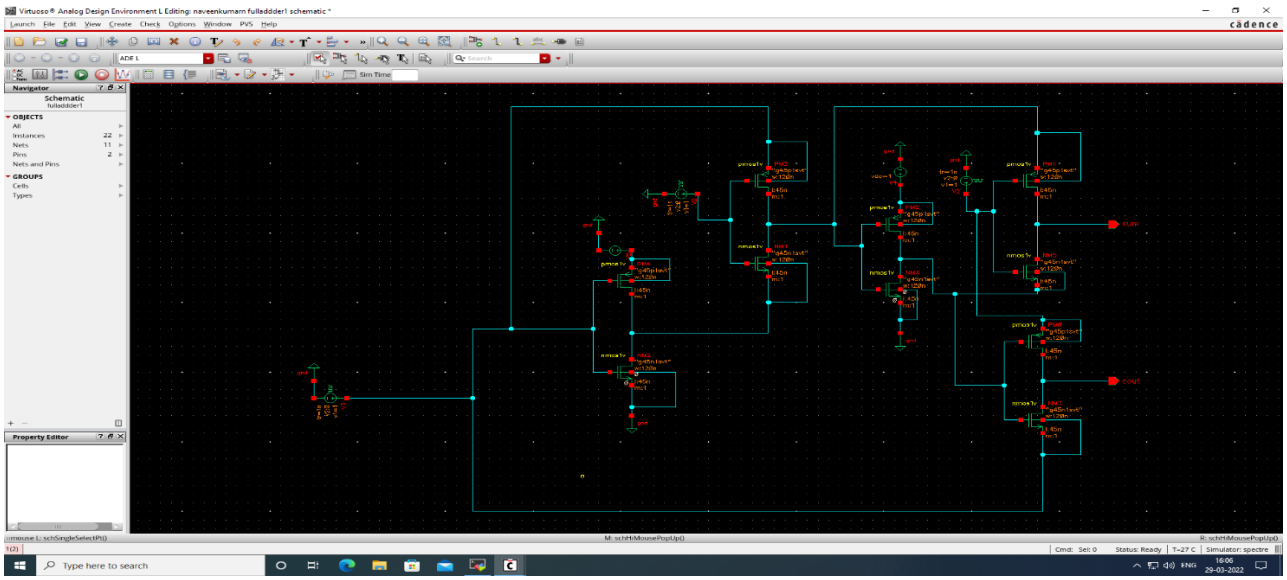

Fig 4: Full Adder using 10T transistor

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Fig 5: Simulated Output of 10T Full Adder

IV. The Proposed 10T Full Adder

The circuit of 10T Adder is a one-bit full adder cell made of five CMOS inverters that are connected as shown in Fig 6. Input A is directly connected to inverter first while input B is connected second and third inverter. Second inverter PMOS drain and third inverter NMOS drain are connected first inverter output while second inverter NMOS drain and third inverter drain are connected directly input A. Second inverter output is connected fourth inverter input and input Ci is given in inverter fifth. There is interesting, the power supply VDD connected first inverter only. All transistors have minimum length (LMIN =45nm according to used Technology), while their widths are typically proposing parameters.

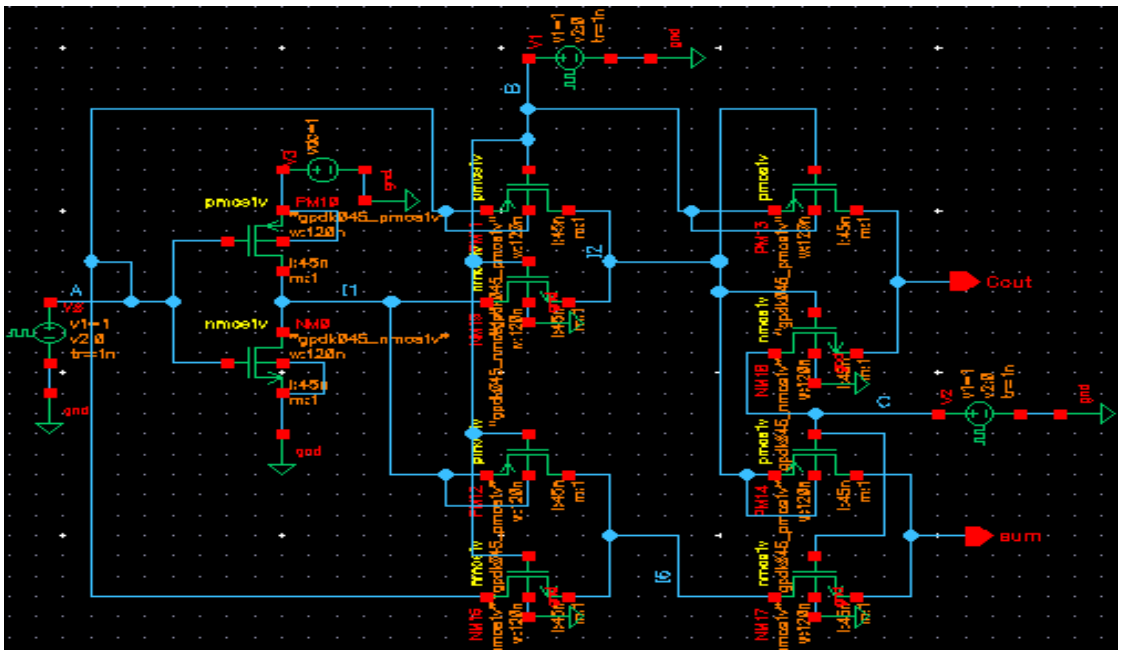

Fig 6: Proposed Ten Transistor Adder cell.

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Based on CMOS 45-nm process technology, the proposed full adder is proven to have the minimum power consumption and less power-delay product by Cadence simulation comparing with other prior literature. The characteristics of the novel hybrid full adder shows that the design has the best power-delay product for carry out signal. Output waveform with leakage current is shown in Fig 7.

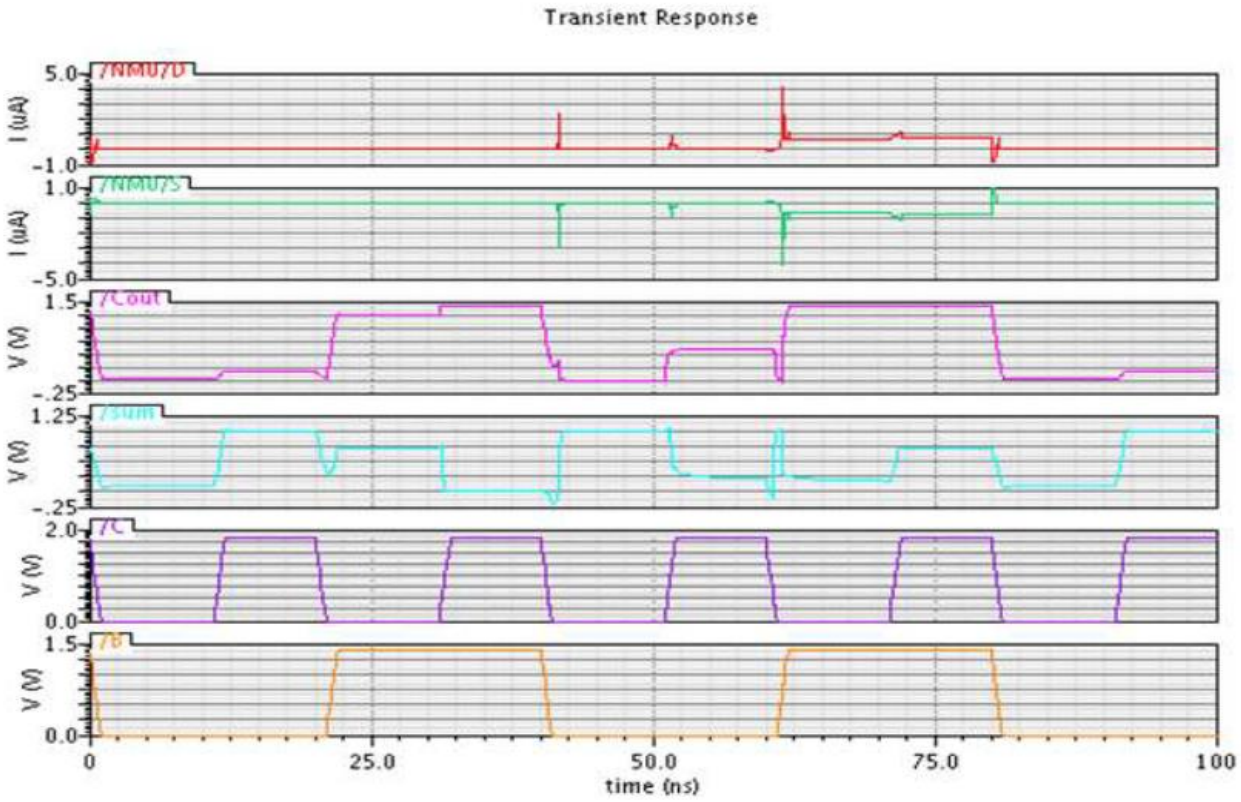

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Fig 7: Leakage current graph of proposed 10T Adder

Table 2: Comparison between base paper design and proposed design in terms of power consumption for various logic design (1-bit Full Adder)

LOGIC DESIGN	45nm(power watt in)	90nm(power in watt)	180nm(power in watt)
C-CMOS	1.10	4.609	13.45
Hybrid Logic[2]	0.65	1.114	5.641
Proposed design(10T)	0.011	0.037	0.342

In the table 2 and Fig 7. shows that the average power consumption for various design. In this table we discuss the various designs like C-MOS, Hybrid logic and proposed technique and concluded that the proposed design shows less power consumption as compare to base paper design.

Table 3: Comparison of power consumption and improvement as compare to base paper results in percentage.

Power Consumption Value and Improvement in Percentage			
Method	Hybrid Logic [2]	Proposed Design using 10T	Improvement in Percentage
Technology			

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45nm	0.65	0.011	98.99%
90nm	1.114	0.037	96.67%
180nm	5.641	0.342	93.93%

Summary of Results: In this paper proposed design consist of ten transistors and using combination of CMOS and transmission gate logic, from discussion or analysis of results concluded as following point.

➢ In the table I and figure VII shows that the average power consumption for various design. In this table we discuss the various designs like C-MOS, Hybrid logic and proposed technique and concluded that the proposed design shows 98.99%less power consumption in 45nm 96.66% less power consumption in 90 nm and 93.93% less power consumption in 180nm.as compare to base paper design.

V. CONCLUSION

In this paper proposed design consist of ten transistors and using combination of CMOS and transmission gate logic, from discussion or analysis of results concluded as following point. The average power consumption for various design compare to base paper design. We use cadence tool for simulation on in different technique and circuit parameter in 10T Adder cell and result that the 10T Adder is the most prominent low power consumption cell. The leakage power can be reduced by using various techniques. We have found that V_{TH} is the most appropriate parameter for leakage power current.

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