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Qualification of 22nm FinFET Via for 5G Technology

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Abstract: As the world is moving on the FinFET technology sizes is scaling down accordingly which will benefit the logic devices as the cost for the customers will be reduced and also the area required for placing it also reduces. FinFET technologies provides significant performance boosts for both logic as well as RF/mmWave over planar technologies. FinFET technology is used in 5G technologies where we need to consider the RF performance such as mobility improvement. The path of RF technology development is to concentrate on how to detach the manufacturing of RF devices from the scaling of logic devices with the least amount of negative influence on the coexistence of RF and logic devices. In order to get technology in right aspect, we need to develop runsets to check if layers are perfectly placed without any error before manufacturing it. DRC (Design Rule Check) is an important part for checking the BEOL (Backend-Of-The-Line) configuration. By maximising design productivity and acting as a doorway to the foundry where the integrated circuit (IC) will be manufactured, a well-made physical design kit (PDK) can help an integrated circuit (IC) designer achieve that goal.The main outcome of this work is to develop a runset which will provide an error free circuit design which will be beneficial for RF and the logic devices.

Keywords: DRC, Via, 5G Technology. FinFET.

I. INTRODUCTION

A process design kit (PDK) is a collection of files that the semiconductor industry uses to simulate the fabrication process for integrated circuit design tools. By specifying a specific technology variation for their processes, the foundry creates the PDK. After that, it is given to their clients for use in the design process. Customers can modify the process design kit to suit their unique design tastes and target markets.

Before returning the design to the foundry to make chips, the designers utilise the PDK to design, analyze, sketch, and validate the design. The data in the PDK is chosen early in the design phase, determined by the market demands for the chip, and is unique to the foundry's process variation. The likelihood of a successful first-pass silicon will rise with an accurate PDK.

Design Rule Checking (DRC) is a technique that determines whether a particular design complies with the limitations given by the process technology that will be utilised to manufacture it. DRC checking, a crucial component of the physical design flow, guarantees that the design complies with manufacturing specifications and won't cause a chip failure. Process technology guidelines are provided by process engineers and/or fabrication facilities. For each process technology, detailed instructions will be provided. Advanced nodes' manufacturing technology advances, increasing the amount of DRC rules and their complexity. Here are several fundamental and typical DRC rule kinds.

The 22FFL process is constantly developing into a complete set of technological capabilities that enable several new applications, including high-speed and low-power communication. Technology features include hybrid RF power FinFET transistors for high signal RF circuit design and RF FinFET transistors for small signal RF circuit design. The first family of RF transistors consists of Low-leakage (LL-RF) and High-density (HD-RF), whose layouts are interchangeable.

Taps are positioned close to the active device to lessen noise coupling and have a reduced overall footprint. For situations where a high transistor density is desired, HD/LL-RF transistors offer good performance on a small layout. High-performance (HP-RF) is defined to target for the best RF performance achievable, whereas the primary enhancement for HD/LL-RF transistor was performed to balance the performance of the device and the fixed footprint.

The self-resonance frequency(SRF) of the passive components becomes increasingly important to take into account in BEOL (Backend-Of-The-Line) arrangement as the operating frequency moves into the sub THz range.

II. LITERATURE SURVEY

The paper [1] talks about the problem such as overshoot, reflection, crosstalk etc. when making a printed circuit board which is having high frequency and are used in high speed projects. This can lead to project failure due to the transformations in electrical signal geometry. All these issues can be solved id the right rules are set in the DRC code and

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validating the design before manufacturing. The author talks about how HyperLynx DRC which is from Mentor Graphics can catch all the design issues in a virtual printed circuit board. HyperLynx DRC is considered to be far better than normal DRC when it comes to validating PCB.

In day-to-day world constant development in the field of Integrated circuits(IC) advanced technologies, physical verification is becoming more important and much more complex in the semiconductor industry. The design rules checking (DRC) verification adopts varies regression patterns-based techniques. The paper [2] talks about a new procedure of verifying the DRC, complementing the standard Regression technique, the regression layout patterns is compared with the DRC check on a line by line basis . By using this technique, we can get all possible defects in the QA stage and also an quantitative analysis for all DRC component. Also the time consumed will be reduced compared to previous methods.

This author of [3] talks about various testing challenges faced in Intel's high-performance IA Cores and also the novel Automatic test pattern generation(ATPG) solutions developed to get the best. Intel's IA Cores performs a design structure which has a unique testing task for the industry standard design for testing(DFT) tools. Firstly, the recurring use of both flip-flops and latches while employing a two-phase clocking scheme. Secondly, the structural based patterns that uses the functional clock network, keeping the power profile as well as performance which is similar to the functional test. The paper discusses on the development to handle certain unique designs and innovative methods to enhance the Design Rule Checks (DRCs).

The paper [4] talks about different approaches for stacking in a multi-layer form, including die to die (D2D) and wafer to wafer (W2W) stacking. The impact on the system yield stack and the productivity cost can be determined by the complexity of the approach taken. It has also been presented that component yield loss is noticed in W2W stacking approaches. To overcome the issue, die to wafer stacking approaches, where pretested KGD's are stacked, have also been considered. When compared to Sequential TCB stacking Die placing with collective TCB can be cost effective for high stacking yield values.

Intel has a unique technology which is the 22nm FinFET technology called as 22 FFL which offers high performance RF transistors achieving fmax and ft above 450 GHz and 300 GHz, respectively. This technology is mainly used in 5G technology which also provides enhanced mmWave back end of line and high performance RF device, with all this features the design will be able to have a great coexistence between logic and RF technologies. [5] shows how these features demonstrate how Intel continues innovating in order to deliver advanced solutions for RF application.

Intel 22 FFL is a popular FinFET technology process which mainly are for optimization of mmWave and RF applications providing greater RF performance to planar technologies. This technology has an improved flicker of noise in planar technologies and provides an really good power gain efficiency enabling wireless applications with low power. FinFET technologies provides excellent performance for both logic as well as RF/mmWave over planar technologies. [6] shows that the 3D fabrication technologies allow keeping Moore's law alive beyond the physical limit of the 2D device fabrication.

In the [7] paper a state of art 12nm FinFET technology which has Performance, Power, and Area improvement compared to 14nm technogy. 30% leakage reduction are seen in SRAM at the same Iread. This technology also shows compelling performance and area scaling. The author talks about how 12nm FinFET technology is highly manufacturable and reliable, as 15% of AC performance improvement and 30% SRAM leakage improvement are been notices when compared to 14nm where the optimization of device architecture took place in junction, fin and contact modules. The 7.5T library which is having aggressive rules and special construct rules which enables 12% scaling of logic area and 16% total power reduction when compared to 14nm.

The [8] paper talks about the analog design flow and the steps involved, using an electronic design automation [EDA] tools and proposes a design methodology.The DRC, LVS, op-amp and generating parasitic extracted SPICE net list are used by EDA tool called as Electric-VLSI. The Ngspice provides electric and electronic circuit simulator for the simulation of SPICE net list. The Ngspice has it's own scripting language which will be used to perform Monte Carlo simulations and corner analysis. The desired results are seen from the simulation results for the designed operational amplifier.

Superconductor IC design tools have advanced thanks to the IARPA SuperTools initiative. Traditional semiconductor layout-versus-schematic verification (LVS) technologies are insufficient for superconductor integrated circuits because they feature Josephson junctions and significantly rely on coupled inductors and inductive interconnects. The development, modification, and parametric verification of superconductor and quantum circuit architectures are made possible under SuperTools, an open-source LVS framework. A Python-based framework called SPiRA was created to make it easier to create parameterized layouts while also accounting for magnetic rule checking and design rule (DRC). Through a rule deck database (RDD) and Python-based PDK schema from which cells are produced as objects with intrinsic properties, SPiRA is made to accept any process. With the capacity to extract an electrical netlist that can be simulated and parameter extraction conducted upon, this approach enables the quick implementation of changes to layouts. GDSII layouts are created via SPiRA, and the Gdspy library enables fast visualisation of the layout. In order to assess SPiRA's capabilities, the extraction results from [9] built parametrically using SPiRA are compared to those for

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layouts created manually. With the aid of the inductance extraction tool InductEx, SPiRA enhances designs for inductance and compact design extraction.

The [10] paper talks about how FinFET along with overactive gate (COAG) is used on 12nm node process technology which will optimize the Maximum Oscillation Frequency (Fmax) and the Minimum Noise Figure (NFMIN) for technologies with larger number of fin. The proposed COAG design shows the reduction of gate resistance of the 40-fin device by ~10-fold, and also improving the Fmax by ~180% when compared to the traditional FinFET's.

In the [11] study, an unique back-end-of-line (BEOL) in Intel's 22nm FinFET (22FFL) technology is used to create a mmWave switch. ExpressVia, which enables direct transistor contact to thick metal layer, is included in the recently developed mmWave BEOL. Design adaptability is also made possible by continuous via and 3+1 thick metal layers. An ultra-wideband (DC-60GHz) series SPST switch is built in this technology, takes use of the additional features, and achieves 1.9dB insertion loss, 21.0dB isolation, 17.3dB return loss, 24.1dBm IP1dB, and 35.9dBm IIP3 at 28GHz within an active area of 0.00176mm. The switch can withstand up to 24.9dBm of output at 28GHz, according to reliability measurements. A good fit for 5G application is the estimated RonCoff at upper metal, which would be 107fs.

The power and delay are one amongst the factors within the design of IC's. Cutting down of transistor's can reduce size of IC, and might sometimes due to scaling the short channel effects is caused when finished beyond nanometre and this causes leakage in power. In order to reduce the short channel effects and to reduce power dissipation, FinFETs are being used. From the [12] paper, it is observed that there is reduction in the power dissipation to a larger extent in 22nm FinFET technology in comparison to 45nm CMOS technology.

The 22FFL is a 22 nm FinFET technology that provides high performance, single-pattern backend flow, and ultra-low power logic transistors. According to the author of [13], high performance transistors exhibit larger NMOS/PMOS driving current when compared to 22nm technology. When compared to SRAM cells, the bit cell leakage can be lowered by 28x when using ultra-low power logic circuits, enabling a novel 6T low-leakage SRAM with bit cell leakage of less than 1pA/cell.

A HyPowerFF, often referred to as a High-Power FinFET, is a device with multiple workfunction materials and oxide thicknesses contained within a single gate. The suggested devices in [14] provide 290 GHz of maximum f and are as dependable as high-voltage IO devices with up to 7.1V of breakdown voltage, making them ideal for designing power-efficient RF power amplifiers (PA). In FinFET and HyPowerFF devices, RF performance and good durability may coexist. The majority of the voltage swing limitation for mmWave PA and RF applications is eliminated by the improved in dependability of large-signal RF performance at no additional expense to the 22 FFL.

III. THEORY AND CONCEPT

A. Challenges for RF technology

When it comes to CMOS technology for both bulk and planar there is a scaling limitation at approx 30 nm process node which is caused due to Drain Induced Barrier Lowering(DIBL), and so the FinFET was introduced for scaling operation in order to mitigate the degradation of DIBL. Due to increase in parasitics and velocity saturation the RF performance aggravates the pitch due to scaling operation as shown in Figure 3.3. It is important to check the RF performance when it reaches the peak at around 20 ~ 25 nm node, which suggests that the transconductance (gm) improvement by the channel length scale saturates, and due to the increasing parasitics the RF performance is impacted negatively.

B. Via

To connect between different metal layer, we require poly layer together with ethe metal layer that we are going to connect. Via minimization is an important factor when it comes to the routing phase in a particular design process of VLSI circuits and systems. The important factor of via is providing electrical connectivity between two layers. The points as shown in figure 3.5 where a net changes layer is where vias are formed. Sometimes due to increase in number of vias, the product reliability is reduced, which can also affect the circuit performance and can cause delay. Therefore, via minimization plays an important factor in vital role within the efficient yield of the circuit.

C. FinFET (Fin field-effect transistor)

Moore's law observes that in two years the amount of transistors on a given area of silicon will be doubled. By increasing computational density, we can achieve higher computational power by increasing the number of transistors. This method of increasing computational power can we achieved by reducing the size of the transistor without affecting the area. As the transistor size is reduced, the distance between the source and the drain also reduced, where the electrode passes in order to generate current, due to this the planar MOSFETs suffer short-channel effects (SCEs). This is the reason why the semiconductor industry has developed FinFET technology To overcome all this issue.

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A fin field-effect transistor (FinFET) is known to be a multigate device, a metal-oxide-semiconductor field-effect transistor (MOSFET) built on a substrate where the gate is positioned on two, three, or four sides of the channel or wrapped around the channel, forming a double or possibly multi gate structure.

IV. METHODOLOGY

A. Objective

- To understand the concept of DRC, runset, testcases and tools used.
- Development of script of the mock runset in Caliber, ICV and Pegasus tool.
- Creating the testcases for that runsets developed.
- Running the testcases and validating the runset for the result.

B. Methodology

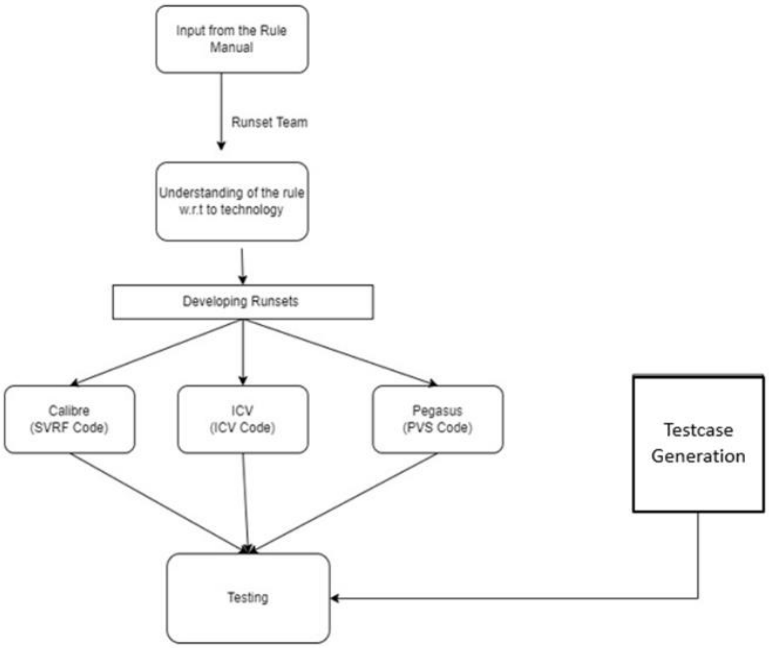

Fig. 1 Flowchart of the work

- The input is taken from the rule manual which is provided by the foundry.
- The inputs are analyzed by understanding the concept of the technology and the components used in it.
- The DRC code is developed in three different EDA tools which are Calibre, ICV and Pegasus, and each of this tool uses different scripting language which is SVRF, ICV and PVS respectively.
- After the completion of the DRC codes, the testcases will be generated which will be used to test all the DRC code code of all three EDA tools.
- After the successful testing of the DRC code, this will be implemented in the 22nm Finfet technology.

C. Design rule

TABLE I Rules for development

Sl.No	Rules
1	via outside lower_metal
2	via outside upper_metal
3	via size/shape is incorrect
4	Via not interacting metal
5	Width via, fixed value

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Sl.No	Rules
6	Via length, fixed value
7	Via_big length, fixed value
8	lower_metal side enclosure of via
9	lower_metal line-end enclosure of via
10	via center to center space
11	via -to- via spacing (edges), minimum, all-directional check
12	via edge to upper_metal corner
13	via may not overlap a corner of upper_metal

V. EXPERIMENTAL RESULTS

In the chapter we will discuss on the results achieved through the proposed methodology. It discusses about the testcases generated and the output from each EDA tool.

A. Work done & Results

Developed the DRC code for ICV tool and created the testcases for the particular via rule. The testcase has been created in the ICV tool which will be used to test the DRC code developed. In this testcase the right-side part are the pass testcases and the left-side path is the fail testcases, which means the DRC code developed should flag the pass in the right side testcases and the fail in the left side testcases. Once the result shows zero missing and zero false, we can say that our DRC code is validated.

Once the testcases is perfectly generated, the validation process will begin by running the code on the testcases and check if the code is coming without any error. The error can be showed by the number of Missing or False counts. So we need to make sure the missing and false counts must be zero by debugging the code till we achieve the perfect code.

TABLE II Results count for all EDA tool

TOOL	Missing	False	OK flag	Not OK flag
Caliber	0	0	332	178
ICV	0	0	794	528
Pegasus	0	0	1266	1204

Ok noflag:- Pass cases where code is checking it as right one
Ok flag:- Fail cases where code is checking it as wrong one
Missing :- Fail cases where code is checking it as right one
False :- Pass cases where code is checking it as wrong one

VI. CONCLUSION AND FUTURE SCOPE

The code validation is carried out in all the three EDA tool which is Calibre, ICV and Pegasus, where the required testcases has been created for the EDA tools and the validation is done on the testcases.

A. Conclusion

The semiconductor is one of the most booming industries where it is growing day by day and the chips are used in every modern device. When it comes to 5G technology we need to make sure that the RF as well as logical performance must be aligned to get desired output. In order to get technology in right aspect it is required to develop DRC codes to check if layers are perfectly placed without any error before manufacturing it. DRC (Design Rule Check) is an important part for checking the BEOL (Backend-Of-The-Line) configuration. The BEOL configuration is a method to make sure the RF and logical performance is aligned. So, we focused on making Via connectivity in an design in the right aspect by developing DRC code.

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The Proposed methodology consist of developing DRC code for all the three EDA tools which are Calibre, ICV, Pegasus and then creating testcases. The DRC code was validated with the testcases and numerous debugging and validation, the DRC code came out to be clean, which can conclude by telling us that the Via in the design chip is perfectly placed and can achieve

B. Future Scope

- The future enhancement of this project can include all the layer which is in a design chip in the DRC code and validating it.
- Doing the same methodology by using Convolution neural network, where this can be done in an automated way.

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