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APB PROTOCOL COVERAGE-BASED VERIFICATION USING UVM

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Abstract: As a part of VLSI technology, millions of transistors is integrated into a single chip called a system on chip (soc). AMBA protocol is much popular protocol for communication of soc component. AMBA was introduced by ARM for on chip communication. AMBA protocol has sub members like AHB, APB, and AXI etc. The APB is used for low bandwidth applications like timer, SRAM, UART etc. Hear in this project, mainly focus on design and verification of APB protocol using UVM, a standard verification methodology nowadays. Also this project involves in creation of coverage report for functionality check of the test bench environment, and also taking coverage report and analysing the design is covered 100% wrt test bench.

Keywords: AMBA, AHB, APB, UVM

INTRODUCTION

IC's are created by combining millions of transistor into single chip using Very Large Scale Integration. When microchips became widely used in 1970, VLSI technology emerged, allowing for the rapid advancement of both semiconductor and telecommunications technologies. Most integrated circuits (ICs) had a restricted functionality prior to VLSI technology. The electrical circuit is made up of logic circuits, RAM, and ROM. These are all combined into a single chip using VLSI technology. An SOC, or single-chip integrated circuit, incorporates the complete component.

The Advanced High-Performance Bus, Advanced System Bus, and Advanced Peripheral Bus are the three main parts of the AMBA bus design. A high performance bus with a larger bandwidth is AMBA AHB or ASB. These components that need more bandwidth, such as high-bandwidth on-chip RAM, high-performance ARM processors, and high-bandwidth external memory, connect to AHB or ASB. AMBA Components including UART, SRAM, DPRAM, keypad, and timer are connected to APB, which has a reduced bandwidth and performance level. The bridge serves as a conduit between AHB or ASB and APB. Therefore, every device linked to APB acts as a slave, and the ProtocolBridge for APB acts as a master. Figure 1.1 below shows the AMBA architectureview.

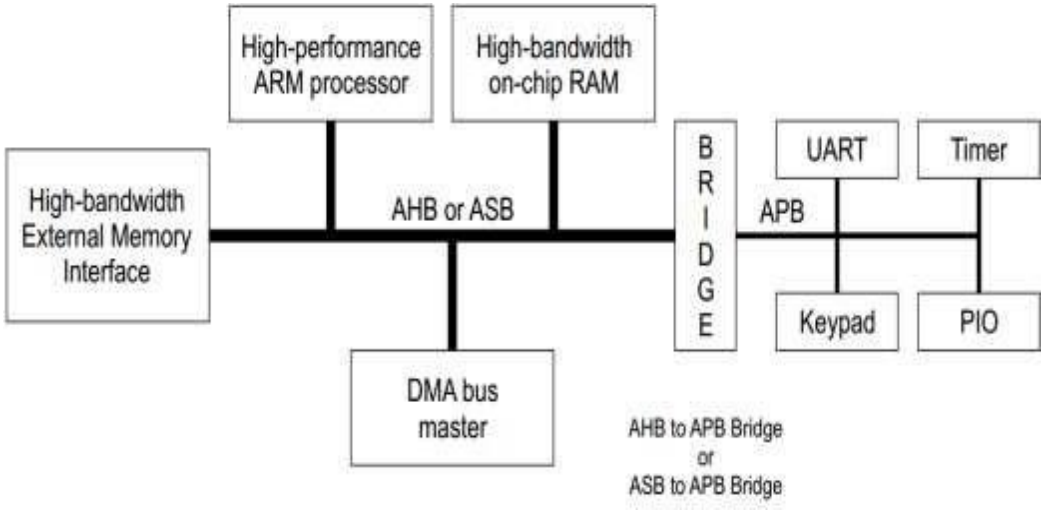

Figure 1.1 AMBA Bus Architecture

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APB Block Diagram

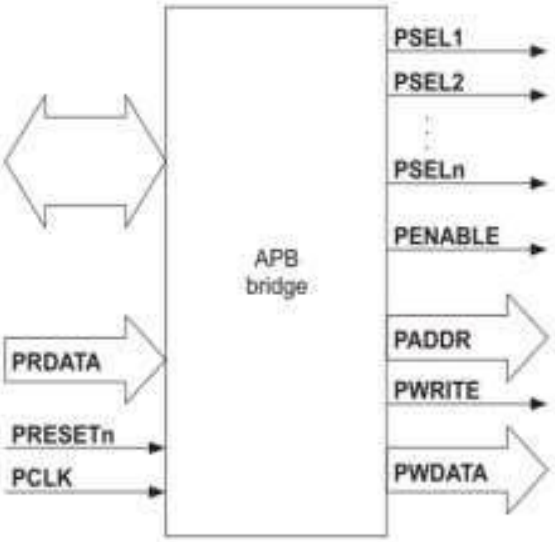

Figure 1.2 Block Diagram of APB Master

APB belongs to AMBA family for low frequency application. APB consists of APBbridge/master and APB slave. Figure 1.2 represents the block diagram of APB master.

APB slave

Figure 1.3 shows Block Diagram of APB slave. APB is simple interface, less complex, low bandwidth non pipelined on chip communication protocol.

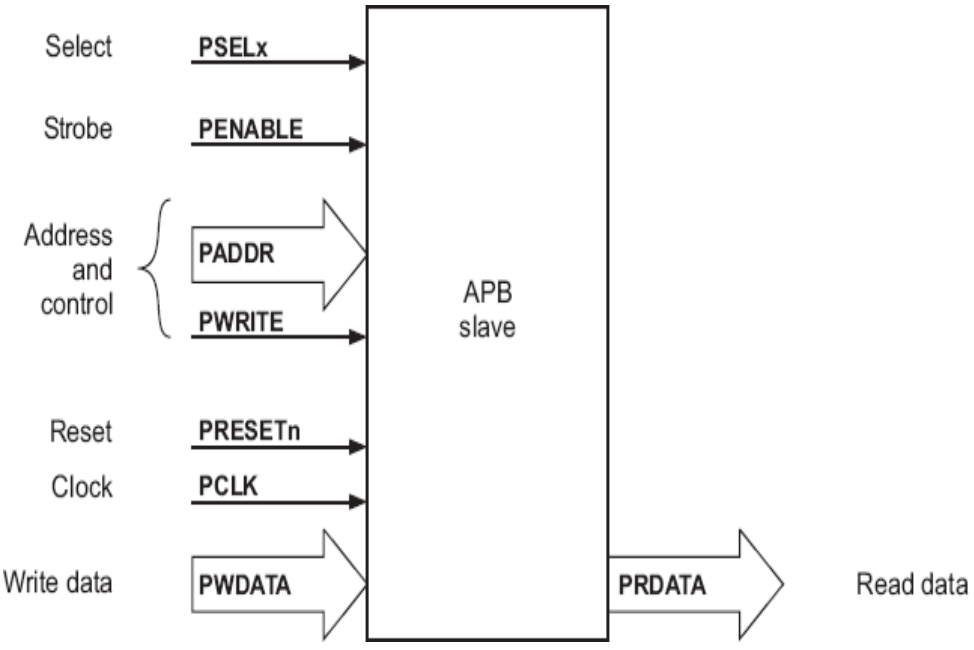

Figure 1.3 Block Diagram of APB Slave

Verification Methedology

Verification has most vital role in VLSI. The goal is to create bug free RTL Design, it seeks for bugs in design in early stage. Around 70% of time is consumed for verification in RTL process. Due to rise in number of transistor with in the chip, the design complexity has increased. This increases the probability of occurrence of error within the design.

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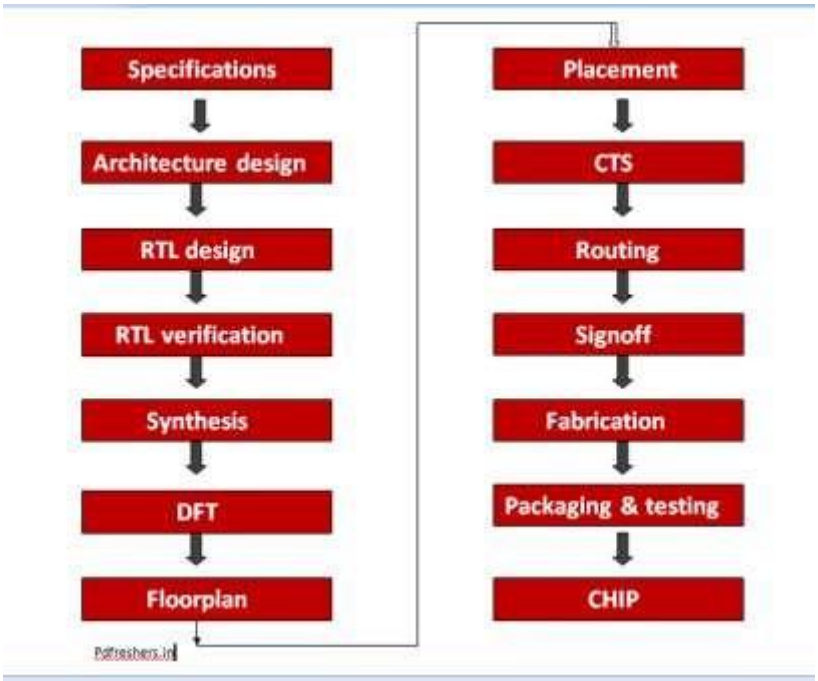

Figure 1.4 RTL Design Flow

Universal Verification Methedology

UVM is most commonly used verification methodology for RTL (register transfer level) design. UVM is an extended methodology from System Verilog. It consists of base class libraries. The verification engineer can create different test scenarios by extending these library classes. UVM also provides many other verification features such as factory for object creation, using macros for complex function, reporting mechanism, phasing, configuration etc.

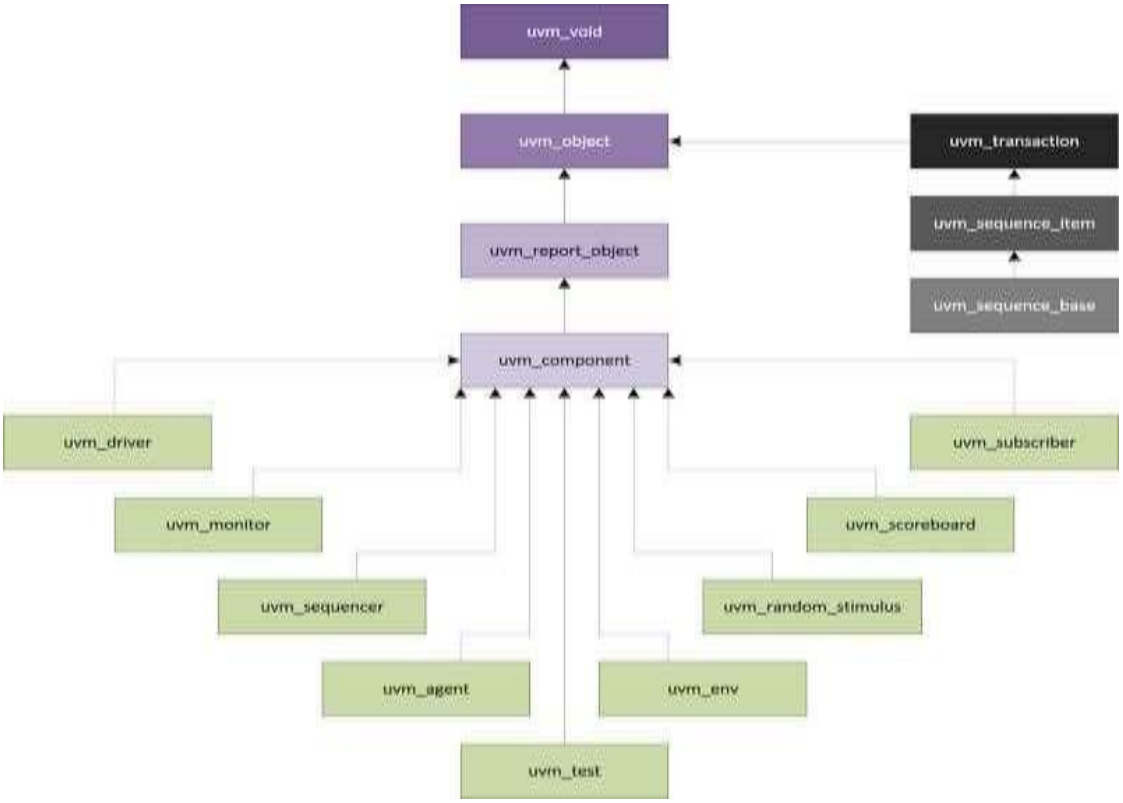

Figure 1.4 UVM class Hierarchy

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UVM Architecture

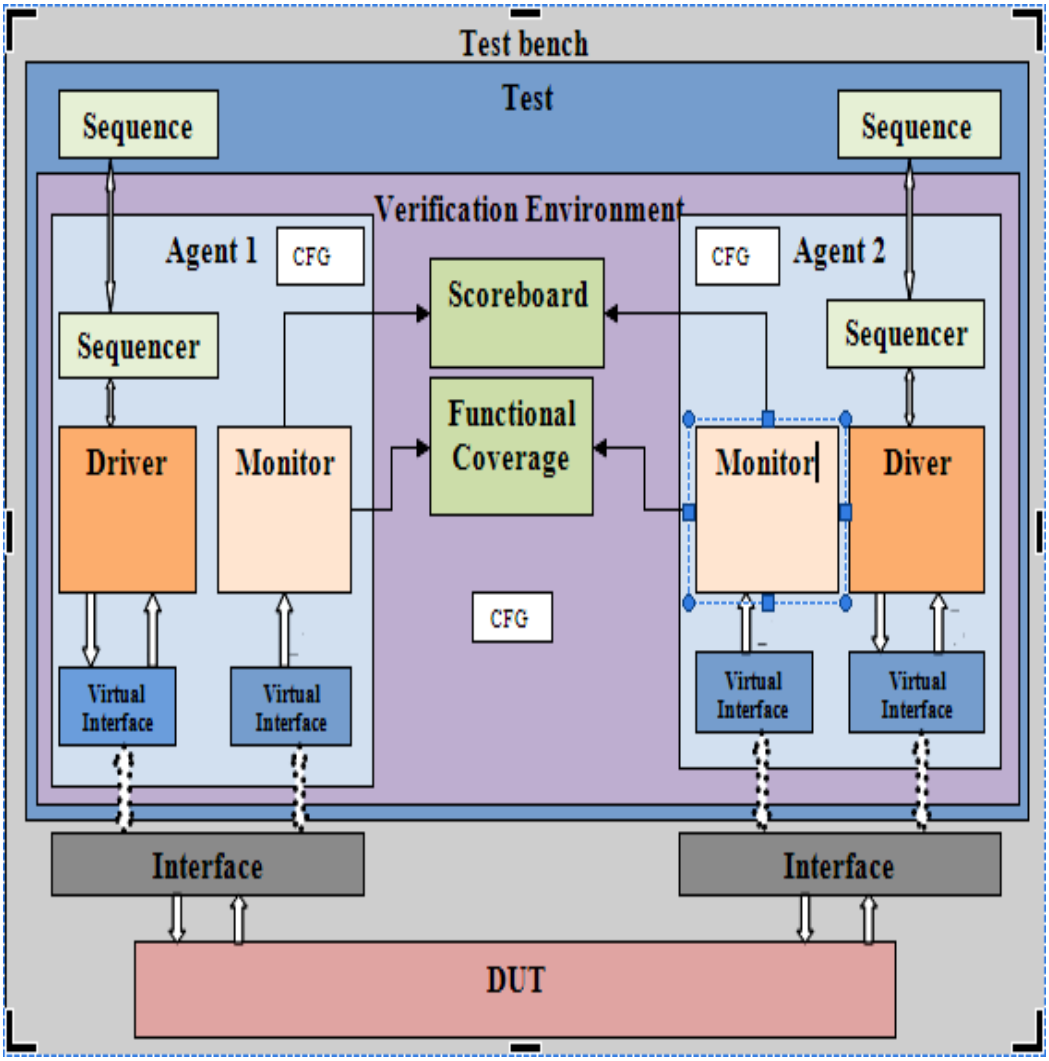

Figure 1.6 UVM Architecture

Sequence item: sequence item is extended from uvm_sequence_item.
Sequence: A sequence is created by extending the uvm_sequence. It is generates a series ofsequence item and sends them to driver via sequencer.
Sequencer: sequencer regulates the flow between sequence and driver. The user uses TLM port toconnect between driver and sequencer.
Driver: driver is extended from uvm_driver, which has get next item and item done. It drives theDUT.
Input Monitor: it acts as a reference module. Verification engineer write reference logic. Input'swhich simulate the DUT are sent from driver to reference module using TLM port.
Output Monitor: output monitor capture the outputs of DUT via virtual interface and send to score board for comparison.
Agent: agent is extended from uvm_agent. An agent contains driver, sequence and monitor.
Scoreboard: scoreboard is extended from uvm_scoreboard. It compares expected value and actualvalue.
Environment: environment is extended from uvm_env. Environment is a container for active and passive agent, scoreboard etc.
Testbench: uvm test bench is called by run test () method.DUT: design under test which is an actual design.
Interface: interface is a communication block between DUT and test bench. It consists of input andoutput signals
Top: top module contains test, interface and DUT.

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RESULT AND DISCUSSION

Output Waveform of APB protocol:

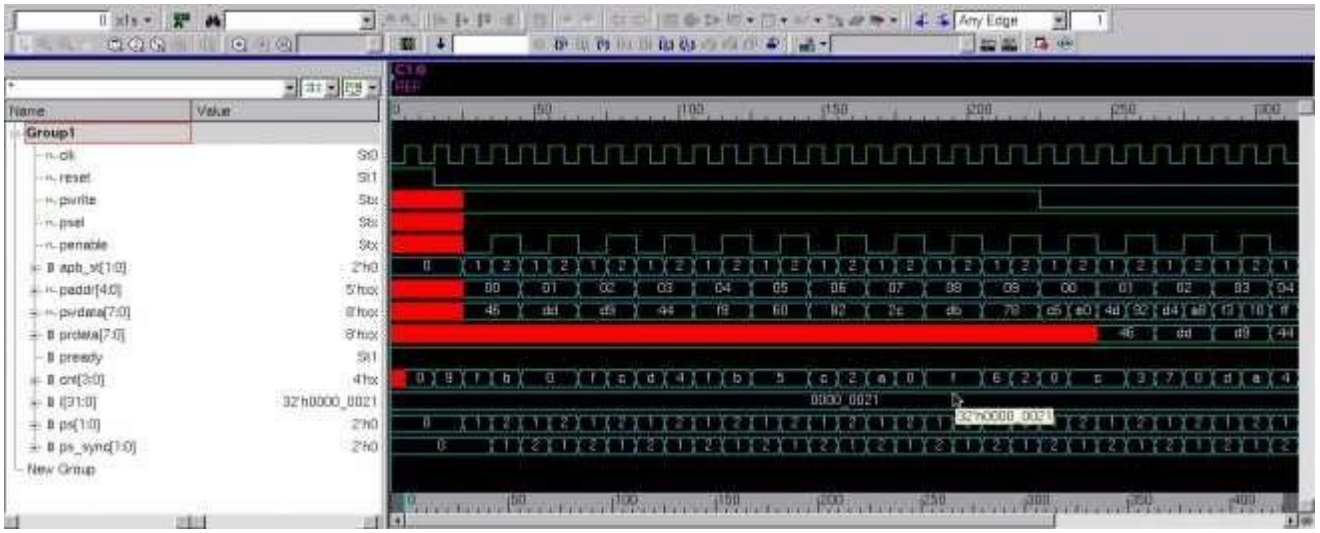

Figure 1.7 Waveform of APB Protocol

Figure 1.7 shows the waveform of APB Protocol.Here based on psel and penable the write and read transaction are performed, we are generating ten address(00,01,.....09) and we perform write operation for all these ten address, then we perform read operation from all these address. pwrite set the read or write operation. If the write and read data matches APB is functionally verified.

Coverage Output

Figure 1.8 shows the coverage of APB, report shows how much percentage of design and top module is covered. The design covers 91.47% of the total code.

Figure 1.8 Functional Coverage of APB

Code Coverage report

This below figure 1.9 shows code coverage report of APB. It is a report for interface, DUT, and testbench coverage

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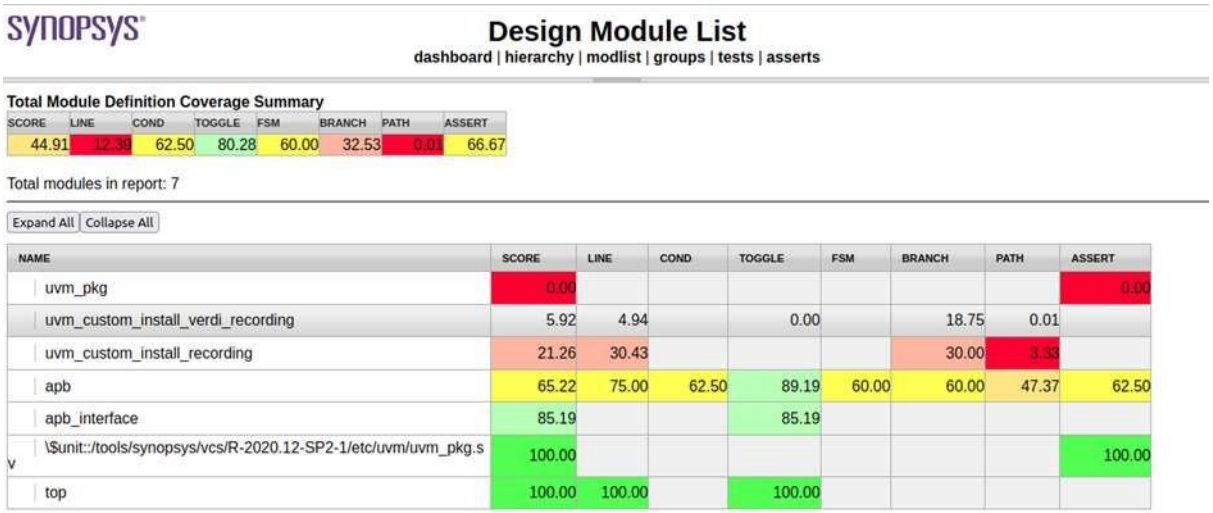

SYNOPSYS

Design Module List

dashboard | hierarchy | modlist | groups | tests | asserts

Total Module Definition Coverage Summary

SCORE	LINE	COND	TOGGLE	FSM	BRANCH	PATH	ASSERT
44.91	12.39	62.50	80.28	60.00	32.53	0.01	66.67

Total modules in report: 7

Expand All | Collapse All

NAME	SCORE	LINE	COND	TOGGLE	FSM	BRANCH	PATH	ASSERT
uvm_pkg	0.00							0.00
uvm_custom_install_verdi_recording	5.92	4.94		0.00		18.75	0.01	
uvm_custom_install_recording	21.26	30.43				30.00	3.33	
apb	65.22	75.00	62.50	89.19	60.00	60.00	47.37	62.50
apb_interface	85.19			85.19				
\$unit::/tools/synopsys/vcs/R-2020.12-SP2-1/etc/uvm/uvm_pkg.sv	100.00							100.00
top	100.00	100.00		100.00				

Figure 1.9 Code Coverage report of APB

CONCLUSION:

The APB has designed and verified using UVM. The waveform result from synopsis conclude the functionality of APB, the coverage report are taken to check design to the test bench of APB. Thus, APB design and verification is successfully.

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