IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

A Comparative Performance Analysis of 6T, 7T and 8T SRAM Ce

Sujata

Guest Faculaty, ECE Department, University Visvesvaraya College of Engineering, Bangalore, Karnataka, India

Abstract: In present work, a comparative analysis of conventional 6T, 7T and 8T SRAM cells has been performed using 180nm process design kit using Cadence Virtuoso. As the CMOS technology getting shifted in nanometer regime it faces a lot of challenges such as short channel effect and process variations. The SRAM parameters such as stability, power dissipation and delay of these considered cells have been investigated. It has been observed that write delay in 6T cell is improved by 2× and 0.14× as compared to 7T and 8T SRAM cells respectively. Furthermore, average read and writes power consumption of 7T SRAM cell found to be 1.2× and 0.98× less as compared to 6T and 8T SRAM cells respectively. Additionally, the 8T cell is having moderate write SNM i. e 32% more than 6T cell but 9% less than 7T cell.

Keywords: SRAM, delay, power dissipation, static noise margin, T (transistor).

I. INTRODUCTION

Now a day's SRAMs become the integral part of the system-on-chips (SoC). Process technology scaling has contributed remarkably in improving the area density and performance of SoC devices . However, future bulk- CMOS scaling faces a lot of challenges because of various limits in material and process technology. In order to overcome these problems, the structures for next-generation technology have been proposed such as low-temperature CMOS, silicon-on-insulator (SOI) MOSFET, SiGe MOSFET, double gate (DG) MOSFET, carbon nanotube FET, and FinFETs.

Today, systems on Chip are always a fast growing market. They have embedded more and more complex functions that require an increasing memory capacity. The Static Random Access Memory SRAM is the mostly used solution where either bandwidth or low power, or both are principal considerations. SRAM is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM), it does not need to be periodically refreshed, as SRAM uses bi-stable latching circuitry to store each bit. SRAM exhibits data reminisce, but is still volatile in the conventional sense that data is eventually lost when the memory is not powered. SRAM is also easier to control (interface to) and generally more truly random access than modern types of DRAM. An SRAM cell has three different states it can be in: standby when the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have read stability and write-ability respectively. Both conditions become difficult to satisfy in advanced technologies because of the high degree of variability in thin CMOS transistor parameter, essentially technologies beyond 45nm. Increasing the memory size makes the required degree of reliability hard to please. This makes the first challenge for the SRAMs in advanced technology nodes. The power consumption increases with the advanced CMOS technologies. CMOS scaling requires not only very low threshold voltages to retain the device switching speeds, but also RAM ultrathin gate oxides to maintain the current drive and keep threshold voltage variations under control when dealing with short-channel effects.

II. CIRCUIT DESIGN AND ANALYSIS

A. 6 T SRAM cell (Six transistor) Design

The conventional 6T SRAM cell is shown in Fig. 1 , consisting of two cross-coupled inverters which are working as storage element in the circuitry. The storage node OUT and OUTBAR are accessed directly through NM3 and NM2 transistors during read operation. In the read operation, the storage nodes are disturbed because of cross-coupled inverters and bit-line access transistors due to voltage division. So, the data is most vulnerable to external noise during a read operation. For the successful read and write operations the single fin for pullup, two fins for pass transistors and three fins for pull-down transistors are taken means '123' scheme is followed.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

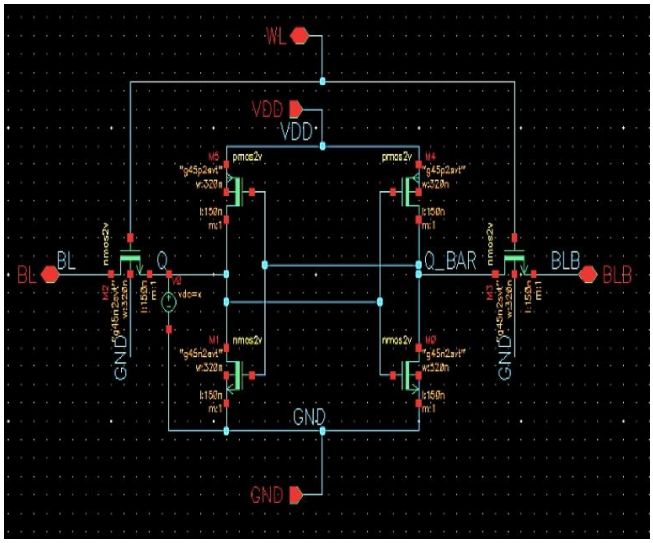


Fig. 1. 6T SRAM Cell

For a successful read operation, the basic condition is that the strength of pull-down transistors must be significantly large than pullup transistor . The BL and BLB lines are pre-charged to VDD. The WL line is pulsed to low to high to read data from the cell which is previously written into cell. The simulated result of read operation has been shown in Fig. 2.

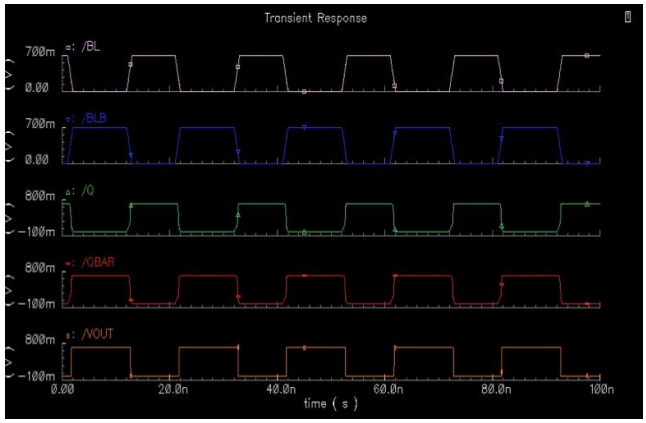


Fig. 2. Read operation 6T SRAM

The simulated write waveforms operation shown in Fig. 3,
the word line (WL) is taken to high (VDD) and then he inverted pulsed inputs are applied to BL and BLB lines. If BL=LOW then BLB=HIGH and outputs are monitored from OUT and OUTBAR.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

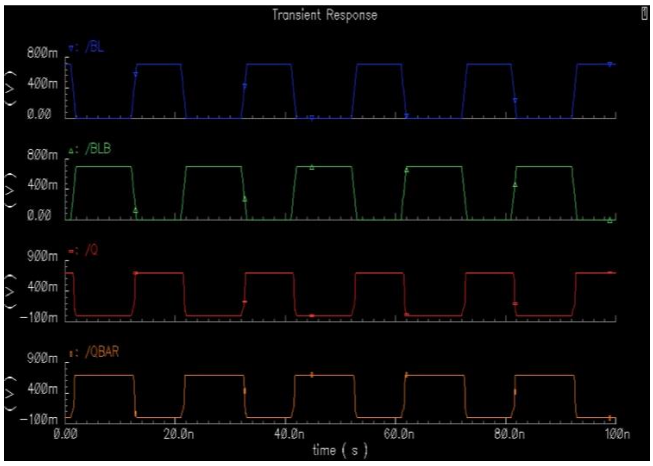


Fig. 3. Write Operation 6T SRAM

For Read Static noise margin shown in Fig. 4, both BL and BLB lines are pre-charged to VDD and word line (WL) is kept at HIGH. A variable voltage source at OUTBAR line is swept from 0 to VDD and outputs are observed form BL and BLB lines.

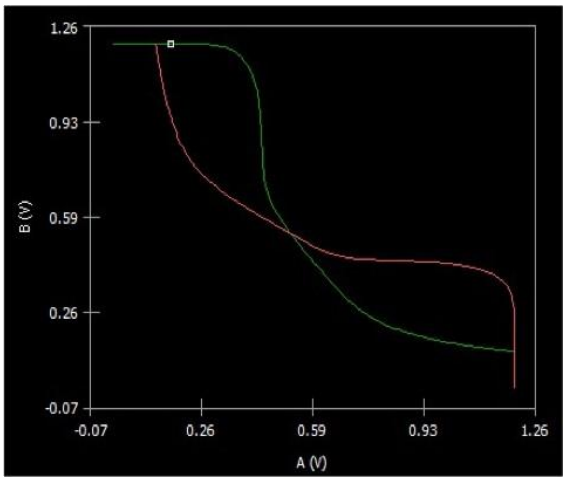


Fig. 4. Read Static Noise Margin

The write static noise margin is evaluated by the combination of RVTC (read voltage transfer curve) and WVTC (write voltage transfer curve) as shown in Fig. 5. The cell beta ratio also plays a vital role for a successful write operation. The both bit-lines are pre-charged to VDD and voltage at OUTBAR node is swept from 0 to VDD and OUT is monitored for RVTC (read voltage transfer curve). WVTC is drawn by applying inverted inputs at bit lines and by sweeping one of the inputs from 0 to VDD, and the outputs are observed form OUT and OUTBAR.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

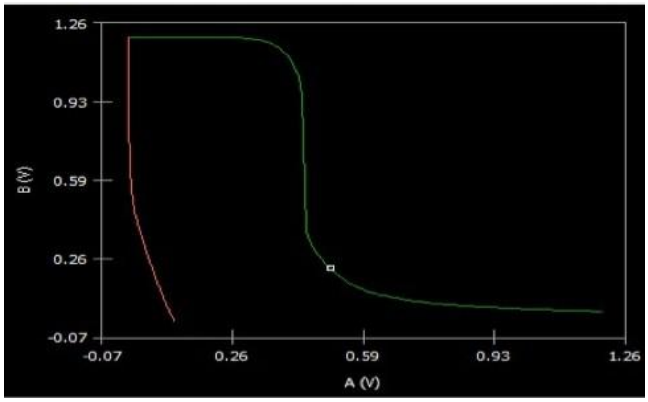


Fig. 5. Write Static Noise Margin

B. 7T SRAM cell (Seven Transistor) Design

In 7T SRAM cell is similar to 6T SRAM cell in place of Vdd of cross coupled inverter onp PMOS transistor is inserted.

When '1' stored in cell, M3 and M2 are ON and there is positive feedback between ST node and STB node, therefore ST node pulled to Vdd by M2 and STB node pulled to GND by M3. When '0' stored in cell M4 is ON and since N node maintained at Vdd by M5 the STB pulled to Vdd, also M2 and M3 are OFF and for data retention without refresh cycle following condition must be satisfied. For satisfying above condition when '0' stored in cell, we use leakage current of access transistors (Ml), especially sub-threshold current of access transistors (MI). For this purpose during idle mode of cell, bit-line maintained at GND and word-line maintained at V Idle.

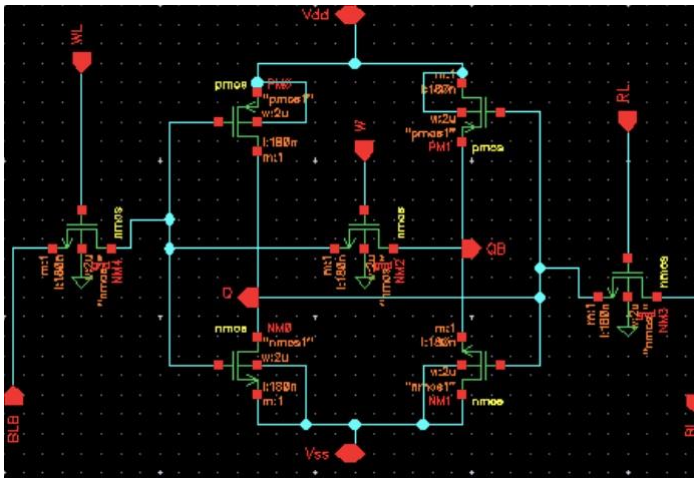


Fig. 6. 7T SRAM Cell

The simulated read waveforms of 7T SRAM cell shown in Fig. 7 . We have performed single ended operation. A pulsed input is applied at Q node. R and W both lines are kept at HIGH and WL is kept at LOW. Output is observed at BLB line.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

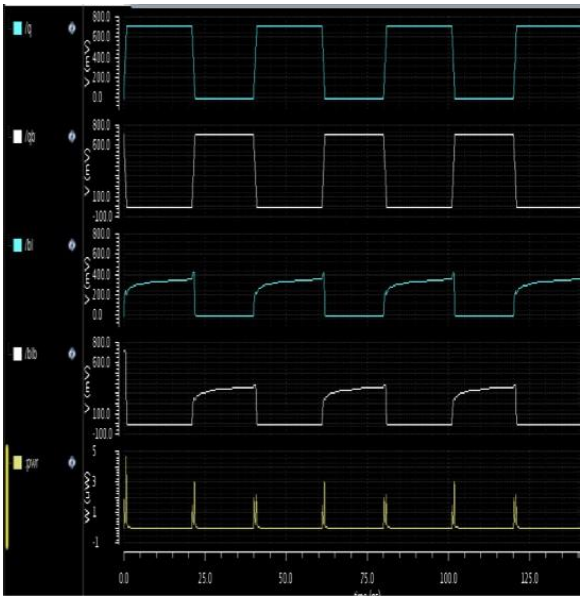


Fig. 7. Read operation 7T SRAM

The simulated write waveforms are shown in Fig. 8. The write operation takes place by cutting off the feedback connection between the inverters. R and W lines are kept at LOW and WL line is kept at HIGH. For single ended operation, a pulsed input is applied at BL and outputs are monitored from Q and QBAR.

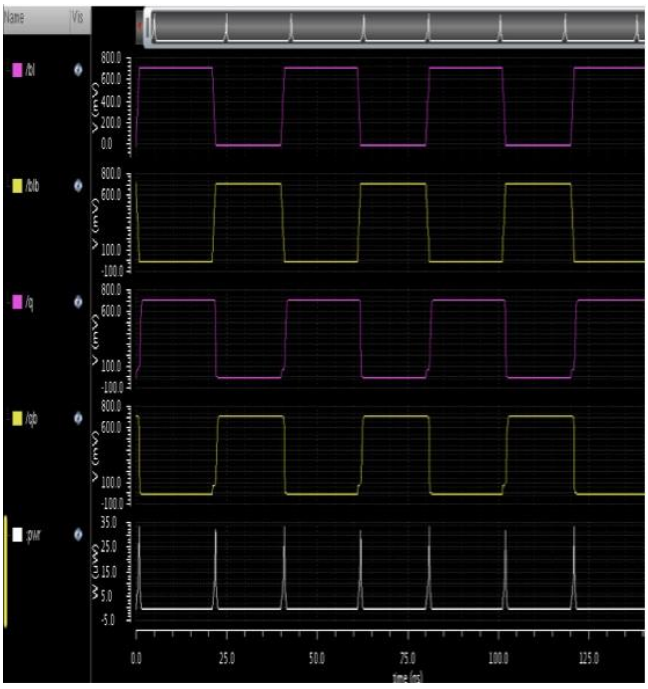


Fig. 8. Write Operation 7T SRAM

The read static noise margin of 7T SRAM cell shown in Fig. 9 The WL and W lines are kept at HIGH and R is kept at LOW. The voltage at node Q is swept form 0 to VDD and BL is monitored for output, same is applied at QBAR to get another curve.

The write static noise margin shown in Fig.10 [8-9], The R and W lines are kept at LOW and WL is kept at HIGH. An input is swept from zero to VDD at BL line. Q and QBAR are monitored for the output nodes. The point at which both

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

curves crosses to each other (cross point) and the difference in potential with VDD at this point will be considered as write static noise margin.

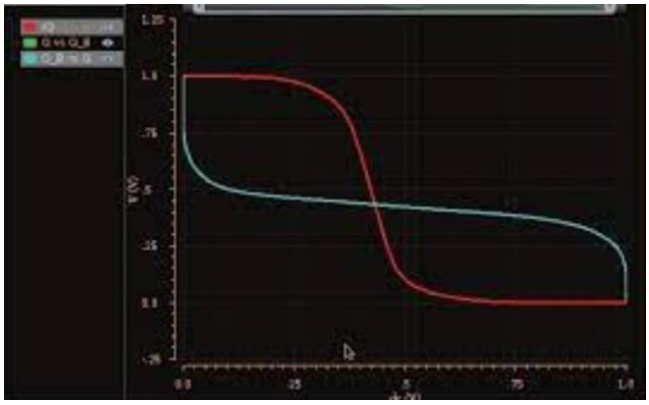


Fig. 9. Noise margin of 7T SRAM

C. 8T SRAM cell (eight transistor) Design

The 8T SRAM cell shown in Fig. 11. An external read buffer circuitry has been introduced which include two more transistors. These transistors help to obtain good SNM. In the 8T SRAM cell write operation takes place in the same way as conventional 6T SRAM cell but the read operation is controlled using RBL and RWL lines.

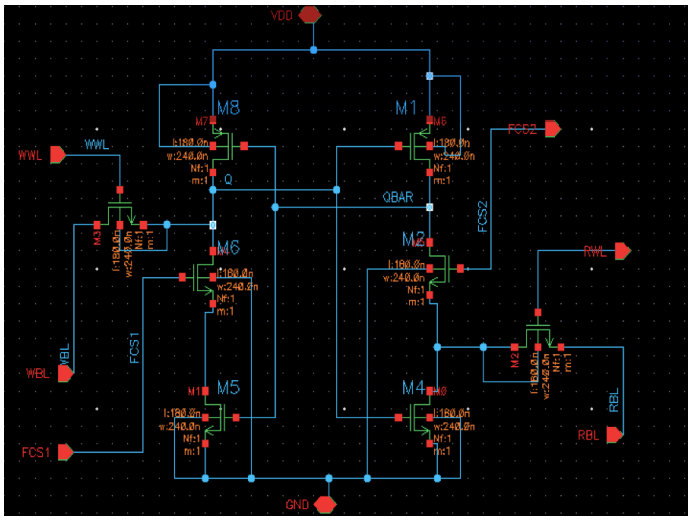


Fig. 11. 8T SRAM cell

The simulated read waveforms of 8T SRAM cell [10] are shown in Fig. 12. The RBL line is pre-charged to VDD and WWL line is kept at LOW. A constant voltage source is placed at QBAR and a pulsed input is applied on RWL line and RBL is monitored for output.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

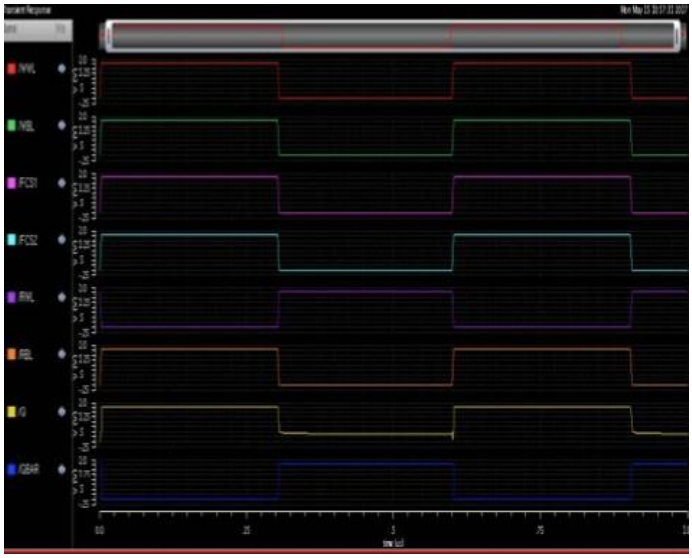


Fig. 12. Read Operation 8T SRAM

The write operation waveforms are shown in Fig. 13 [10]. The write operation in 8T SRAM cell takes place in same way as conventional 6T SRAM cell. In write operation RWL line is kept at LOW and inverted pulsed inputs are applied at WBL and WBLB line. Q and QBAR are monitored for output.

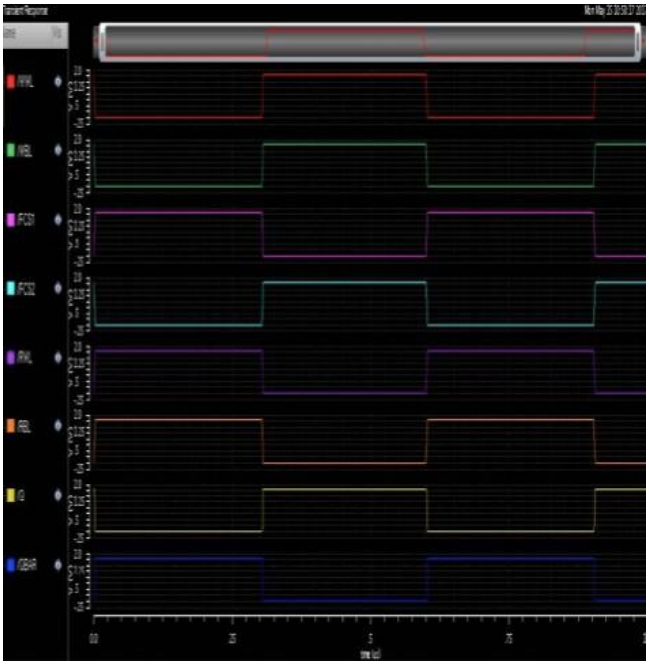


Fig. 13. Write operation 8T SRAM

The read static noise margin of 8T SRAM cell is shown Fig.14
. The WWL line is kept at LOW and RWL kept at HIGH. A voltage source at QBAR swept from zero to VDD and output is monitored at RBL. A square box is fitted into curve to determine the RSNM value.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

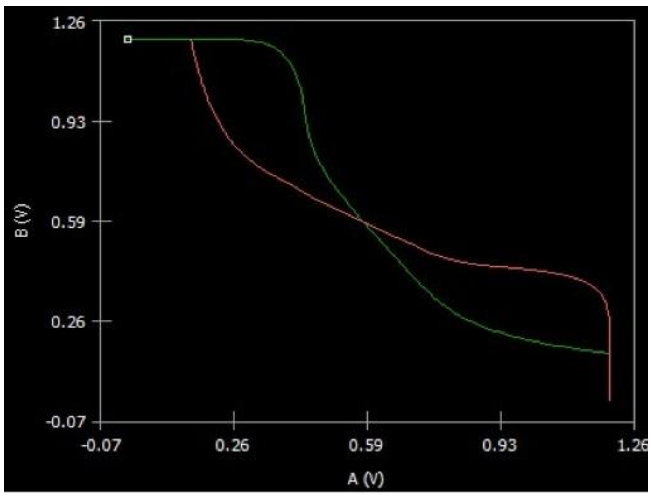


Fig. 14. Read Static Noise Margin

The write static noise margin of 8T SRAM cell shown in Fig. 15 . In this circuit, RVTC is evaluated by keeping RWL line HIGH and a voltage source is swept from zero to VDD at QBAR. RBL is monitored for RVTC. For WVTC, WWL line is kept at HIGH and inverted inputs are applied through WBL and WBLB. A voltage source at WBL is swept from 0 to VDD. Q and QBAR are monitored for the output.

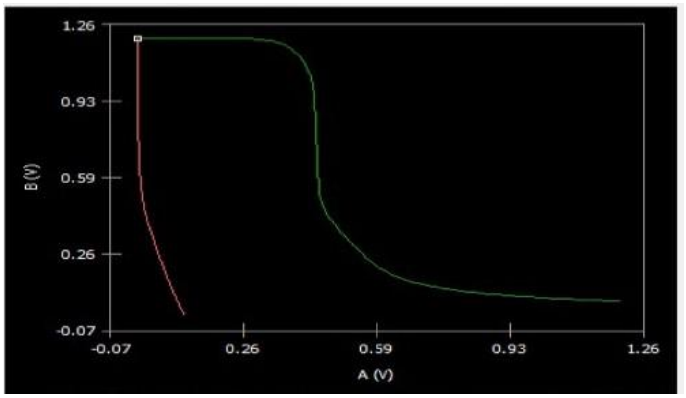
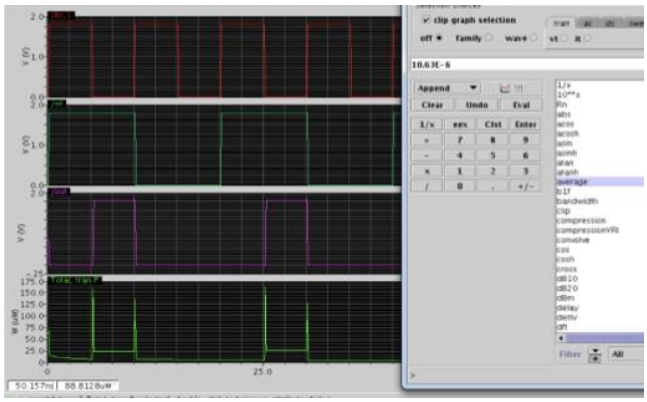


Fig. 15. Write Static Noise Margin



All the above calculation and Simulations are done at 250mV of VDD, and pulsed input time period was taken as 20ns and pulse width as 10ns.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

The power consumption of Static Random Access Memory cell depends on consumption of the power which used to perform the operation of the transistor. Dynamic power consumption in SRAMs is consumed due to the charging and discharging capacitances during read and write operation and during each cycle of SRAM particular amount of Energy is drawn from the power supply and dissipated. For each cycle the power consumption is depended on the type of operation (read or write).

A average power dissipation of any device over one period can be obtained by following expression.

$$P = [(1/T) \int^{T} Idt] \times V$$

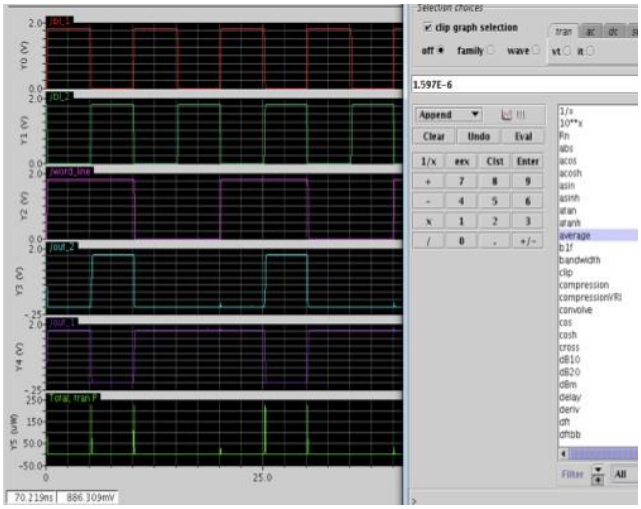


Fig. 16. Simulated results for power consumption of 6T SRAM cell

Fig. 17. Simulated results for power consumption of 7T SRAM cell

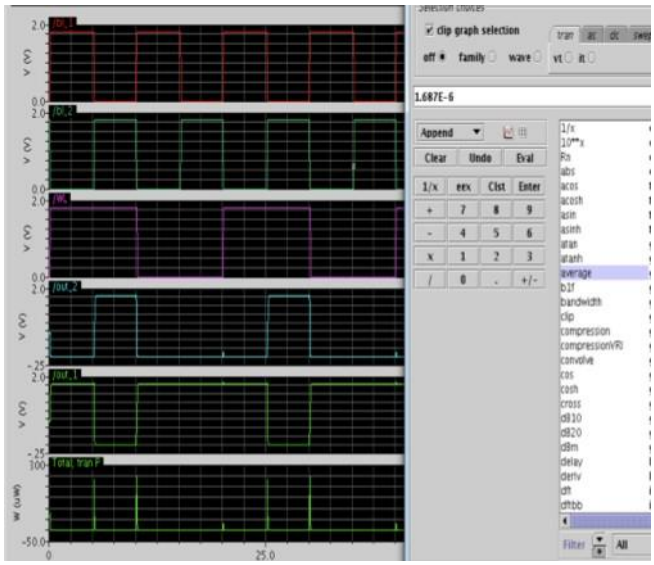


Fig. 18. Simulated results for power consumption of 8T SRAM cell

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.39 ⁜ Vol. 11, Issue 9, September 2022

DOI: 10.17148/IJARCCE.2022.11906

Table 1 Comparison of power consumption

Parameter	6T	7T	8T	9T
Power consumption (µW)	1.597	10.63	1.68	1.86

IV . CONCULSION

From all the above simulations we can compare performances of the SRAM cells. In the overall 7T is having a good performance except write delay but this cell is operating in the single ended operation, and the single ended is not considered as reliable as differential. At the benchmark of speed 6T cell is having good performance but its read power consumption is too high as compared to other topologies. At the benchmark of power consumption 7T cell having best performance but its operation mode was single ended also write delay is high and at the benchmark of SNM 7T is again a better option but its operation is single ended so the 8T cell is preferable in WSNM.

REFERENCES

[1] Manish Verma, Shubham Yadav and Manish Kurre, "Comparitive analysis of sram cell topologies at 65nm technology," International Research Journal of Engineering and Technology (IRJET), 2018

[2] Hare Krishna Kumar and V.K. Tomar, "Stability analysis of Subthreshold 6T SRAM cell at 45 nm for IoT application," International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-8 Issue-2, July 2019.

[3] Fossum J.G. and Trivedi V.P.," Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs-Cambridge University Press (2013)".

[4] Reeya Agrawal and V.K. Tomar, "Analysis of Low Power Reduction Techniques On Cache(SRAM) Memory," 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), 2018.

[5] C.Premalatha, K.Sarika and P.Mahesh Kannan, "A Comparative Analysis of 6T, 7T, 8T and 9T SRAM Cells in 90nm Technology," IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), 2015.

[6] Sagar Joshi and Sarman Hadia, "Design and Analysis for Low power CMOS SRAM cell in 90nm technology using cadence tool", International Journal of Advanced Research in Computer and Communication EngineeringVol.2,lssue 4, pp. 1814-1817,April-2013.

[7] Christiensen D.C. Arandilla, Anastacia B. Alvarez, and Christian Raymund K. Roque," Static Noise Margin of 6T SRAM Cell in 90- nm CMOS," UKSim 13th International Conference on Modelling and Simulation,2011.

Bhawna Rawat, Kirti Gupta and Nidhi Goel," Low Voltage 7T SRAM cell in 32nm CMOS Technology Node," International Conference on Computing, Power and Communication Technologies,2018.