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DESIGN OF LOW POWER HIGH SPEED 16T CMOS FULL ADDER IN CPTL LOGIC

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Abstract: Full adder is a digital logic circuit that implements addition of binary numbers. The circuit of full adder forms a basic component of ALU (Arithmetic Logic Unit) in Microcontrollers and Microprocessors. They are used in concepts like Fast Fourier Transform in DSPs.

In order to generate memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of full adders. Full adders are a part of Graphics Processing Unit for graphics related applications.

The objective of this project is to analyze the 16T low power CPTL full adder and optimize its power dissipation and propagation delay by simulating the circuit in 45 nm and 32 nm processes. By implementing designs across successive process generations, 2-dimensional design space is explored for low power and high performance. The performance of full adder is validated across a range of frequencies upto 1.25 GHz. The SPICE based simulations are carried out using LTspice

Keywords: VLSI, CMOS, CPTL,Full adder,ALU, Power, Delay.

I. INTRODUCTION

Today, CMOS technology is the dominant IC fabrication technology in VLSI industry and is used for making high-end microprocessors, microcontrollers, memory modules, sensors, and Application Specific Integrated Circuits (ASICs). Relentless scaling of the MOSFET over the decades has been the technology driver that has made System-on-chip (SoC) implementation a reality today. The advent of SoC-driven mobile electronics requires ultra-low power consumption to support the mobility function in addition to reasonably high performance to support multimedia and gaming applications on the move.

Full Adder

The addition of n-bit binary numbers requires the use of full adders, and the process of addition proceeds on a bit-by-bit basis, LSB to MSB. After the least significant bit, addition at each position adds not only the respective bits of the words but must also consider a possible carry bit from addition at the previous position.

Design of Full Adder

A full adder, as shown in Fig. 1.1, is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs and two outputs. Two of the input variables, denoted by A and B, represent the two bits to be added. The third input C, represents the carry from the previous significant position. The truth table of the full adder is listed in Table 1.1. When all input bits are 0, the outputs are 0. The Sum output is equal to 1 when only one input is equal to 1 or when all three inputs are equal to 1. The $Carry$ output has a carry of 1 if two or three inputs are equal to 1. The simplified Boolean expressions for Sum and Carry are given by Eq. (1.1) and Eq. (1.2).

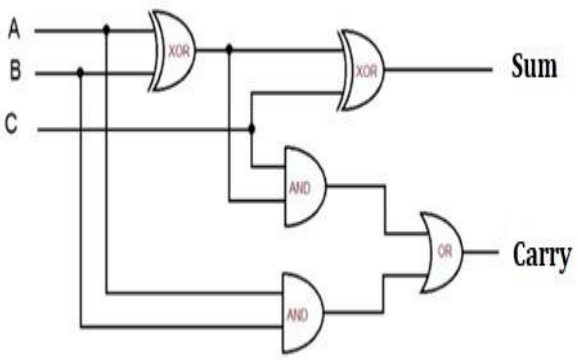

Figure 1.1: Full adder logic gate circuit.

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Sum = A′B′C + A′BC′ + AB′C′ + ABC (1.1)
Carry = AB + AC + BC (1.2)

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1.1: Truth Table for Full Adder.

An n-bit binary adder is a digital circuit that produces the arithmetic sum of two n-bit binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of the next full adder in the chain of n-stages. [1]

CMOS Logic Style

In CMOS (Complementary Metal-Oxide Semiconductor) technology, both N-type and P-type transistors are used to realize logic functions. CMOS technology is the dominant semiconductor technology for microprocessors, memories, and application-specific integrated circuits (ASICs). The main advantage of CMOS over NMOS and bipolar technology is the low power dissipation.

Pass transistor Logic Style

The drain/source terminals of pass transistors are not connected to power supply rails, but the signal passes through them. The basic difference between pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads.

Introduction to Pass-Transistor Logic

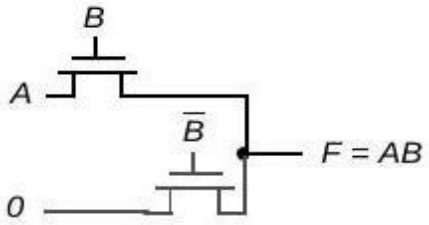

Figure 1.3: Implementation of AND gate.

A popular and widely-used alternative to complementary CMOS is pass-transistor logic, which attempts to reduce the number of transistors required to implement a logic function by allowing the inputs to drive gate terminals as well as source/drain terminals. This is in contrast to logic families which only allow inputs to drive the gate terminals of MOSFETS.
Fig. 1.3 shows an implementation of the AND function constructed that way, using only NMOS transistors. In this gate,

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if the B input is high, the top transistor is turned on and copies the input A to the output F. When B is low, the bottom transistor is turned on and passes a 0.

The switch is driven by $\bar{B}$ seems to be redundant at first glance. Its presence is essential to ensure that the gate is static, this is, that a low-impedance path exists to the supply rails under all circumstances, or, in this particular case when B is low. This approach promises that fewer transistors are required to implement a given function. For example, the implementation of the AND gate in Fig. 1.3 requires 4 transistors (including the inverter required to invert B), while a static CMOS implementation would require 6 transistors. The reduced number of devices has the additional advantage of lower capacitance. Unfortunately, as discussed earlier, an NMOS device is effective at passing a 0 but is poor at pulling a node to V_{DD}. When the pass transistor

CMOS Pass Transistor Logic (CPTL)

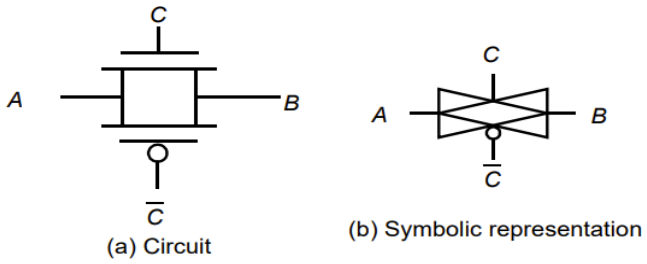

Figure 1.4: CPTL.

The most widely-used solution to deal with the voltage-drop issue is the use of CPTLs. It builds on the complementary properties of NMOS and PMOS transistors: While NMOS devices pass a strong 0 but a weak 1, PMOS transistors pass a strong 1 but a weak 0. The CPTL combines the best of both device flavors by placing a NMOS device in parallel with a PMOS device to build CMOS pass transistor, as shown in Fig. 1.4. The control signals to the CPTL (C and $\bar{C}$) are complementary. The CPTL acts as a bidirectional switch controlled by the gate signal C. When C = 1, both MOSFETs are on, allowing the signal to pass through the gate and when C= 0, both MOSFETs are off, and signal does not the output node.

II. DESIGN AND IMPLEMENTATION OF 16T FULL ADDER CIRCUIT

16T CPTL Full Adder

The 16T full adder in CPTL style, shown in Fig. 1.5, consists of low-power XOR and XNOR gates, pass transistors, and CPTLs. The adder offers high speed and low power consumption than the previous implementations of the full adder. Instead of using an inverter to generate the complementary signal of (A ⊕ B), a 4 transistor XNOR circuit is employed to eliminate the possible short circuit power consumption introduced by the inverter. Its area and PDP are less than the 20T TGCMOS design but slightly higher delay when compared to 20T TGCMOS design.

As in the case of the low power circuit, cascading full adders lead to an overall slight increase in the propagation delay which becomes excessive for long chains of full adders. This drawback is solved in the TG drive cap. Output buffers which interrupt the CPTL chain when cascading full adders are added.

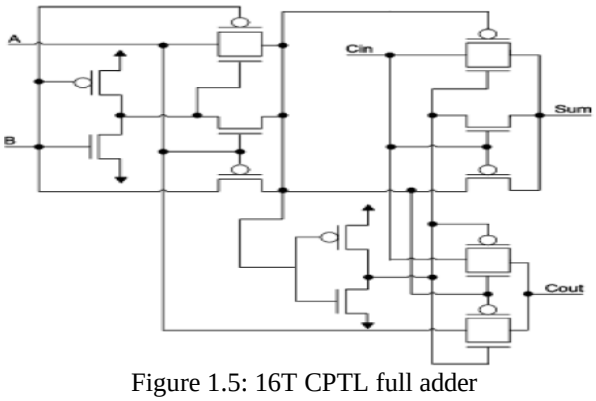

Figure 1.5: 16T CPTL full adder

A 16T full adder in CMOS pass transistor logic style, shown in Fig. 1.5, is implemented in PTM (Predictive Technology

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model) 45 nm and 32 nm low power process. The adders are simulated using the LTspice tool to optimize the design for power and speed simultaneously and characterize its area. The key process parameters like the VDD, and V_{th0} of NMOS/PMOS are tabulated in Table 2.1.

The 16T FA circuit in CMOS pass transistor logic style in 45 nm and 32 nm process are successfully simulated

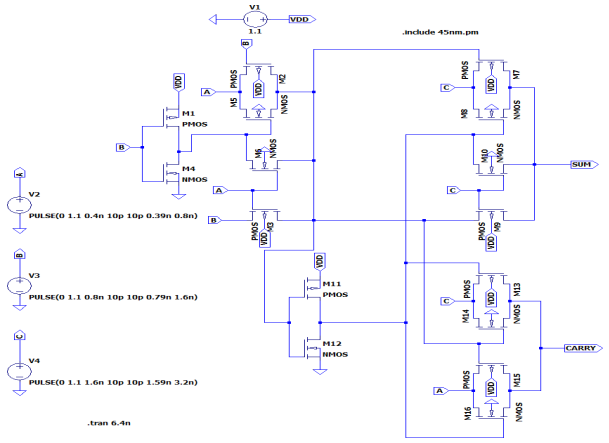

Figure 1.6: Schematic of full adder in CMOS pass transistor logic style for 45 nm.

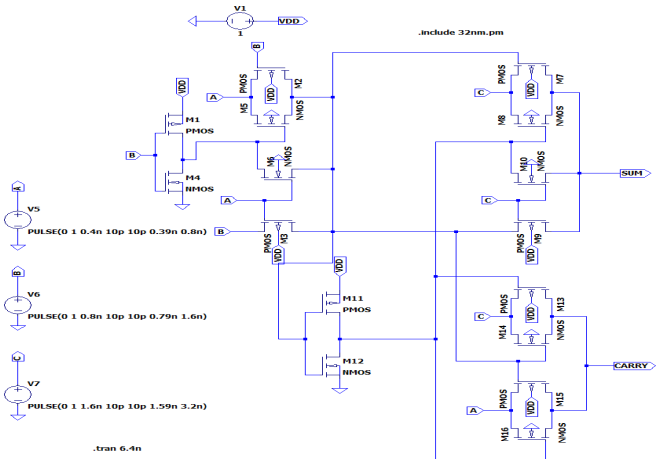

Figure 1.7: Schematic of full adder in CMOS pass transistor logic style for 32 nm.

III.RESULTS AND DISCUSSION OF 16T FULL ADDER

The simulations of 16T full adder CMOS pass transistor logic style in 45 nm and 32 nm are performed to evaluate power dissipation and propagation delay. Transient analysis is performed using LTspice circuit simulator.

Simulations are performed for operating frequencies 0.5 GHz and 1.25 GHz of the LSB. The pulse inputs for the schematic are V(a), V(b), and V(c) and their corresponding outputs are V(sum) and V(carry).

Simulations of 16T Full Adder in 45 nm process

The transient response and average power dissipation of 16T full adder in *45 nm process* at 0.5 GHz frequency of the LSB is shown in Fig. 3.1 and Fig. 3.2 demonstrate the transient response and average power dissipation of 16T full adder in 45 nm process at 0.5 GHz and 1.25 GHz frequency respectively.

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Simulations of 16T Full Adder in 32 nm process

The 16T full adder in CPTL is designed in *32 nm process* and simulations are repeated to generate the transient response and average power dissipation at operating frequencies of 0.5 GHz and 1.25 GHz frequency shown in Fig. 3.3 to Fig. 3.4, respectively.

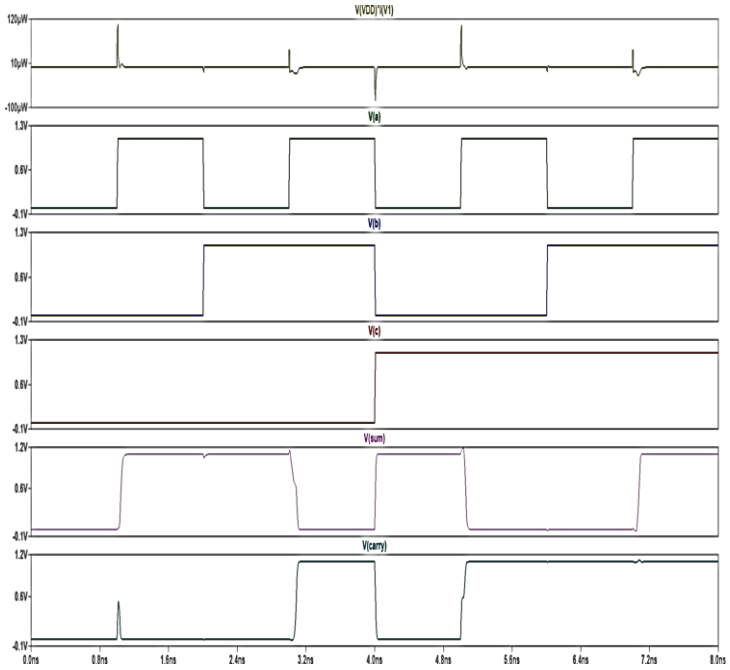

Figure 3.1: Transient response of 16T full adder in CPTL logic style in 45 nm at 0.5 GHz.

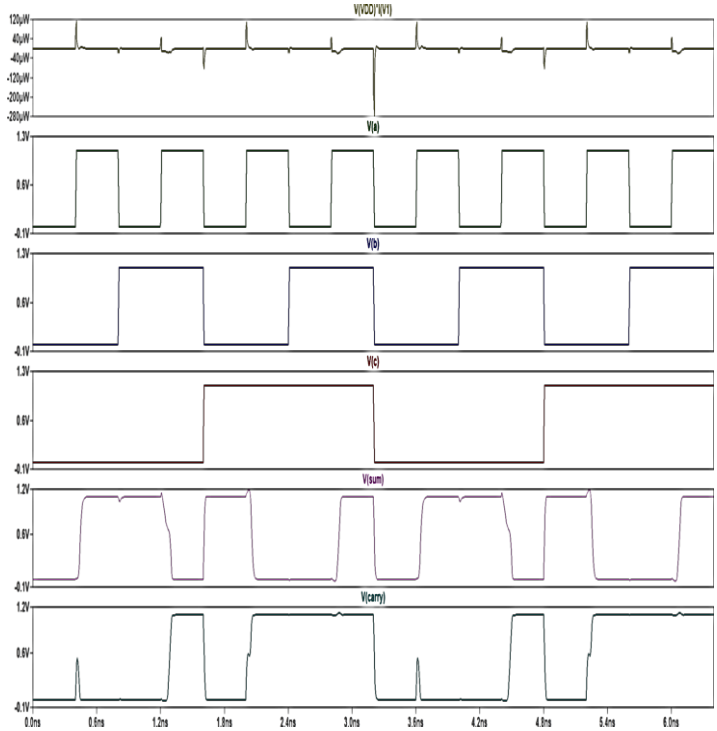

Figure 3.2: Transient response of 16T full adder in CPTL logic style in 45 nm at 1.25 GHz.

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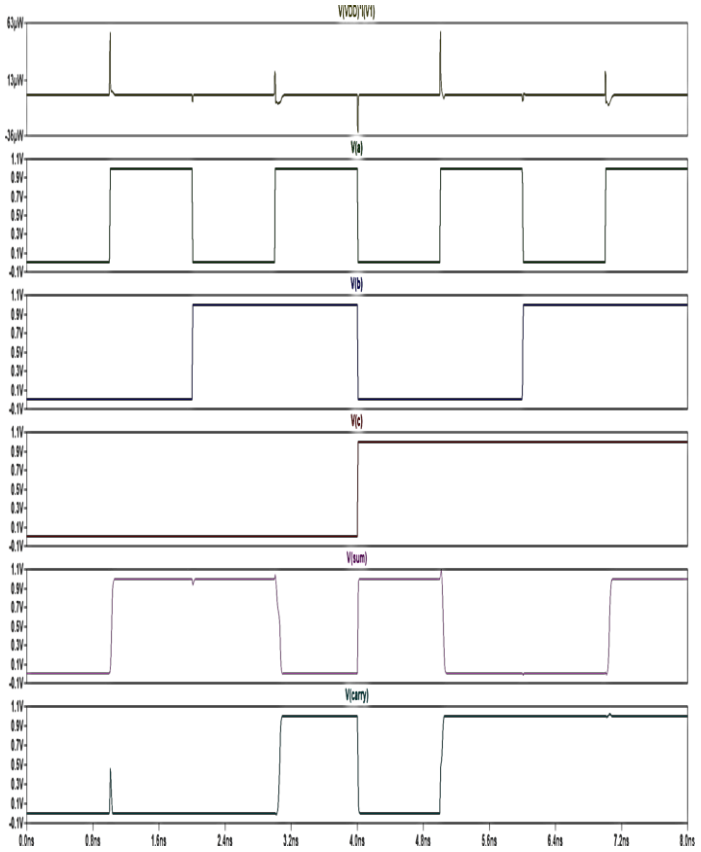

Figure 3.3: Transient response of 16T full adder in CPTL logic style in 32 nm at 0.5 GHz.

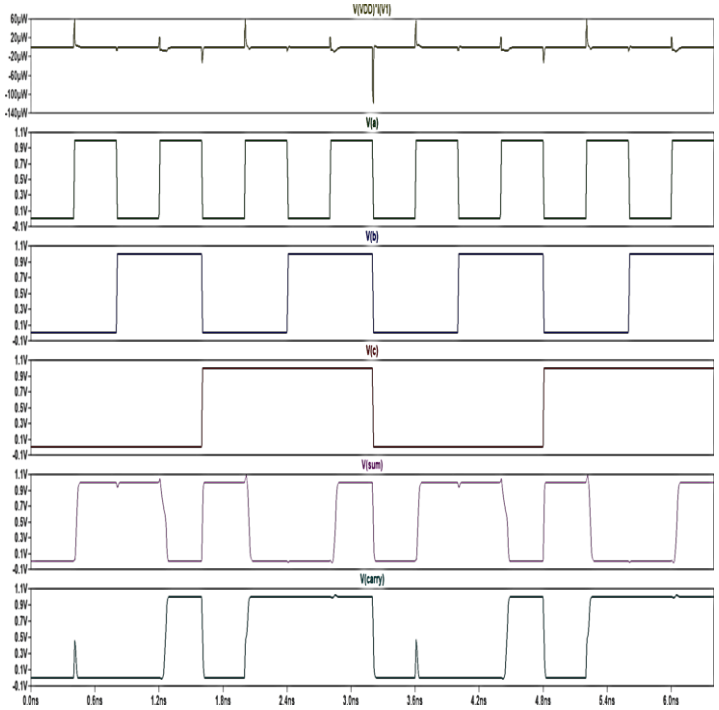

Figure 3.4: Transient response of 16T full adder in CPTL logic style in 32 nm at 1.25 GHz.

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IV SIMULATION RESULTS AND DISCUSSION

Simulation results demonstrate that with increasing operating frequency, the output signal waveforms exhibit increasing amounts of distortion, inclusive of glitches. However, the voltage levels are not significantly impacted, indicating reasonably good noise margins.

The area, power dissipation, propagation delay for sum and carry, and their PDP product are tabulated in Table 3.1 for 16T CPTL full adder implemented in 45 nm and 32 nm PTM process. The delay reduction, power savings, and area savings are computed as the design moves from 45 nm process to the 32 nm process.

Technology Parameters	**45 nm**	**32 nm32332 nnmnm**
Power Dissipation (nW)	20.151	10.194
Time Delay $\tau\tau_{pLH}$ Sum (ps)	14.867027	14.591351
Time Delay $\tau\tau_{pHL}$ Sum (ps)	46.021622	44.789337
Time Delay $\tau\tau_{pLH}$ Carry (ps)	50.555556	49.921251
Time Delay $\tau\tau pHL$ Carry (ps)	**18.745946**	
Technology Parameters	**45 nm**	**32 nm**
Propagation Delay Avg Carry (ps)	30.4443245	29.690344
Propagation Delay Avg Carry (ps)		33.9444095
PDP - Sum (×1tt^{-22^1}J)	34.650751	302.6633667
PDP - Carry (×1tt^{-22^1}J)	613.483583	346.0293104
Area (× 1$tt^{-1^{11}}$ mm^{22})	106.2	60.16

Table 3.1: Performance metrics of 16T CPTL full adder at 45 nm and 32 nm PTM process.

The power dissipation of 16T CPTL full adder in 45 nm technology is *20.151 nW* and in 32 nm it is *10.194 nW*, representing a power savings of 49.41%.

The rising edge delay in generating the sum output $\tau\tau_{pLH}$ is 14.87 ps in 45 nm technology and 14.59 ps in 32 nm technology, representing a delay reduction of 1.88%. The falling edge delay in generating the sum output $\tau\tau_{pHL}$ is 46.02 ps in 45 nm technology and 44.79 ps in 32 nm technology, representing a delay reduction of 2.67%.

Similarly for carry output, the rising edge delay $\tau\tau_{pLH}$ is 50.55 ps in 45 nm technology and 49.92 ps in 32 nm technology, representing a delay reduction of 1.25%. However, the falling edge delay in generating the carry output $\tau\tau_{pHL}$ is 18.75 ps in 45 nm technology and 17.97 ps in 32 nm technology, representing a delay reduction of 4.16%.

Considering the Power Delay Product (PDP) as the figure of merit of 16T full adder, PDP for sum output is 613.48 nW.ps in 45 nm technology and 302.66 nW.ps in 32 nm technology, representing a PDP savings of 50.67%. However, for the carry output, the Power Delay Product (PDP) is 698.25 nW.ps in 45 nm technology and 346.03nW.ps in 32 nm technology, representing a PDP savings of 50.44% .The area of 16T CPTL full adder in 45nm technology is $106.2\times10^{-15}m^2$ and $60.16\times10^{-15}\ m^2$, representing an area reduction of 43.35%.

From the discussion above, the contribution of 32 nm process over 45 nm process is significant to the extent of 50 % savings in PDP product, the savings coming almost entirely due to the power savings. High performance is guaranteed with a negligible delay reduction. This is attributed to the selection of low power 45 nm and 32 nm process for the design to be deployed for low power applications. Further, the area reduction of 43 % aids in low power portable electronics.

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V.CONCLUSION AND FUTURE WORK

Conclusion

A low-power and high-performance 16T CPTL full adder circuit is designed and optimized for low power mobile applications. The 16T full adder is a combination of inverters and CMOS pass transistors.
Simulations have been performed on the LTspice tool using 45 nm and 32 nm PTM processes to assess the optimized design for power dissipation and delay. The optimization is done in such a way that the trade-off between power and speed is minimal. Waveform distortions have been reduced to the maximum extent possible but there are still a few glitches at higher frequencies due to which the frequency of operation is capped at 1.25 GHz. Good noise immunity and high voltage swings have been achieved by optimizing the design. From the simulated results, the amount of power savings achieved with 32 nm against 45 nm is 49.41 % and PDP with 32 nm against 45 nm is 50.67%. High performance is guaranteed with a negligible delay reduction. Further, the area reduction of 43 % aids in low power portable electronics.

Future work

The design can be optimized to achieve further power savings by generating glitch-free output and further enhance the operating frequency beyond 1.25 GHz.

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