PERFORMANCE ANALYSIS OF INTERCONNECT CIRCUIT TECHNIQUES FOR HIGH-SPEED VLSI INTERCONNECTS

Manjula Jayamma[1], N. Ramanjaneyulu[2], Rama Subbaiah Boya[1], Y. Mallikarjuna Rao[3]

SVR Engineering college, Nandyal, Andhra Pradesh-518501, India[1]

Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal, India[2]

Santhiram Engineering College, Nandyal, Andhra Pradesh-518501, India[3]

Abstract: The aggressive technology scaling in VLSI leads to decrease the size of chip. Such continual miniaturization of VLSI devices has strong impact on the interconnects in several ways. Interconnects in high-speed applications suffer from crosstalk, signal delay and ground noise, causing degradation of system performance. Thus, interconnects are becoming a limiting factor in determining circuit performance. This paper presents a comparative study on different interconnect circuit techniques for on chip interconnects.

We have compared different circuit structure by placing on RC and RLC interconnects. In this delay benefit for current sensing increases with an increase in wire width. Unlike repeaters, current sensing does not require placement of buffers along the wire and it eliminates any placement constraints. Out of all these techniques a differential RLC current mode signaling circuit insertion has offered the less amount of energy. All the circuits are simulated and compared different parameters such as power, delay and energy by using microwind in 45nm technology.

Keywords: Interconnect, repeaters, wire, Current mode, differential signaling, clamped bit line Sense Amplifier, energy dissipation.

I. INTRODUCTION

As very large scale integration (VLSI) progresses into very deep submicron (VDSM) interconnect play an increasing role in the overall performance and power consumption of high-performance chips. With scaling, wires will get electrically longer, increased RC product. Wire delay will dominate device delay and create a performance bottleneck [1]. With the increase in number of wires and their resistance, the amount of resources required to drive them also increases.

Thus, leading to higher power dissipation. Due to a higher wire aspect ratio and smaller line spacing, the coupling capacitance between neighboring wires becomes the major component of the total wire capacitance. Technology scaling trends have also resulted in a significant increase in inductive effects in interconnects [2], [3].

Inductance also impacts the wire width optimization [4]. Inductive and capacitive coupling make interconnect coupling noise significant and cause signal integrity concerns. Interconnect scaling is thus considered to be the real challenge to CMOS scaling [5], [6].

With the increase in interconnect resistance, delay-optimal repeater insertion fails to meet the required performance. The number and size of repeaters are on an increase with technology scaling resulting in increased power dissipation. This paper presents a comparative study on different interconnect solutions such as repeater insertion, voltage mode signaling, current mode signaling, differential RC current mode signaling, differential RLC current mode signaling, to get less delay, signal swing, power and as well as energy for faster on-chip interconnects.

II. DIFFERENT INTERCONNECT SOLUTIONS

1. REPEATER INSERTION:

In Repeater Insertion, Repeaters are inserted into interconnects lines to reduce the total Propagation Delay [10], [11]. Applying this method to the general case of an RC, RLC interconnect lines to observe energy dissipation.
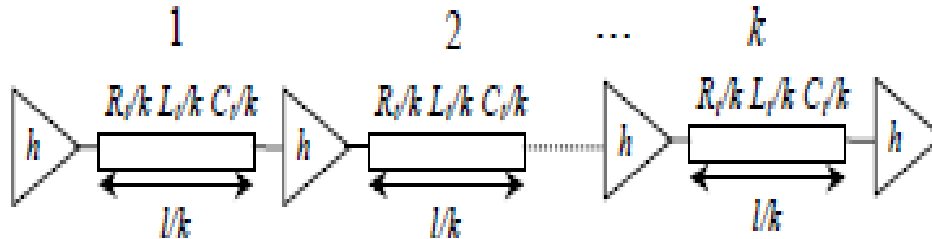

Fig 1.1 Repeater insertion technique

Repeaters are used to divide the interconnect line into K sections as shown in the figure. The repeaters are each uniformly the same size and h times larger than a minimum size buffer. The repeater output impedance is R_0/h and the input capacitance of the buffer C_L is $hC0$. Inserting Repeaters at regular intervals changes the dependence of delay on the wire length from quadratic to linear.

For limiting case, L→0, propagation delay reduces to $0.37RCl^2$ which is quadratic to the delay. For the limiting case where R→0, the propagation delay is given by $l\sqrt{(LC)}$ which is a linear. Thus the quadratic dependence of the propagation delay on the length of an RC line approaches a linear dependence as "inductance effect "increase [7].An optimal repeater insertion solution is determined by the size and number of repeaters inserted.

Several drawbacks are present in this technique such as Repeaters insertion solution requires a regular placement of uniformly sized buffers. If the repeaters are inserted at regular intervals, repeater chain performance degrades [9], [8]. Repeaters account for a significant proportion of the total chip power consumption. With increase in wire resistance the number of repeaters required to drive the wire increases. The addition of repeaters along the wire adds device switching delay, which limits the achievable delay reduction. The experimental results shows that the amount of energy dissipated in RC line is more compared to RLC line, due to the inductance effect in RLC line which reduces the delay. Thus the overall energy dissipation reduces. Both the wire models are simulated and compared.

2. VOLTAGE MODE SIGNALING:

In voltage mode signaling, the receiver provides high impedance termination (R1=∞).The signal on the interconnect changes over a full voltage swing and the sensing circuit at the destination determines the signal state by using this voltage value.[8] An inverter drives a interconnect, charging the wire capacitance that leads to a voltage buildup along the line. Another inverter senses the voltage and provides a high impedance termination.

The output is terminated by an open circuit. This high input impedance of the receiver gives rise to high input capacitance which leads to high charging and discharging time for RC interconnect chain. Hence voltage mode signaling has large delay. Due to high input impedance at the receiver, the charge accumulated at the input of the receiver does not get effective discharge path to ground as a result this may cause electrostatic induced gate oxide break down[8], [12]. The drawbacks of voltage-mode signaling including low signal swing, high switching noise injection, high sensitivity to supply voltage fluctuation and ground bouncing. These can be avoided in current mode signaling.
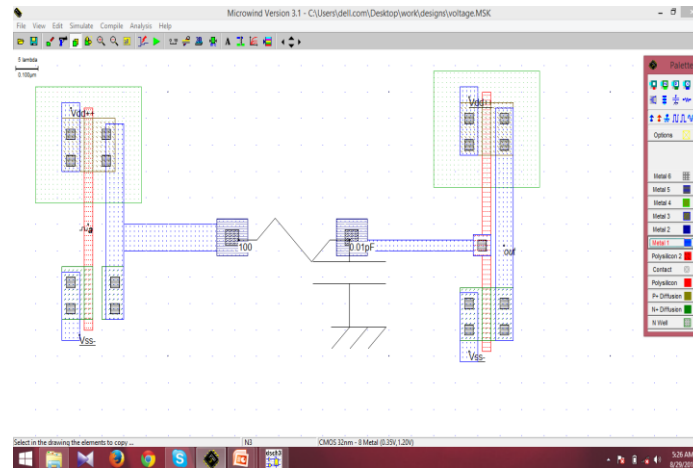
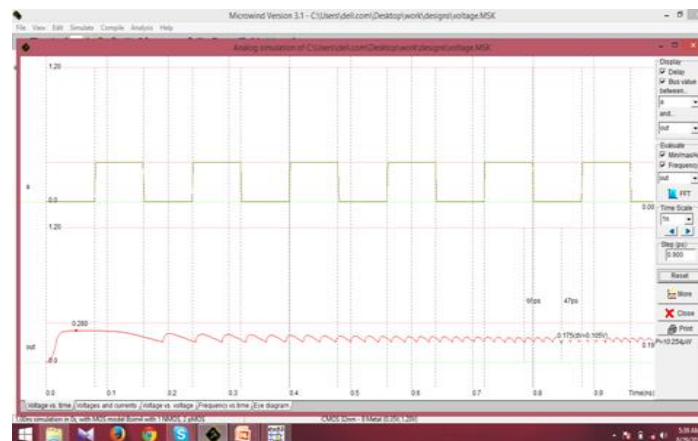**Fig 2.1 Implementation of voltage mode signaling.**

Fig 2.2 Simulation output of voltage mode signaling.

3. CURRENT MODE SIGNALING:

Current sensing or current mode signaling determines the logic value transmitted on a wire based on the current through the wire. In current mode signaling the important design variables that affect energy dissipation, performance are termination impedance and driver output resistance as well as supply voltage [20]. In current sensing, the line is terminated by a short (Rl=0) as opposed as open in voltage sensing. This short helps avoiding of charging of wire capacitance, thus saving power and time.

The advantages of current mode signaling are low voltage, small propagation delay, signal integrity, low power and low switching noise [17], [18]. But current mode signaling requires a special receiver circuit as compare to the conventional CMOS inverter used in voltage sensing. Also, the low impedance path to ground leads to static power dissipation [8], [13]. The experimental results show that the amount of power dissipation and delay is reduced.
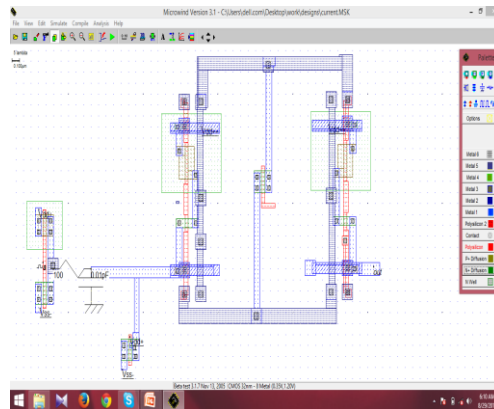
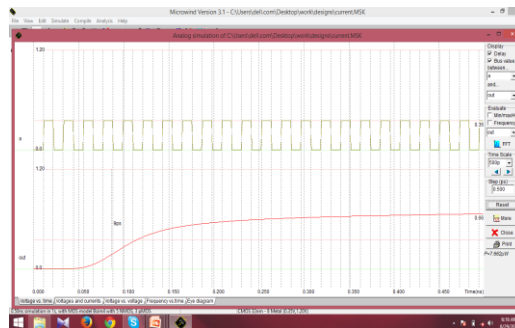**Fig 3.1 Implementation of Current mode signaling.**

Fig 3.2 Simulation output of Current mode Signaling.

There are two types of current mode signaling. They are Single Ended Current mode Signaling, Differential Current mode signaling. In single ended current mode signaling, the number of inputs is constrained to one. Whereas in differential current mode signaling the number of inputs are two. Single ended sensing has been explored for crossbars and on chip interconnects. Although single ended sensing consumes less routing area, it is extremely sensitive to noise as compared to differential sensing. Analytical studies have shown that current-sensing can provide significant delay and power benefits for interconnects [8], [15]. Due to its robustness toward noise, differential current-sensing is preferred over single-ended sensing or single ended current mode signaling.

4. DIFFERENTIAL RC CURRENT MODE SIGNALING

Current Sensing Technique was first proposed for Sense Amplifiers in the memories. The proposed sensing technique uses less power and faster than a differential voltage sense amplifier. Blalock and Jaeger presented a current mode sensing scheme for Dynamic RAMs using clamped bit line sense Amplifier. The use of current sensing technique allows highly capacitive bit lines to be clamped at a fixed voltage, thus allowing faster sensing. Since large capacitance associated with the bit lines are not charged or discharged, this technique consumes less power [8], [19].

The operation of the modified clamped bit line sense amplifier (MCBLSA) is as follows on assertion of EQ signal the two outputs equalize. An equal amount of current flows through the two legs of the receiver. A differential current applied to inputs breaks the metastable balance. When EQ is deserted, the cross coupled inverter pair switches, thus giving a voltage output determined by the differential current between two inputs. The desired low impedance termination for current sensing is provided by the "always on" transistors M5 and M6 of the receiver. The driver consists of cascaded inverters designed using "factor of four"(FOR) sizing rule. The driver and the load are of minimum size inverters, this is because to observe maximum transfer. The interconnect is modeled as a distributed RC network.
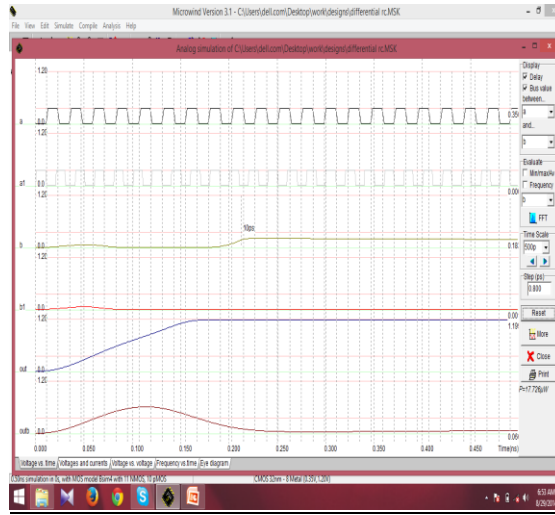
Fig 4.1 Simulation output of Differential RC Current mode Signaling.

5. DIFFERENTIAL RLC CURRENT MODE SIGNALING

The differential current mode signaling with RLC interconnect consist of a sense Amplifier, Enhancement mode linear Resistor, RLC interconnect, Driver and load termination. The use of sense Amplifier is it allows highly capacitive bit lines to be clamped at a fixed voltage that allows faster sensing. Since large capacitances associated with the bit lines are not charged or discharged consumes less power [21], [22].

Enhancement mode NMOS linear resistor is used instead of depletion mode transistor this is because dynamic range of enhancement mode is more compare to depletion mode. In depletion mode transistor a fixed and limited dynamic range within the absolute value of the threshold voltage [16].
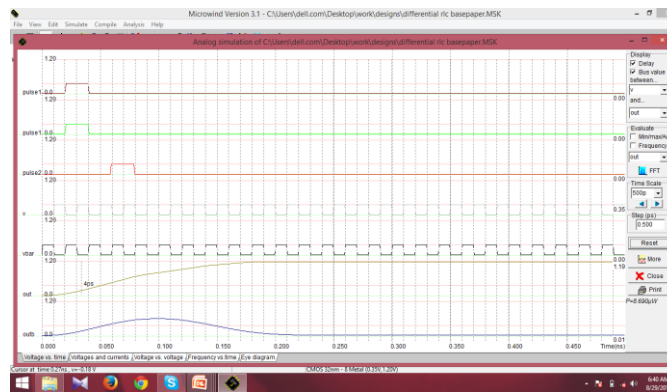

Fig 5.1 Simulation output of Differential RLC Current mode Signaling.

The amount of dissipation of energy depends on driver, receiver and wire .The wire effect on energy dissipation is of both wire width and wire length. The following tables show the variation of energy based on wire width, length, driver and receiver. Thus it is observed that the amount of energy dissipation is less in differential RLC current mode signaling compared to other interconnect structures.
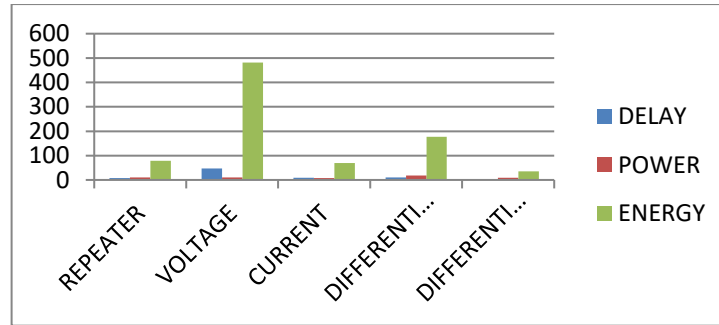
Fig.5.2 Performance of various Techniques by comparing the power, delay and Energy

III.   CONCLUSIONS

This work presents a study of different alternative circuits in interconnects to improve the performance by reducing delay. First, we simulated a optimal repeater insertion technique, delay and power values calculated by placing in RC and RLC interconnects. In this technique offers high switching delay, this can avoided in current mode techniques. Next we have simulated voltage and current mode signaling techniques by placing in both the RC and RLC interconnects. Calculated power, delay, energy parameters and compared with all circuit techniques. Out of all the circuits, the differential RLC current mode signaling offers very less amount of delay to 4ps. Thus the energy can be achieved also less in this technique. All simulations have done in 45nm technology using microwind.

REFERENCES

[1] International Technology Roadmap for Semiconductors [Online]. Available: http://public.itrs.net

[2] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance," in Proc. IEEE/ACM Design Automation Conf., 1998, pp. 560–565.

[3] C. Venkataiah, N. Ramanjaneyulu, Y. Mallikarjuna Rao, V. N. V. Satya Prakash, M. K. Linga Murthy, N. Sreenivasa Rao "Design and performance analysis of buffer inserted on-chip global nano interconnects in VDSM technologies" Nanotechnology for Environmental Engineering, May,2022. https://doi.org/10.1007/s41204-022-00249-x

[4] V. Sulochana , C. Venkataiah , Sunil Agrawal & Balwinder Singh " Novel Circuit Model of Multi-walled CNT Bundle Interconnects Using Multi-valued Ternary Logic", IETE Journal of Research,December,2020. https://doi.org/10.1080/03772063.2020.1864235

[5] C.Venkataiah, V.N.V. Satya Prakash, K. Mallikarjuna and T. Jayachandra Prasad, "Investigating the effect of chirality, oxide thickness,temperature and channel length variation on a threshold voltage of MOSFET, GNRFET, and CNTFET", Journal of mechanics of continua and mathematical sciences, pp 232-244, September, 2019. https://doi.org/10.26782/jmcms.spl.3/2019.09.00018.

[6] Vijay Rao Kumbhare, Punya Prasanna Paltani, C. Venkataiah, and Manoj Kumar Majumder "Analytical Study of Bundled MWCNT and Edged-MLGNR Interconnects: Impact on Propagation Delay and Area", IEEE Transactions on Nanotechnology, VOL. 18, PP-606-610, June, 2019. https://doi.org/10.1109/TNANO.2019.2920679.

[7] C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Insertion of optimal number of repeaters in pipelined nano interconnects for transient delay minimization", Circuit systems and signal processing, February, 2019. https://doi.org/10.1007/s00034-018-0876-7

[8] C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "FDTD algorithm to achieve absolute stability in performance analysis of SWCNT interconnects", Journal of computational electronics, June, 2018. https://doi.org/10.1007/s10825-017-1125-1

[9] C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Crosstalk induced performance analysis of single walled carbon nanotube interconnects using stable finite difference time domain model", Journal of nanoelectronics and optoelectronics, Vol. 12, pp. 1-10, June, 2018. https://doi.org/10.1166/jno.2017.2300

[10] C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Signal integrity analysis for coupled SWCNT interconnects using stable recursive algorithm", Microelectronics Journal, volume. 74, pp. 13-23, April, 2018. https://doi.org/10.1016/j.mejo.2018.01.012

[11] C.V.S. Reddy, C.Venkataiah, V.R.Kumar, S.Maheswaram, N. Jains, S.D. Gupta and S.K. Manhas "Design and simulation of CNT based nano-transistor for greenhouse gas detection", Journal of nanoelectronics and optoelectronics, Vol. 12, pp. 1-9, April, 2018.   https://doi.org/10.1166/jno.2017.2133

[12] C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Impact of Supply and Threshold Voltage Scaling on Performance of Cu and CNT Interconnects", International Journal of Pure and Applied Mathematics, Volume 118 No. 5, pp. 117-126, July, 2018.

[13] C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad "Effect of line parasitic variations on delay and energy of global on-chip VLSI Interconnects in DSM technology" International conference on Micro-electronics, Electromagnetics and Telecommunications (ICMEET), Lecture Notes in Electrical Engineering 434, pp. 221-228, July, 2018. https://doi.org/10.1007/978-981-10-4280-5_23.

[14] C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad "Effect of Interconnect parasitic variations on circuit performance parameters" IEEE International conference on communication and electronics systems(ICCES), Coimbatore, India, pp. 289-292, October, 2016, 978-1-5090-1066-0/16/$31.00 ©2016 IEEE

[15] Naru Venkata Mahidhar Reddy, C. Venkataiah "Performance Analysis of a Low-Power High Speed Hybrid Full Adder Circuit" International Journal of VLSI Designs and Communication systems (0757-0760), Volume 109 – No. 4, September 2016.

[16] C. Venkataiah, M. Tejaswi "A Comparative Study of Interconnect Circuit Techniques for Energy Efficient on-Chip Interconnects" International Journal of Computer Applications (0975 – 8887), Volume 109 – No. 4, January 2015.

[17] C. Venkataiah, V. N. V. Satya Prakash , V.Neeraja "Performance Analysis of Boostable Repeater in Different VLSI Interconnects and Applications" International Journal of Advanced Research in Computer and Communication Engineering Vol. 3, Issue 11, November 2014.

[18] C.Venkataiah, C.Vijaya Bharathi, M.Narasimhulu "Power Efficient Weighted Modulo 2n+1 Adder" International Journal of Computer & Organization Trends –Volume 3 Issue 11 – Dec 2013.

[19] K.Venkata Siva Reddy, C.Venkataiah "Design of Adder in Multiple Logic Styles for Low Power VLSI". International Journal of Computer Trends and Technolgy-volumes3 issue3, June, 2012.

[20] Salendra.Govindarajulu, C.Venkataiah, K.Mallikarjuna, G.Himabindu, C.Snehitha "Design of energy-efficient, high-performance CMOS flip-flops in 65 and 120 nm technology." International Journal of Advances in Science and Technology, Vol.2, No.3, March, 2011.

[21] H. Zhang,V. George, and J. Rabaey, "Low-swing on-chip signaling techniques: effectiveness and robustness," IEEE Trans. VLSI Syst., vol. 8, pp.264–272, June 2000. VLSI circuits," IEEE Trans. VLSI Systems pp. 195–206, Apr. 2000.

[22] Sampo tuuna, Ethiopia Nigussie,Jouni Isoaho and Hannu Tenhunen."Modeling of Energy Dissipation in RLC current Mode Signaling" IEEE Trans. VLSI Systems vol.20, no.6, june. 2012.