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Performance Analysis of Repeater Insertion Technique for Future VLSI Interconnects

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Abstract- In Nanometer regime, process variation and circuit aging cause remarkable and unnecessary and ambiguous circuit system characteristics and the resultant effects on the system design remains a great challenge to the designers. Even though the Guard band design can provide a little protection against these effects yet creates an increased design issues. Hence there is a strong need to equip circuits with the capability of tuning themselves and thereby compensating the variations with a proposed adaptive nature. This work is an effort towards supply voltage adaptation for variation resilience in VLSI interconnects. The main idea is a boostable repeater design that can transiently and autonomously raise its internal voltage rail to boost switching speed. The boosting can be turned on/off to compensate variations. The boostable repeater design achieves fine-grained voltage adaptation without stand-alone voltage regulators or an additional power grid. Since interconnect is a widely recognized cause of bottleneck in chip performance, and tremendous repeaters are employed on chip designs, boostable repeater has plenty of chances to improve system robustness.

Keywords: Interconnects, Process variations, switching time.

I. INTRODUCTION

As technology continues to shrink, process variations can have a significant negative impact on yield due to the wider spread of performance and power consumption. Post-silicon tuning allows the adjustment of device characteristics after a die has been manufactured to compensate for the specific deviations that occurred on that particular die. Power density has become a significant concern in microprocessor design due to the large numbers of transistors integrated in a single die and the increasing clock frequencies[1].

In Nanometer regime, process variations and circuit aging cause remarkable, and often unwanted, uncertainty in circuit system characteristics. Efficiently harnessing the variation effects remains a major challenge to be solved. Guard-bands, if large enough, can ensure that performance specifications are satisfied in the presence of the worst case variations. However, they often entail large design overhead and waste substantial resources, especially power, in typical cases. Statistical techniques are primarily to reduce the pessimism of guard-bands, but cannot reduce the variations [2-5].

A more fundamental strategy is to equip circuits with the capability of tuning themselves and thereby compensating the variations, i.e., adaptive circuit design. This paper is an effort on circuit voltage adaptation for power-efficient resilience to process and aging induced timing variations. In general, an adaptive circuit contains two major components: variation detection and variation compensation. By varying body voltage, transistor threshold voltage can be tuned for either faster switching speed or lower leakage power. The main advantage of ABB is that it can be applied at fine granularities with relatively small overhead. However, its tuning range is limited due to forward-biased junction leakage. Supply voltage adaptation, which is known as adaptive supply voltage (ASV), can compensate variations by changing supply voltage [5-10]. Voltage adaptation is more effective than ABB on power-performance tuning.

A straightforward implementation of fine-grained voltage adaptation usually incurs large overhead on either regulators or power grid (power delivery network). Consider a million-gate chip design, which is not uncommon in modern technology. If individual voltage tuning is applied at the granularity of hundred-gate blocks, one would need ten thousands of voltage regulators, which are evidently impractical [10-12]. Unlike OAB, which relies on dynamic device sizing, our boostable repeater exploits transiently higher voltage rail for speed improvement. Therefore, the extra load presented to timing path from a boostable repeater is significantly smaller. Another related paper is dual- VDD buffer. However, it requires two VDD lines. The boostable repeater design enables fine-grained circuit adaptation, and therefore, power-efficient resilience to variations. It presents limited load overhead to timing paths, and thus has small timing penalty in low power mode. The weakness is that it has significant device area overhead.

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II. LITERATURE SURVEY

A. Existing Methods

There are two main approaches for variation compensation: adaptive body bias (ABB) and supply voltage adaptation. Adaptive body bias (ABB) is a well known adaptive technique which tunes body voltage to control transistor threshold voltage. By varying body voltage, threshold voltage can be varied and It can be applied at fine-granularities also. If variation effect is strong, ABB can either lower transistor threshold voltage to restore performance or increase the threshold voltage to reduce leakage power. Supply voltage adaptation, a.k.a. adaptive supply voltage (ASV), can compensate variations by Changing supply voltage.

ASV has several advantages over ABB. First, ASV can be applied to almost any kind of circuits while ABB is difficult be applied on SOI (Silicon On-Insulator) circuits. Second, the tuning range of ABB is limited because of junction leakage current. The leakage power (PLEAK) and dynamic (switching) power (PD) can be expressed as,

$$P_{leak} = I_{leak} \cdot v_{dd}$$
$$P_D = \propto f C v_{dd}^2$$

where I_{LEAK} stands for the cumulative leakage current through circuit, α is activity factor, f is operating frequency, and C is for load capacitance. ASV reduces PD as well as P_{LEAK} by tuning VDD. Overall, ASV is a stronger and more sustainable leverage than ABB.

Recently, dual static supply voltage based adaptation techniques are reported they assume that two power supply (VDD) lines are available to a circuit block. The circuit block can be adaptively connected to either high or low VDD through sleep transistors. The difference between the two supply voltages is small so that there is no need to use level shifters as for voltage islands. These works did not show details on how to obtain the two different power supply lines at the same place, which is a difficult task. When the block sizes are small, i.e., in fine granularity, this approach implies nearly doubling of power grid wires. Power grid in modern chip designs is already huge, complex and has very limited room for additional overhead. Both fine-grained ASV and dual static supply voltage require more than one supply voltages. Conceivably, there are only two options to obtain a supply voltage: 1.Option 1: generate it from an off-chip voltage regulator and delivery it to on-chip destinations. 2. Option 2: generate it locally using on-chip voltage regulator [12-18]. Both involve voltage regulator which has two categories: switching regulator and linear regulator. Linear regulator is compact, relatively easy to be integrated on-chip and has 5fast responses. However, its energy-efficiency can be low compared to switching regulators, especially when voltage difference between input supply and regulated output is large. Switching regulator can be divided into two categories, switched-mode regulator and switched-capacitor converter. For dual static supply voltage, if one obtains the additional voltage through option 1, there would be a large power delivery network overhead due to duplicated supply lines.

For example, if a half of the entire circuit is powered by the dual static supply voltage, the size of power delivery network would increase by 50%. In current chip designs, the power supply network for even single voltage level is already very complex and heavily loaded. Hence, the room for additional power delivery lines is very small. If one chooses option 2, there are also problems. For linear regulators, small ones with limited output load current capacity is not sufficient to compensate large scale variations while large ones supporting high output load current cause too much power waste as well as stability issues which in turn increase complexity of regulator design [18-25].

For fine-grained ASV, there is no obvious good solution either. If one goes with option 1, the overhead on off-chip regulators would be huge. Consider a chip with a half million gates. If each block of 5k gates has its own ASV, then the chip needs 100 regulators each of which should supply all the 5k gates in each block. Option 2 is far from being practical as well since a large number of on-chip regulators each of which 6powers 5k gates cause either huge area overhead (from switching regulators) or large power waste (from linear regulators).

The main idea is a boostable repeater design that can transiently and autonomously raise its internal voltage rail to boost switching speed. The boostable repeater design achieves fine-grained voltage adaptation without stand-alone voltage regulators or an additional power grid. Adaptive design provides a power-efficient approach to variation tolerance.

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III. BOOSTABLE REPATER DESIGN

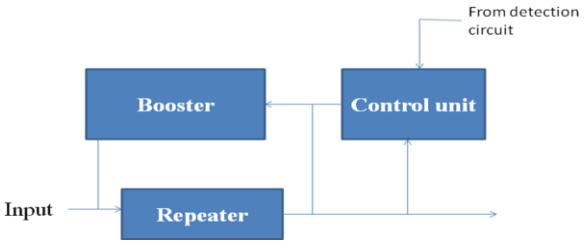

Fig. 1 Block diagram of Proposed work

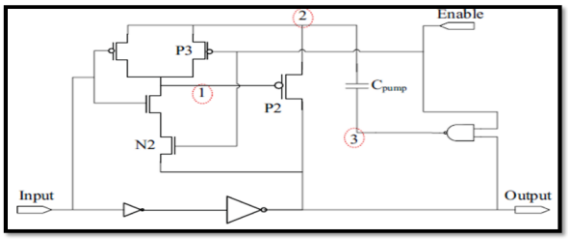

Fig. 2 Detail view of the block schematic

The proposed boostable repeater design is to use a transiently high voltage rail to assist the V_{DD} in high performance mode and simply turn off the high voltage in low power mode. In other words, the low power mode is the same as conventional static CMOS circuits. In the complete layout of the filter can be seen. The four capacitors were fixed at 2 pF, and layout as a doublepolycapacitor. The design procedure followed the method developed. The Simulation results shows that the center frequency has a range of operation from 4.5 MHz and 5 MHz while the quality factor is about 250 (a small variation occurs because the transconductor output resistance).

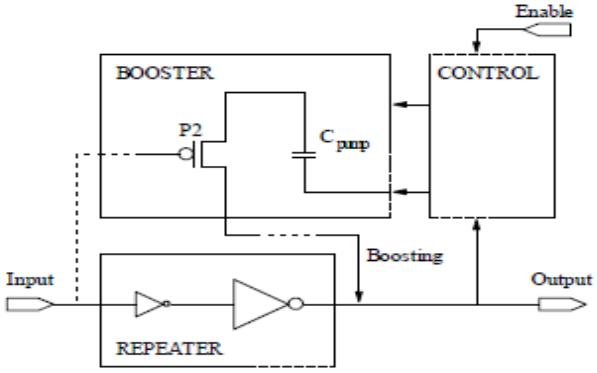

Fig. 3 Schematic view of boostable Repeater

This speed-up is achieved with the increase of voltage V2 (voltage at node 2) change (the solid line). The rightmost curve of and indicates that the V2 change and the speed-up gain naturally induce more power consumption. These curves provide guidelines to choose the sizes of P2 and Cpump.

Typically, we use 1.7µm width for P2 and 10fF for Cpump. For simulating the carried work Micro wind 4.0 is chosen which gives a design schematic with various layout editors. The basic requirements are Microwind 3– CAD tool, 32 nm layout editors, 32 nm layout analysis tool. The present document introduces the design and simulation of CMOS integrated circuits, in an attractive way thanks to user-friendly PC tools MICROWIND3. The lite version of these tools only includes a subset of available commands. The Lite version is freeware, available on the web site www.microwind.org.

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IV. SIMULATION RESULTS

The simulation results involve the design of conventional repeater and boostable repeater describing the waveforms for different length and width between voltage, time and current. These results show the working functionality of these repeaters for various layout editors.

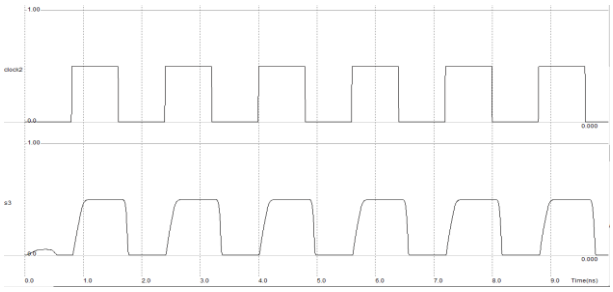

Fig. 4 Voltage vs Time waveforms of conventional repeater at length & width 70 & 140nm

The Fig 4 shows the voltage versus time waveforms of conventional repeater at length & width of 70 & 140nm. Clock2 signal is input and S3 is output of conventional repeater. The conventional repeater repeats the voltage at input end. Here we get the output S3 is approximately equal to the input signal.

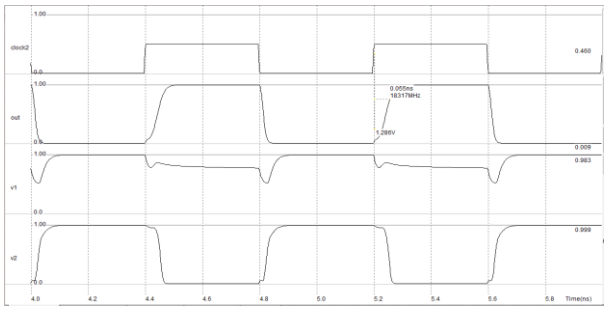

Fig. 5: Voltage vs Time waveforms of Boostable repeater at length & width 70 & 140nm

Here a chain of D-flip flops is taken as application circuit and conventional repeater and boostable repeater circuits are inserted and the results of those circuits are shown below.

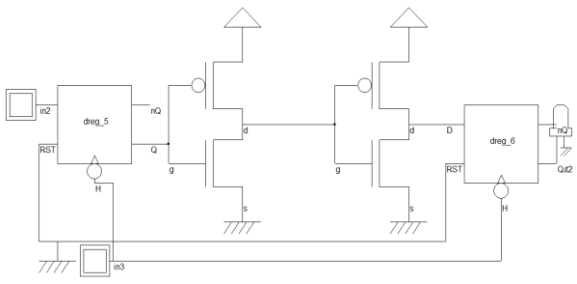

Fig. 6 Transistor level diagram of chain of D-flip flops with conventional repeaters

The Fig 6 shows the transistor level diagram of chain of D-flip flops with conventional repeater. Here two negative edge triggered D-flip flops are taken as chain and in between those two conventional repeaters are inserted. And when the clock signal (in3) is low then only the output is raised equal to the input voltage (in2). The output voltage at the second flip flop is approximately equal to the input voltage at the first flip flop.

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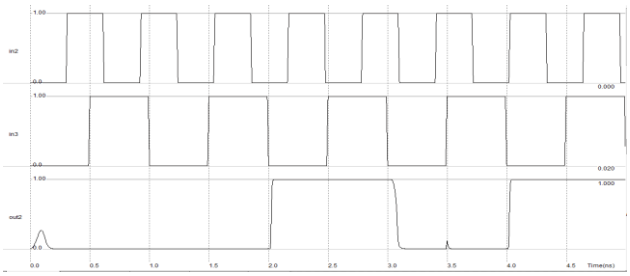

Fig. 7: Voltage vs Time waveforms of Chain of D-flip flops circuit with conventional repeater at length & width 70 & 140nm

The Fig 7 shows the voltage versus time waveforms of Chain of D-flip flops circuit with conventional repeater at length & width of 70 & 140nm. Here in2 is input signal and in3 is clock of D-flip flop, the output signal voltage is approximately equal to the input signal voltage.

The D-flip flop is negative edge triggered, so the output is triggered whenever the clock signal (in3) is negative and we get the output approximately equal to the input voltage. But when conventional repeater is used some glitches are present in the output voltage which is shown in Fig 5.6.

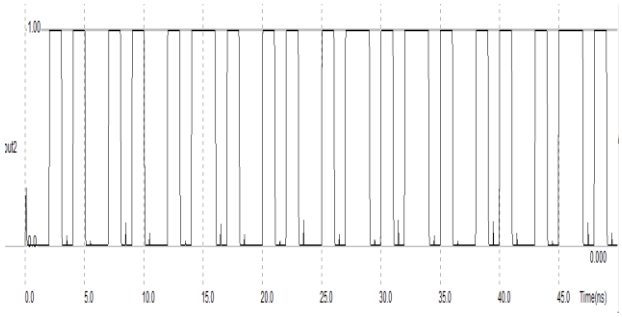

Fig. 8: Glitches in the output of Chain of D-flip flop circuit with conventional repeater

The Fig 8 shows the glitches present in output of chain of D-flip flop circuit with conventional repeater, which are overcome by using Boostable repeater in the place of conventional repeater.

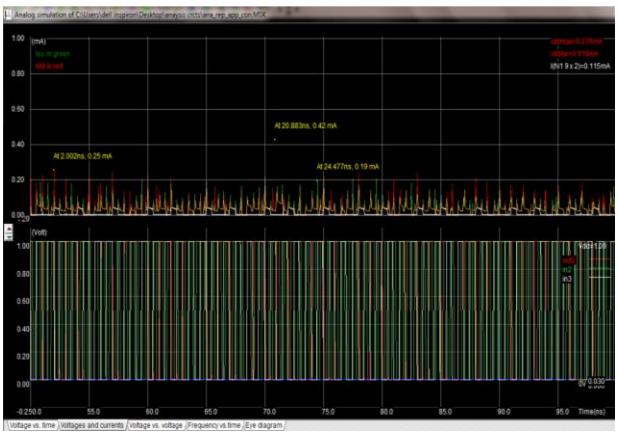

Fig. 9: Voltage vs Current waveforms of Chain of D-flip flops with conventional repeater at length & width 70 & 140nm

The Fig 9 shows the voltage versus current waveforms of chain of D-flip flops with conventional repeater at length and width of 70 & 140nm.

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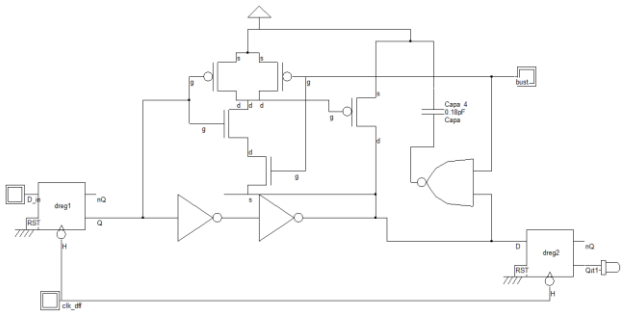

Fig. 10: Transistor level diagram of chain of D-flip flops with Conventional & Boostable repeaters

The Fig 10 shows the transistor level diagram of chain of D-flip flops with Boostable repeater. Here two negative edge triggered D-flip flops are taken as chain and in between those two conventional repeaters are inserted. And when the clock signal (clk_dff) is low then only the output is raised equal to the input voltage (D_in). The output voltage at the second flip flop is approximately equal to the input voltage at the first flip flop.

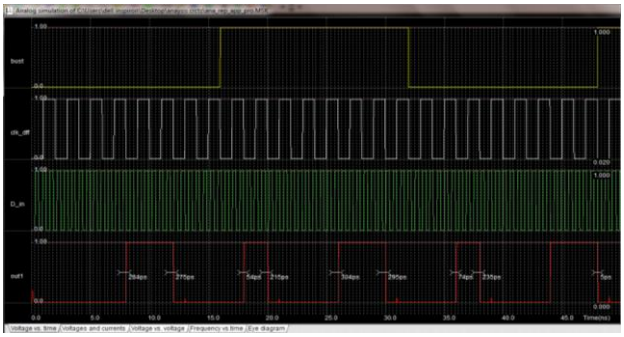

Fig. 11: Voltage vs Time waveforms of Chain of D-flip flops circuit with Boostable repeater at length & width 70 & 140nm

The Fig 11 shows the voltage versus time waveforms of Chain of D-flip flops circuit with Boostable repeater at length & width of 70 & 140nm. Here in2 is input signal and in3 is clock of D-flip flop, the output signal voltage is approximately equal to the input signal voltage.

The D-flip flop is negative edge triggered, so the output is triggered whenever the clock signal (in3) is negative and we get the output approximately equal to the input voltage. And Fig 6.14 shows the glitches in the chain of D-flip flop circuit with Boostable repeater.

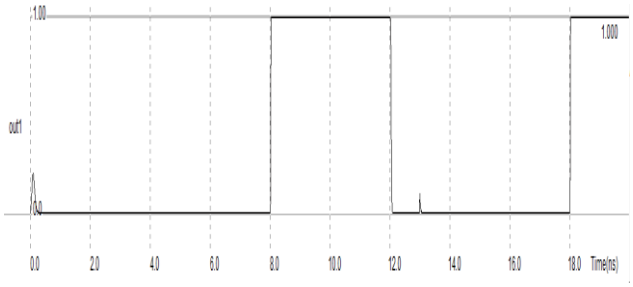

Fig. 12: Glitches in the output of Chain of D-flip flop circuit with Boostable repeater

Fig 16 shows the glitches in the output of chain of D-flip flop circuit with Boostable repeater. When compared to the conventional repeater glitches are reduced when boostable repeater is used in the palce of conventional repeater.

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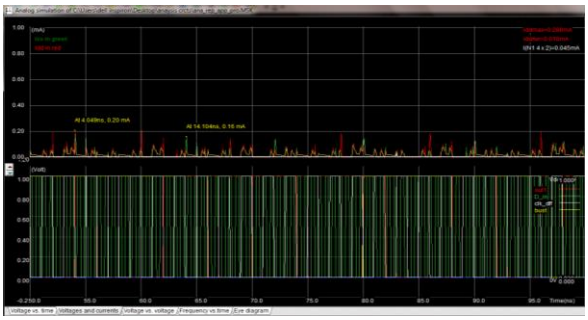

Fig 12: Voltage vs Current waveforms of Chain of D-flip flops with Boostable repeater at length & width 70 & 140nm

Table 1.1: Rise time comparison between conventional & boostable repeaters

	Rise time (ns)	
	Conventional Repeater	Conventional & Boostable Repeater
Individual repeater circuits	0.182	0.055
With chain of D- FF circuit	0.728	0.318
Chain of repeaters with D- FF circuit	1.046	0.929

From the above table, the rise time is less when boostable repeater is used along with the conventional repeaters. So, the switching speed is increased when boostable repeaters used.

VI. CONCLUSION

In this work, a new technique of boostable repeater design is proposed, which can transiently boost its switching speed. This technique can be applied to achieve variation and aging resilience in a power efficient manner. Our approach also significantly outperforms the previous paper on OAB. In future research, this will further investigate the application of boostable repeaters in dynamic power management. The further research over design automation approaches to implement the proposed system in standard design procedures, and minimizing charge leakage from charge pump to maintain boosting capability longer.

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