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Design of 30 GHz wide-band LNA for Next Generation Cellular Communication

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Abstract: In this paper, a low noise amplifier is designed at 30GHz for millimeter wave applications. The LNA is designed using BSIM4 transistor in complementary metal oxide semiconductor (CMOS) technology. The bandwidth ranges from 28GHz to 30GHz. the LNA design has two stages. A common source topology is designed at both stages which provide highly stable characteristics with high gain and low NF. In the first stage, noise and input matching is improved by using a degenerative inductor. The second stage is designed to achieve flat gain response over a wide bandwidth. The highest gain achieved by the LNA is 39.129dB at 30 GHz. The noise figure is less than 1.1dB over the entire bandwidth. 1 volt of supply voltage has been given. Advanced Design System (ADS) software is used for design of LNA and simulation of results.

Keywords: Advanced Design System, CMOS, Degenerative Inductor, Fifth Generation, Gain, LNA, 30GHz.

I. INTRODUCTION

The next generation of cellular system is designed by using 5G wireless technology. The 5G wireless technology works at different bandwidths [1]. The 5G standard are not yet finalized, but mm-wave bands are the best choices for the high demand of 5G bandwidth. For 5G at mm-wave, the frequency spectra selected a band from 28GHz to 32GHz because of its lesser atmospheric absorption properties [2]. A multi-antenna beamforming system is required by the 5G network to have good directional communication and overcome the path losses [3]. The frequency spectrum of 5G technology differs from one country to another. It also differs between the service providers of 5G technology. Based on availability of the spectrum each company/country favors a particular 5G frequency band [4]. The spectral efficiency can be increased at high frequency with frequency reuse and MIMO technologies because the interference is minimized by the narrow beam width of the high frequency signal.

For mmWave communication tremendous LNA designs are proposed. A 3-stage cascade amplifier co-designed with embedded high-pass filters is designed in [5]. A passive gm boosted CG-cascoded stage coupled with series peaking configuration is implemented in [6]. In all these configurations the purpose is to design the LNA which can achieve minimum noise figure and maximum forward Gain.

A LNA of two-stage is designed and implemented by using CS cascode topology. First stage has been designed to improve input matching network, minimize the noise. Here inductively degenerated source is used to maintain the forward and reverse return losses and LC input matching network. We are using BSIM4 CMOS transistor. The default gain of the first stage is insufficient to get desired results. So, to overcome this drawback the design has been cascaded. Flat gain is obtained at the second stage.

The organization of rest of the paper is as follows. Section-II discusses about the BSIM4 transistor and its parameter. Section-III shows the design details. The simulation results are presented in section-IV and section-V includes conclusion.

II. BSIM4 TRANSISTOR

For the simulation of any electronic circuit and integrated circuit an exact transistor model is required. BSIM4 belongs to a family of MOSFET. BSIM4 is accurate and scalable transistor whose width and length are decided by the LNA designer. This BSIM4 is also a predictive, robustic and physics based MOSFET SPICE-model. BSIM4 transistor is suitable for 0.13um CMOS technology and it also suitable for 90nm, 65nm, 45nm/40nm, 23nm/28nm and 22nm/20nm CMOS technologies.

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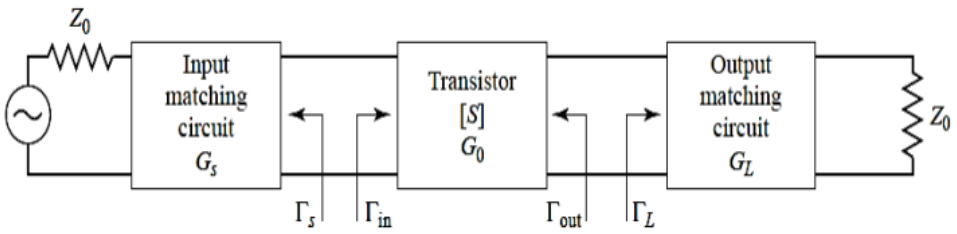

Fig. 1 Block diagram of LNA with source and load reflection coefficient

Using S-Parameters with the correct V_{DD} value, the performance parameters of low noise amplifier like input-output return loss, power-supply, output power, noise figure, stability, linearity, gain are characterized. Commonly in RF design field while biasing the transistor, the I_{DS} values are in mA or uA, but exceptionally in BSIM4 the Ids value has to be taken high.

When a transistor is biased, the main focus is to stabilize the transistor (K>1). After stabilizing, when the transistor's S-Parameters are obtained it has been observed that S_{21} (Forward Gain) of BSIM4 is having a negative value. The gain of the first stage is somewhat better than the stability circuit. By observing the behaviour and characteristics of BSIM4 transistor the second stage is designed by using CS topology which produced gain more than 20dB. From this it is concluded that increase in the number of stages increases gain of the LNA [7]. A general block diagram of LNA is shown in Fig. 1.

The goal of any low noise amplifier designer is always to achieve noise figure as low as possible because a minute change in NF of LNA (NF_{LNA}) can affect NF of the receiver. The NF of any recipient can be decreased by a small reduction in the noise figure of low noise amplifier. The total noise of the receiver NF_{rxr} can be given by Friis equation (1). Where the subsequent blocks after LNA are denoted as NF_{rem} and the LNA gain is denoted as G_{LNA}.

$$NF_{rxr} = \mathrm{NF}_{LNA} + \frac{\mathrm{NF}_{\mathrm{rem}} - 1}{\mathrm{G}_{\mathrm{LNA}}} \tag{1}$$

Another important parameter of LNA is Linearity which is measured by using P1dB. The LNA has to be operated in the linear region to satisfy the relation of output power Pout and input power Pin. The linearity of the receiver depends on the linearity of each block in the receiver chain.

$$P_{out}(dB) = P_{in}(dB) + G(dB) \tag{2}$$

The stability is the most important parameter of LNA which verify whether the designed circuit is stable or not. In order to avoid oscillations, the low noise amplifier should be unconditionally stable. K is the stability/Rollet factor which has to be greater than 1 and β1 is the alternate stability which has to be less than 1.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}|^2|S_{21}|^2} \tag{3}$$

$$\beta_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - \Delta \tag{4}$$

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| \tag{5}$$

The parameters like small chip area, low power consumption, noise figure, stability, gain and linearity decide the working of LNA.

III. DESIGN METHODOLOGY OF LNA

A. Biasing Circuit

One The transistor has been biased in order to achieve low noise figure. With V_{DS} of 1 volt and Ids of 9.874 Amp a bias voltage of 0.72V has been obtained at overall wide bandwidth.

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B. Design Methodology

The proposed design of LNA is as shown in Fig. 2. The LNA has two CS stages which are cascoded. The BSIM4 NMOS transistor is used with a supply voltage is 1V. 100fF of coupling capacitor (CC) is added in-between the 2 stages which connects both stages. 117.209fF of input capacitance, 125fF of output capacitance and 70fF of padding capacitance are the part of matching network.

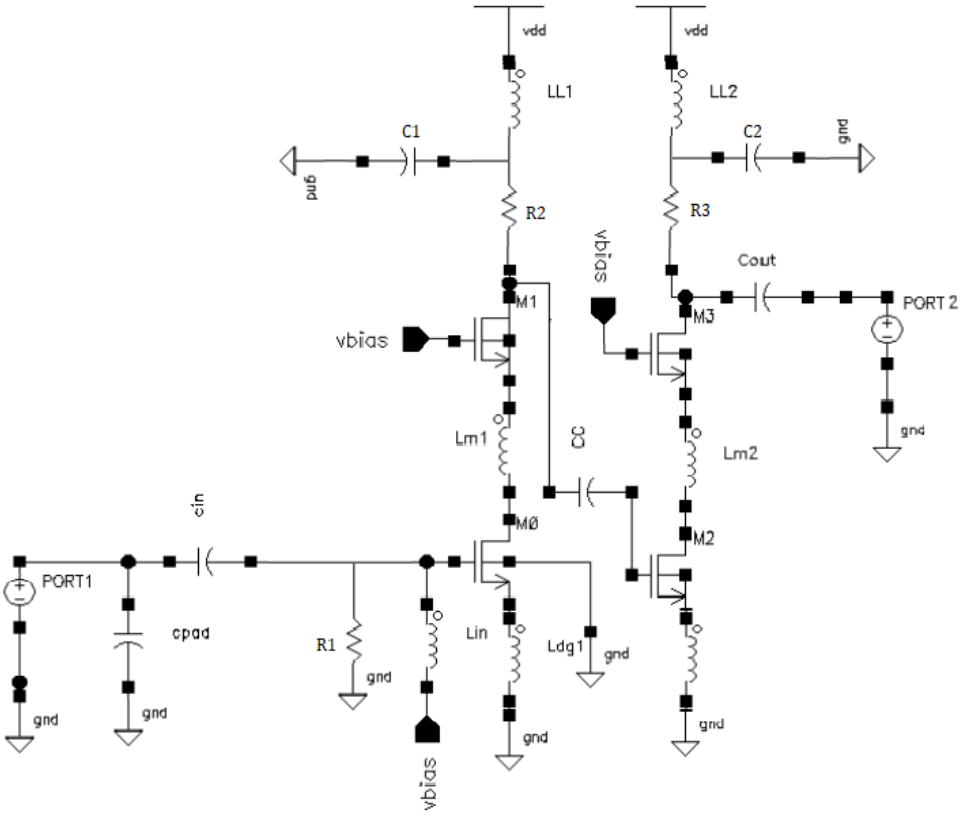

Fig. 2 Proposed two stage LNA topology

As a degenerating inductor Ldg1 (1nH) is connected at the source of Mo transistor and at the source of M2 transistor a degenerating inductor Ldg2 (34nH) is connected. Both the Drain-Gate inductors play an important role in stability and gain. By using Lin of 1.5nH, the biasing circuit is protected from the RF signals. To resonate at fundamental frequency, two drain inductors of 20nH (Ld1) and 34nH (Ld2) are used with Drain-Source Capacitance (Cds).

An inductor Lmd1 of 120pH is connected between M0 and M1 and Lmd2 of 65.711pH is connected between M2 and M3. A two-stage CS cascode topology LNA design provides the necessary gain without disturbing the linearity and noise figure.

C. S-Parameters

With a low supply-voltage when a low noise amplifier is designed at high frequency of 30GHz, the input-output matching becomes important. First input matching has to be designed. There are many ways to find input-output matching networks. For matching first Zin and Zout values has to be found. Then by using smith chart tool which is available in ADS, one can design the matching circuit. It is seen that Zin = 20.093 – j26.749 and Zout = 76.196 – j29.431. By minimum NF and maximum gain, the point of optimum reflection coefficient is selected at the source and load. For achieving minimum NF and maximum power transfer, the transmission line matching is preferred. β is the wave number which can be calculated by using equation (6) and the design of transmission line is according to equation (7).

$$\beta = \frac{2\pi f\sqrt{\varepsilon_{eff}}}{c} \tag{6}$$

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$$Z_L = Z_O \, X \, \frac{Z_L + j\, Z_O \, tan\beta l}{Z_0 + j\, Z_l \, tan\beta l} \tag{7}$$

D. LNA linearity and stability increasing techniques

The LNA has to be stable otherwise it can be called as oscillator (K<1). Without any change in the LNA parameters, the accurate frequency of operations is decided by stability parameter. For LNA stabilizing (That is, if the stability of the design is below 1 for some of the frequencies) we come up with two techniques. The popular one is do not let-down the forward gain S_{21}. By raising the cascaded transistor's transconductance in common source low noise figure topology and by decreasing reverse reflection the gain can be maintained as shown in Fig. 3.

When inductor is added at the source of a transistor, it acts as a noiseless R (resistor) and decreases the forward gain. The second method of stabilizing is to decrease the gain by adding inductor at the source of the transistor at the second stage. Linearity also by increased by this method.

IV. LNA PARAMETERS RESULTS AND DISCUSSION

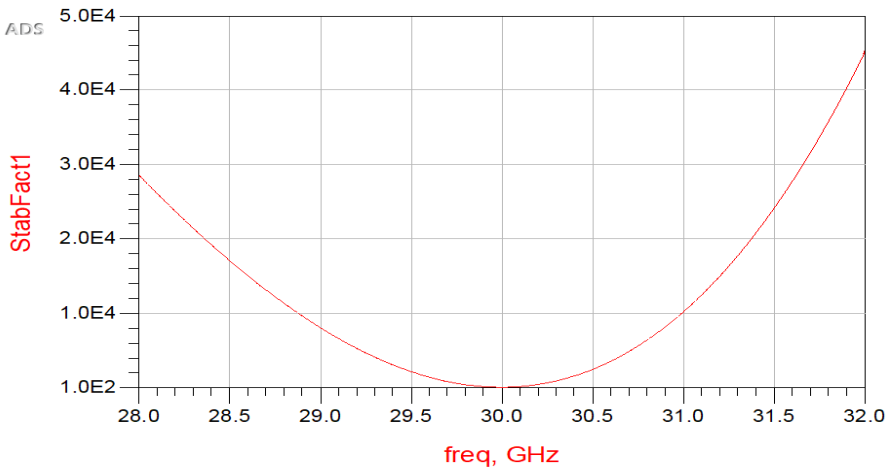

Fig. 3 Stability factor of the LNA

From Fig. 3, it can be concluded that the designed LNA is unconditionally stable. Here K>1 for overall frequency band. Fig. 4 shows that all Load circles and Source circles are outside the Unit circle due to which for any load variations the proposed LNA is stable.

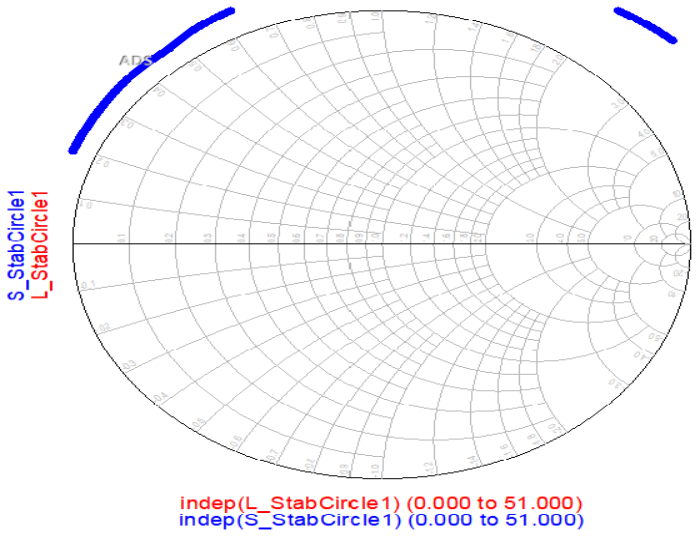

Fig. 4 Source and load circles

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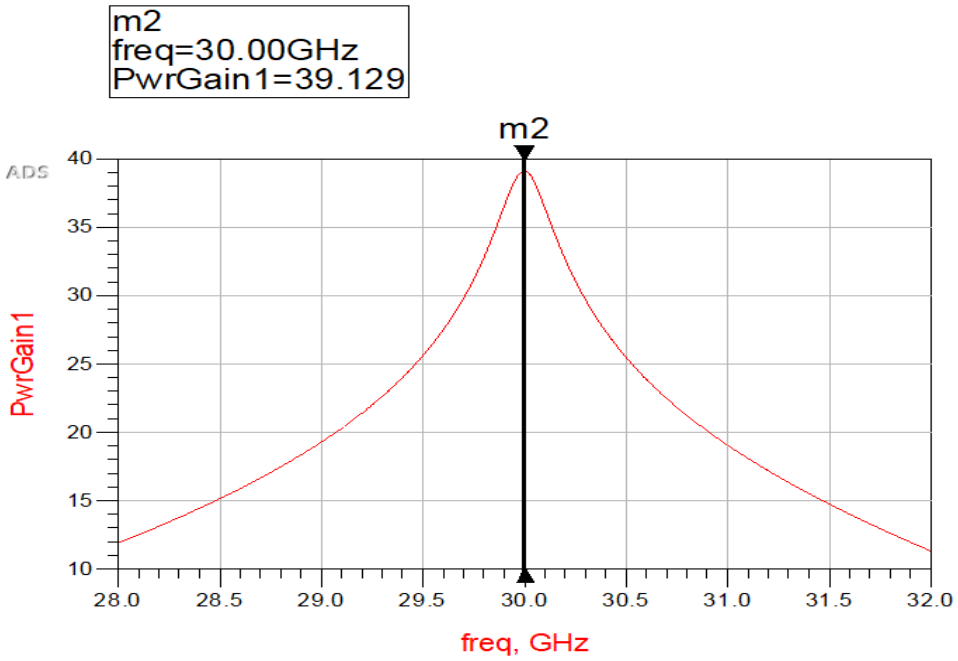

Fig. 5 Gain of low noise amplifier (in dB)

The simulation result of gain is as shown in Fig. 5. By increasing the size of the transistor, one can achieve a forward gain above 22dB. The LNA obtained a peak gain of 39.129dB. NF of 0.622dB is observed at 30 GHz as shown in Fig. 6. The disadvantage of increasing the size of the transistor is, with increase in size it also increases the noise percentage of the circuit. Through lumped-matching, low noise figure can be achieved. As shown in Fig. 6 the noise figure is less 1.1 dB for overall bandwidth.

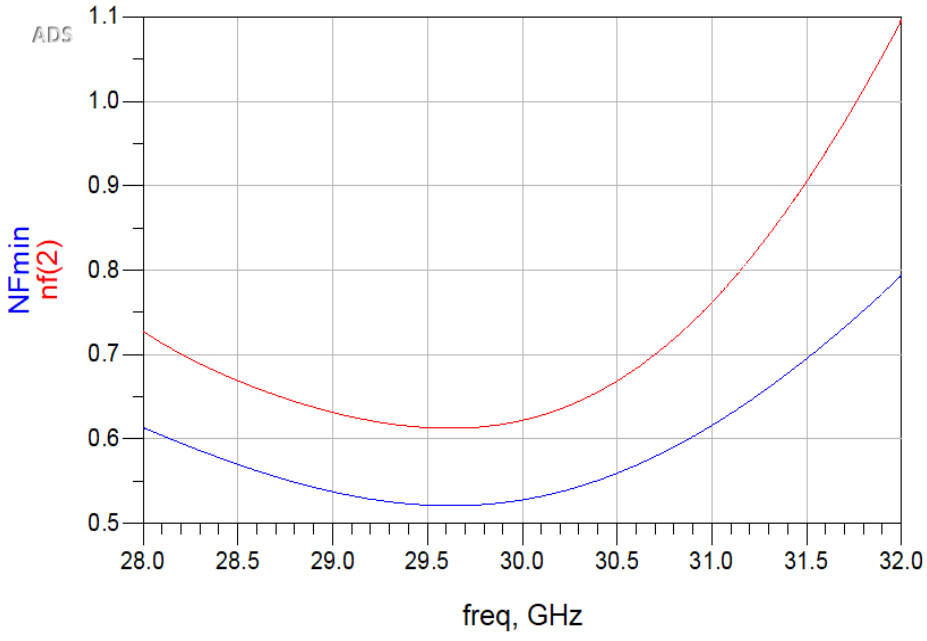

Fig. 6 NF of LNA

To analyse the result of the designed LNA, it has to be compared with already available LNA designs. The TABLE I shows some of the referred design parameters for 5G technologies which are then compared with the proposed LNA design.

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TABLE I COMPARISON WITH THE STATE OF THE ART

Ref.	V_{DD} (V)	Topology	Frequency (GHz)	Noise Figure (dB)	Max Gain (dB)
[2]	1.2	2-Stage Cascode	33	4	24.5
[4]	1	3-Stage Cascode	28	4	24
[6]	1.1	gm boosted cascoded CG-CS	28	3.3	35
[7]	1.8	2-Stage Cascode with active balun	30	0.95	44.57
This Work	1	2-Stage Cascode	28-32	0.613-1.097	10-39.129
This Work	1	2-Stage Cascode	30	0.622	39.129

V. CONCLUSION

This research paper proposes the use of a compact CMOS based LNA for emerging fifth generation (5G) technologies. The techniques of stabilizing a circuit which are explained in section-III_D allow LNA to perform optimum operations. The high gain and wide bandwidth offered by the designed LNA is convenient for the DCR. The proposed low noise amplifier can also support the multiband 5G process and the requirements for a parallel bank of different multiplexed LNAs are avoided. The NF, forward gain S_{21} are 0.622dB and 39.129dB respectively which are obtained at 30GHz.

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