IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

# Thermal Stability Analysis of Radiation Hardened 14T and 15T Differential Ended RAM Cells for Outer Space by 22nm Technology

**Dharma Teja Lanka[1], S. Rajendra Prasad[2], K. Srinivasa Rao[3]**

Department of Electronics and Communication Engineering, Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering and Technology, Hyderabad, Telangana, India[1]

Department of Electronics and Communication Engineering, Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering and Technology, Hyderabad, Telangana, India[2]

Department of Electronics and Communication Engineering, Malla Reddy Institute of Technology, Maisammaguda, Dhullapally, Secunderabad, Telangana, India[3]

**Abstract:**Static Random Access Memory is a volatile type of memory used for enhancing the data rate of operations in devices for outer space applications. The semiconductor devices might be damaged or would experience a malfunction resulting in software errors due to avionics and radiation conditions. The ionising particles in space may lead to the state of change in the memory cell and distract the multiple bit operations in the written mode. This phenomenon is known as a single event upset (SEU). Scientific Advancements in various technologies and architecture design of SRAM are being introduced. Consequently, SEU type of errors could not be prevented but could be minimized to a significant extent. Here a 14 T based 3 terminal and 4 terminal CMOS SRAM cell is designed and is compared with a 15T 3 terminal and 4 terminal SRAM cell. Circuits are implemented using Tanner 16.5 version. Using MATLAB, performance metrics like SNM, read delay and write delay are observed. The proposed 15T SRAM cell improves the performance in terms of deviation in HSNM by 79%, 2% from 13T and proposed 14T SRAM cells during the rise in temperature. The CMOS SRAM cell is designed to minimize leakage by reducing the operating voltage. The proposed cells are also implemented using FinFET, CNTFET, and GNRFET technologies in the development stage. In the proposed 15T SRAM cell, power is reduced by 12.8%, and the delay factor reduced by 13.2% compared to 13T SRAM cell.

**Keywords:** sram, rhbd, hsnm, seu, finfet, cntfet, gnrfet.

## I. INTRODUCTION

Radiation hardening is used in electronic circuits to reduce the damage or malfunction of the circuit around nuclear reactors and in space due to the high ionising effect. In some cases, ionizing radiation caused the malfunction of the circuit, especially in terms of memory devices. tThis radiation ionising effect is eventually known as a single event upset (SEU) [1, 2]. On the other hand, this radiation might not damage the memory. Still, it can cause a malfunction in the operation of the device, which is known as multi-effect, and the combination part was named as Single Event Multi Upset effect (SEMU) [22].

This radiation effect can be handled by resetting [7] the power cycle under state machine-based previous state identification using a software-based controlled strategy.
This will not change with low investment as it will be in outer space applications [4]. The memory devices designed with the help of CMOS [16] ionising effect also caused the soft error [17] by flipping the bit in the device. This effect is caused due to the accumulation of holes in the oxide layer. This method delays accessing memory devices, which is a serious problem. A varied write cycle can elaborately reveal test results of SRAM memory devices during the ionizing dose test.

The size of the integrated circuit machines decreases with each successive technology generation. This strategy aims to both boost the efficiency of integrated circuits while also integrating a significant number of devices into each unit area. The size of the transistors that form the memory cells is approximately equal to Moore's law. As a result, the cell density of each cell decreases from one generation to the next [1]. The current technological processes used to produce

DOI: 10.17148/IJIREEICE.2022.10648

SRAM compatible metal-oxide-semiconductor (CMOS) memory are in nanometre. The element size of the transistors element makes each cell a nanometre system.

SRAM supply voltage is also reduced. However, this decline did not follow the speculation of the International Technology Roadmap for Semiconductors (ITRS). It was moderate and was mainly due to the limit placed on the transistor's threshold voltage scaling to avoid an excessive increase in current leakage [2]. To meet the operational requirements of modern electronic devices, integrated SRAMs are generally required. Due to this necessity, a significant amount of the space is allocated. Predictions suggest that the number could rise to 90% [3] and this leads to higher costs.

Design professionals are attempting to incorporate a large number of SRAM cells into each unit. This process leads to the formation of cells of smaller size in order to extract the full potential of the technology. SRAMs are typically designed with transistors as close to size as possible and arranged as high as possible. In addition, to reduce power consumption, the voltage is kept as low as possible. Although, as mentioned earlier, the expected power reduction was not fully utilized in real technology.

Due to the reduced size of the device and the reduction of the power generated in the production of successive technologies, the SRAM design faces two major issues: one is cell stability and the other is related to its exposure to radiation of temporary events. The latter problem is focused in this paper. However, SRAM stability issues are also being discussed.

SRAMs are one of the most critical components of regional radiation. They are very sensitive to those effects caused by a single particle of energy which are called single event upsets (SEUs). They are called as soft errors (SE) because the circuit is not damaged permanently even though a fault is occurred.

Due to SEUs generated in the circuit, the interaction of powerful particles creates pairs of electron holes so that part of this charge is collected through a sensitive area that affects its power supply. If the above node is an SRAM node and the interference level is high enough, it may examine the cell's status and alter the data it stores, resulting in an error. These errors are wrong. A particle can transform data contained in one or more memory cells without causing damage in SRAM. According to this description, cells have the ability to be reprogrammed and perform normally.

The problem of radiation effects in integrated circuits is not new. This assumption is due to the high flow of active particles of these materials operating at these high exposure points. In addition, the atmosphere protects part of the dynamic particles from outside the earth so that at higher altitudes the rising particles rise. To reduce effects, outdated components should not be used, error detection and repair techniques as well radiation tolerant materials need to be employed. The implementation of these measures ranges from construction and technical to system level. There are many well-known strategies for reducing SEU effects, such as triple modular redundancy (TMR), which may be appropriate for certain applications. However, many of them include higher fines in terms of cost, power and performance, which may be gained in the space industry, but which are not acceptable in other FPGA application fields.

In addition, due to technical limitations, SEUs become a major concern for the reliability of conventional power plants and SRAMs in particular, not only in high-density areas but also at low bandwidth, where radiation frequency is low. In the case of SRAMs, the number of errors during each unit in SRAM memory due to temporary radiation events has increased by technical measurements [3, 5]. This fact has two main causes. The first reason is the reduction in the size of the transistors that make up the cells and the decrease in electrical energy. Both factors reduce the amount of electrical charging used by a cell to store a single piece of information. Therefore, it is easy for the charge resulting from particle interactions to disrupt cell content. The second reason is cell proliferation, i.e, high cell density.

The implemented SRAM [9] architectures have undergone a Total ionising dose (TID) [14] test, low dose rate effect (ELDR) and Single Event effect test to prove the stability against radiation in space application.

The major contributions of the paper are

- Designing 14T and 15T SRAM models and testing them with three terminals and four-terminal models.
- Testing RSNM and WSNM using various FET technologies on 22nm.
- Calculating performance metrics and identifying the best model of all designed models.

In [3], a low voltage 13T SRAM is designed to minimize the hardness of circuitry with less operating voltage. Even with this, it's hard to use in space applications. In [12], robust dual access 12T SRAM cell is designed for better

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

PDP at low operating voltage. Here, the hardness isn't reduced even at different operating voltages. A critical charge of 15T SRAM is proposed in [6] with zero percent failure with effective delay, but it could not hold better power dissipation. An efficient 14T SRAM is designed in [8], but the operating voltage and technology were outdated.

In [11], an interleaving stacked 14T SRAM is designed and tested on different operating voltages for better analysis. However, an external circuit for injecting the current results in excessive area utilization is required.

A cross-coupled inverter-based 12T SRAM is designed in [12] for better PDP in both read and write modes at different operating voltages. However, the hardness was not minimized. A dual interlocked storage cell 12T SRAM is designed in [18] with minimal failure probability, but less effective in efficiency. In [21], polarity-based 14T SRAM is designed with effective minimization of area and power with a trade-off of delay. A quad node interlocked feedback mechanism is proposed in [23] with 12T SRAM to provide soft error prediction.

The paper's organization is as follows, in section II, a survey on different approaches and radiation hardness-based soft error minimization is discussed; section III deals with the design and mathematical representation of the system; section IV helps in understanding the results obtained during the simulation. Section V represents the paper's conclusion and works implemented considering the future directions of the work.

## II. METHODOLOGY

### II.1 Working of 14T

The proposed SRAM bit-cell comprises six PMOS transistors (M3-M8) and eight NMOS transistors (M1, M2, M9-M14) as displayed in

Fig. 1. The RHBD 14T SRAM bit cell is fabricated utilising four stacked inverters Inv1, Inv2, Inv3, and Inv4.

The Inv1 (Inv2) inverters worked to keep the NMOS transistors M9 (M10) between M3 (M6) and M11 (M14) transistors. Additionally, the Inv3 (Inv4) inverter is worked by keeping the PMOS transistors M7 (M8) transistor between the M4 (M5) and M12 (M13) transistor of the normal inverter. Communications between NMOS (PMOS) transistors for Inv1 and Inv2 (Inv3 and Inv4) marked Q and QN (S0 and S1) separately. The Q and QN (S0 and S1) are $0 \rightarrow 1$, eliminating noises as an NMOS (PMOS) transistors encircle them. Low Vth transistors develop the voltage yield at intersections Q, QN, S0, and S1.

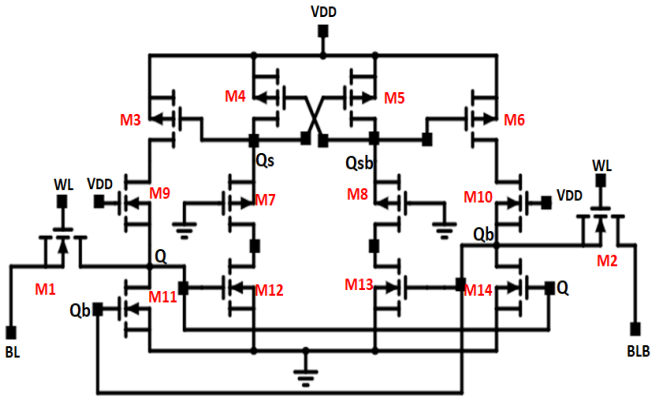



**Fig. 1 Proposed 14T SRAM cell**

The M13 and M14 devices utilise the word line (WL)to add volume centre points (Q and QN) to the line pieces (BL and BLN) separately. In the RHBD 14T SRAM cell, the M7, M8, M13, and M14 transistors are constantly in an ON state, without working mode. Subsequently, as the WL is set to a certain level (VDD), section level transistors (M13 and M14) test/compose SRAM bit-cells. Volume crosses Q, QN, S0, and S1 are devoted to ensuring data in the RHBD 14T SRAM bit-cell. The overhaul of this capacity utilises the new Predictive Technology Model (PTM) libraries of 22nm at 0.9V VDD and room temperature. As WL is low (ground/gnd), that is in the RHBD14T SRAM hold, sitting

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

tight for Q = S1 = 1, and QN = S0 = 0, transistors M3, M2, M5, and M12 are open, while other devices are closed (aside from all modes in semiconductor M7, M8, M11, and M12).

Then, the RHBD 14T SRAM bit-cell stands firm on its foothold dependably. RHBD 14T bit-cell strategy begins after pre-charging BL and BLN to VDD, WL coordinates VDD to open access devices (M13 and M14). The degree of focus in Q and BL holds in VDD, albeit the power level in BLN drops to 0 with the M14 access contraption and the M12 pull-down device, as displayed in

Fig. 1.

BL and BLB are kept 'in' 0 'and' 1 'for configuration work individually. The sub-areas of Q and QN are individually chosen as 1 and 0. As the WL is brought to the basic level (VDD) simultaneously, the power levels in the BL and BLN charge the QN to '1 'and prompt the convergence Q to '0' independently. The practical plan and utilisation of the proposed bit-cell diagrams of RHBD 14T SRAM are displayed in

Fig. 1.

- The centre Q abandons 1 to 0 because of a strike of particles. The M4 closes momentarily. The voltage at inverter 1 is in the show mode (reason 0). Hence, M1 is open always. Hence, Q will be changed to its lower state (reason 1).
- The changing data in centre Q ('0' to '1 ') opens the semiconductor M4, and the data in centre point QB will be reconfigured.

### II.2 Working of 15T

In the proposed SRAM configuration, MOSFET is supplanted by FinFET, CNTFET and GNRFET based semiconductors. The SRAM cell contains 15 semiconductors of which M3, M4, M5, M6, M7, M8, M9, M10, M11, M14 and M15 constructs a drag organisation, and the M1, M2, M12, and M13 assembles a drag organisation.

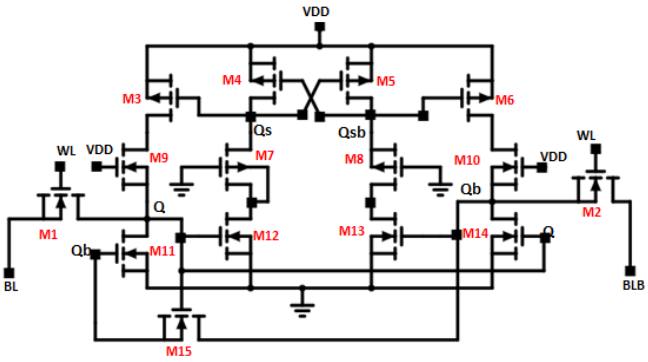



**Fig. 2. Proposed 15T SRAM cell**

The bit cell configuration fuses a mix of semiconductors in piece cell geography contrasted with 6T SRAM, exchanging with superior execution and low power utilization. This approach is utilized as a reaction strategy to reduce the expanded power utilization. The 15T SRAM bit cell is designed by stacking at least two semiconductors in every inverterwhere the inverters are associated equally. For proficiency work, Bit Line (BL) and Word Line (WL) are obligatory; the cell utilises five signals to be specific BL, BLN, WWL (Write Word Line), RWL (Read Word Line ) and RBL (Read Bit Line.). The SRAM working in 3 distinct ways is depicted below.

To play out the M13 read admittance, the semiconductor joins a solitary edge adding something extra to a 15T SRAM cell plan. The RWL signal (Read Word Line) controls each cell, and the read cycle begins with a pre-section accuse of a short-doled outline BL and BLN at rationale one voltage which typically builds the learning execution speed. After the piece line has been pre-charged, the name line is inoculated, which permits the semiconductor to access and cause a

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

voltage drop across one of the more modest lines. The Q position is driven in a steady position in rationale 0 or 1 because of the two-fold worked process. Eventually, Bit Line (BL) is set to 0.9V and 60ns of the beat time frame and 30ns of the beat range as per the Bit Line Negation (BLN) declares that - 0.9V (for example BL backward) with 40ns span and 20ns beat width.

Hence, the Read Bit Line (RBL) is set to 0.9V a 100 and 50ns for beat span and reach. Assuming bitline is pre-charged, two-word signal WWL and RWL are inoculated at 0.9V with PP = 60ns and PW = 30ns of WWL and PP = 80ns and PW = 40ns of RWL. Here RWL is empowered in rationale 1 with the goal that the BL esteems are shown in the SRAM yield Q (for example, the qualities in the bitline are perused, and the SRAM yield is taken in Q). If the BL yield is rationale one and the RWL is set to rationale 1, SRAM peruses the result as rationale 1. Even though assuming the BL yield is rationale 0, the RWL signal is inoculated in rationale 1, then SRAM peruses yield as rationale 0.

SRAM accomplishes both proficiency work, and the composting cycle stated 15T SRAM is finished by calling frail reaction hubs. Slender lines are associated with record access semiconductors and keep on being constrained by the line of text. The ideal worth entered in a bitline can be rationale 0 or 1. For instance, on the off chance that rationale will be composed, then BL = 0 and BLN = 1 and for the situation assuming rationale one is composed, BL = 1 and BLN = 0 qualities are immunised. Whenever you have set the piece line esteems, the line of words is empowered to enact and make the worth put away in the association cycle.

At an inventory voltage of around 0.9V piece rate, BL and BLN are given - 0.9V and 0V with PP = 60ns and PW = 30ns. Then, at that point, the bitlines are inoculated to do the necessary composing work. WWL demands that - 0.9V with PP = 60ns and PW = 30ns separately RWL is set to 0.9V and PP = 80ns and PW = 40ns individually. Here in the above signal highlights, when the compose signal is immunised, the SRAM Q yield delivers the contrary worth of the real yield. To compose rationale 0, a bitline is immunised in rationale 1, and a line of words is set while composing rationale one and a thin line is set to rationale 0, and a line of words is inoculated.

Thermal Stability Analysis of proposed SRAM cells

SRAM memory cell operates in three modes: Hold mode, write mode and read mode..During write mode, memory cell disturbance is not considered because we need to write data into the memory cell which have to be replace the present data. During read mode, cell gets disturbed by pre-charged bit lines, which is considered as read disturbance. This read disturbance is handled by conventional memory cell and Schmitt trigger-based cells, which were already proposed. So during hold mode disturbance due to radiation will affect the data in the memory cell.At room temperature, only read failures occurs. Usually for rise in temperature, SEUs may occur and results in hold failure. The proposed 15T SRAM cell is designed in such a way that it can withstand SEUs. For rise in the temperature during the hold operation, voltage at node-Q rises by ∇V which is pulled to level-‘0’ through activating pull down path (M11) as shown in Fig. 2.

The rising voltage (∇V) turns M12 ON, so stacked memory node pulled to low level, which turns M5 transistor and turns off the M6 transistor. So node-Qb is raised to level-’1’. The feedback mechanism in the proposed SRAM cell turns On the M11, which brings the node-Q to level-‘0’. So stability of proposed 14T SRAM cell is improved when compared with 13T SRAM cell as shown in

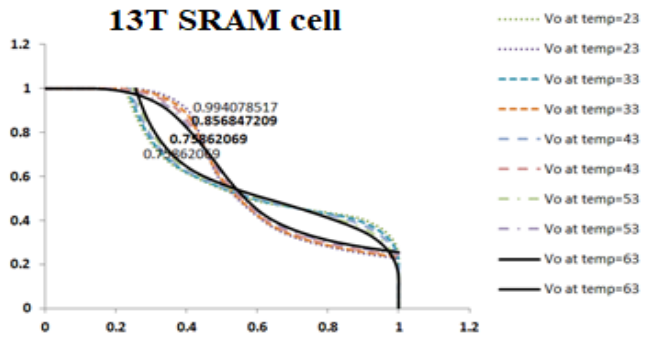



Fig. 3

Fig. 3 and Fig. 4. The figures show the improvement of HSNM, which is calculated using butterfly curve method (DC transfer characteristics of inverter circuits formed by M3-M11, M6-M14).

The calculated HSNM for 13T SRAM is 198mV at room temperature, which is degraded to 96mV when temperature is raised to $63^{O}$C. The observation from the calculation of HSNM shows that 13T SRAM cell has less stability with

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

temperature changes (∇HSNM=102mV). The proposed 14T SRAM cell has more stability as temperature increases (∇HSNM=27mV).

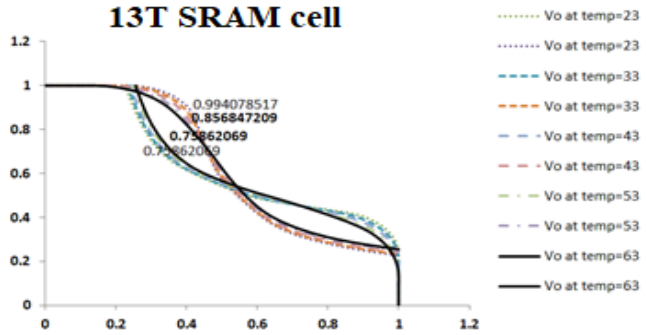



**Fig. 3. Butterfly curve analysis of 13T SRAM cell**

HSNM= 0.994-0.792=198mV at temp=23$^{O}$C
HSNM= 0.856-0.758=96mV at temp=63$^{O}$C
∇HSNM=102mV

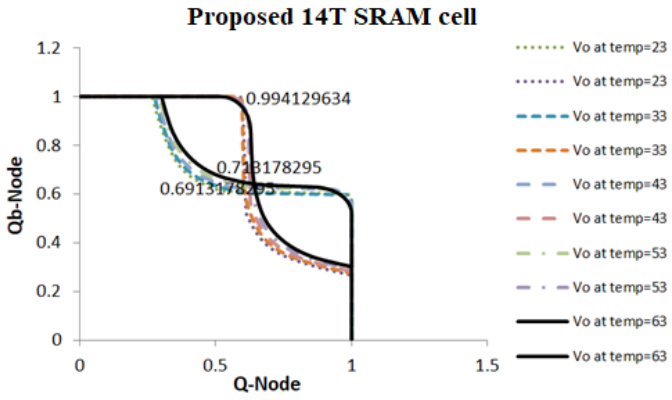



**Fig. 4. Butterfly curve analysis of proposed 14T SRAM cell**

HSNM= 0.994-0.691=303mV at temp=23$^{O}$C
HSNM= 0.994-0.718=276mV at temp=63$^{O}$C
∇HSNM=27mV

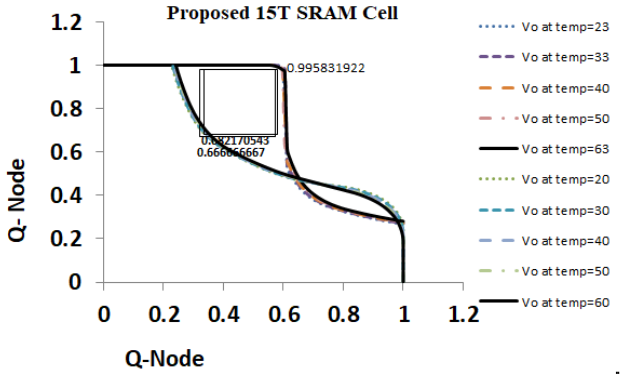



**Fig. 5. Butterfly curve analysis of proposed 15T SRAM cell**

HSNM= 0.995-0.661=334mV at temp=23$^{O}$C

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

HSNM= 0.994-0.6828=313mV at temp=63$^{O}$C

∇HSNM=21mV

The proposed 15T SRAM cell is designed in such a way that voltage raise in the node-Q, can activate the feedback configuration through extra transistor (M15) to minimize the disturbance. The disturbance at node-Qb will not affect the transistor M11, when transistor M15 is off. So stability of proposed 15T SRAM is improved when compared to 13T SRAM cell and proposed 14T SRAM cell.

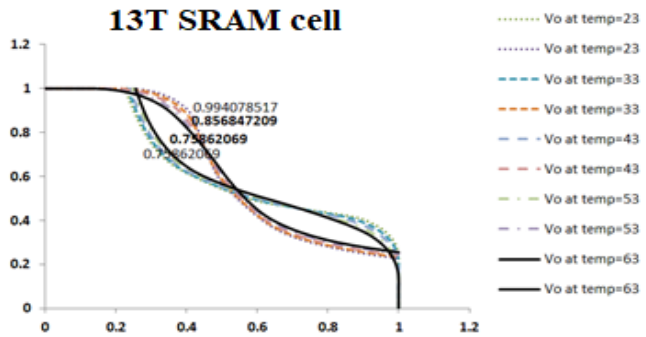
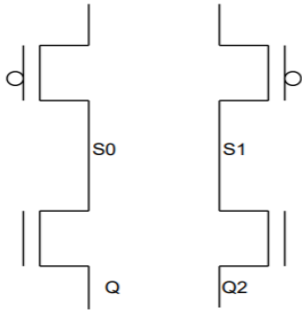



Fig. 3 Fig. 4 and Fig. 5, we can observe that HSNM is not deviated much in proposed 15T SRAM cell (∇HSNM=21mV). So proposed 15T SRAM cell is much better in terms of stability when compared to 13T SRAM cell and proposed 14T SRAM cell. The proposed SRAM cells can withstand SEU's because of less deviation in stability (∇HSNM) due to rise in the temperature.

Physical Layout Design PLD consists of three stages majorly partitioning, floor planning and placement1 Partitioning

Here in this stage of proposed model tries to detect the RHE in SRAM unit using Q, $Q_0$, S and $S_0$. Allocation of Q, $S_0$ & $Q_n$, $S_1$ results in minimizing the RHE problem.




$$C(Q, S_0) - (1)$$
$$C(Q_n, S_1) - (2)$$

As it already known that RHE problem might be a software error or malfunction of the devices used in building the SRAM unit as this is a result of shifting the bit at output stage of data transferring mode. In our approach Q, $Q_0$, S and $S_0$are the outputs of the system where proposed model initiates identifying the RHE problem at this stage of the implementation. Therefore, this made the SRAM unit to know at which device i.e., P1, P3, N2 and N4 out where the error was generated that helps in optimizing the RHE problem and the relation was given in equation (1) and equation (2) and from these 2 equations a clear vision of comparing the stage outcomes as Q = $Q_0$ and S = $S_0$. If above mention both conditions were out of phase to each other, and the system was not affected with RHE or any of the condition else both the conditions were true it ,results in error representation. In floor planning stage these conditions are compared with previous stage to obtain the results at which stage the malfunction occured. As earlier stated in this section the optimization was performed with respect to early-stage detection.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

## 2 Floorplanning

The stage-based relation between Q and $Q_0$ results in the triggering generated error, S and $S_0$ relation helps in tracing the error in active state of the devices. These operations were considered to be the conditions of the error tracing to pull the error and shift the operation bit in the next stages of the proposed model. This section helps in suggesting the direction of error whether it is horizontal or vertical and this was named floor planning as the direction of the error will be traced here.

## 3 Placement

Standard SRAM cell allotment with $P_3$ & $P_1$ along $N_2$ & $N_4$ units to activate C (Q, S) along ($Q_0$, $S_0$) in Q reciprocal manner. The C (Q, S) is activated in Q by shifting the bit operation from the previous state based on C (Q, S). It will be reversed. Therefore, power was compared with extreme energy change and checking with respect to temperature.

$$p = \frac{p_r}{p_q} * \frac{\exp(-E_Q - E_{Q_n})}{K_t} > 1 \qquad (3)$$

Where$E_Q$ be the energy at Q &$E_{Q_0}$ be the energy at $Q_0$
If Qis an inactive state

$$E_Q - E_{Q_0} < 0$$

else

$$E_Q - E_{Q_0} \geq 0$$

$K_t$ is Boltzmann constant(4)

Portioning worth ked on temperature

$$L_H(T) = L_H(T_i)\left[\frac{\log T}{\log T_i}\right]$$

$L_H(T_i)$is the initial temperature T is the current temperature and the cost is estimated as

$$0 = \sum_{\text{net i}} [X(i)Wh(i) + y(i)Wr(i)] \qquad (5)$$

X& y are spans in vertical and horizontal and $W_h$, $W_r$ are wire of our approach where horizontal has no operation

$$C = \sum_{\text{neti}} [y(i) * Wr(i)] \qquad (6)$$

Find cost function n

$$C = \sum_{i=1}^{n} (Oij)\text{^}n \quad (7)$$

&Probability and quantization are given by

$$F(p_i) = \frac{1}{\sum_{p \in p_c} F(p)} \quad (8)$$

## 4 Material based Charge state

The probability of error traced with each device in SRAM cell will get checked by the voltage change and verified it with respect to material and charge mode of the device. The device voltage test was performed at gate, terminals level but the quantization and energy utilization were performed at gate which helps in improving the oxidation process and charge state detection that finally evolved in tracing the error if the bit was shifted even in condition of no charge or temperature variance also it corrects the error.

$$V_G - V_{FB} + \frac{t_{ox}}{2\varepsilon_{o\gamma}} Q_d - V = \frac{t_{ox}}{2\varepsilon_{o\gamma}} Q_e + V_T * \ln\left(\frac{Q_e(Q_e + Q_d) \Big/ \left(4 * V_T * {\varepsilon_{s_i}}/{w_{s_i}}\right)}{q\left(\frac{n_i^2}{N_{s_i}}\right) * w_{s_i}\left[1 - \exp\left(\frac{w_{s_i}}{4 * V_T * \varepsilon_{s_i}}\right)(Q_e + Q_d)\right]}\right) \qquad (9)$$

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

$$V_G - V_D - V_q = -q_m + \ln(-q_m) + \ln\left(\frac{q_z^2}{e^{-q1} - q_z^{-1}}\right) \quad (10)$$

$$C_Q = \frac{q^2 q_v m}{\pi * b^2} (11)$$

The difference between the charge and state along with gate and drain voltages with threshold limit will tell whether the system is in error mode or not. The charge stages at 4 terminals and 3 terminals were calculated for minimizing the load effect of the transistors. This operation was clearly explained with different load effect conditions of the system

## III.RESULTS AND DISCUSSIONS

In table I the 14 T 3 terminal results were compared with existing technologies and yields in 3 to 8% variation in power, 4 to 6% in area and less than 1% effective in compared with existing 22nm technologies like CMOS, FINFET, CNTFET and GNRFET.

Table I: 14T SRAM without DRV

| Performance Metrics | CMOS | FINFET | CNTFET | GNRFET |
|---|---|---|---|---|
| POWER (nW) | 10.84 | 10.2709 | 10.0398 | 9.643232 |
| TOTAL AREA (μm) | 7.10 | 6.72725 | 6.5758 | 6.316139 |
| DELAY (pS) | 5.8 | 5.4955 | 5.371851 | 5.159663 |
| READ DELAY (pS) | 292.82 | 277.447 | 271.2044 | 260.4918 |
| WRITE DELAY (pS) | 17.64 | 16.7139 | 16.33784 | 15.69249 |
| WSNM (mV) | 597.14 | 565.7902 | 553.0599 | 531.214 |
| RSNM (mV) | 98.99 | 93.79303 | 91.68 | 88.06122 |

In table II the14 T 4 terminal results were compared with existing technologies and yields in 3.4 to 7.8% variation in power, 4.2 to 6.3% in area and less than 1% effective in compared with existing 22nm technologies like CMOS, FINFET, CNTFET and GNRFET.

Table II: 14T with DRV

| Performance Metrics | CMOS | FinFET | CNTFET | GNRFET |
|---|---|---|---|---|
| POWER(nW) | 10.7045 | 10.14251 | 9.914307 | 9.522692 |
| SENSITIVE AREA(μm) | 7.01125 | 6.643159 | 6.493688 | 6.237188 |
| DELAY(pS) | 5.7275 | 5.426806 | 5.304703 | 5.095167 |
| READ DELAY(pS) | 289.1598 | 273.9789 | 267.8143 | 257.2357 |
| WRITE DELAY(pS) | 17.4195 | 16.50498 | 16.13361 | 15.49634 |
| WSNM(mV) | 589.6758 | 558.7178 | 546.1466 | 524.5738 |
| RSNM(mV) | 97.75263 | 92.62061 | 90.53665 | 86.96045 |

In table III the15 T 3 terminal results were compared with existing technologies and yields in 1 to 2% variation in power, 0.2 to 0.6% in area and less than 1% effective in compared with existing 22nm technologies like CMOS, FINFET, CNTFET and GNRFET.

Table III: 15T without DRV

| Performance Metrics | CMOS | FinFET | CNTFET | GNRFET |
|---|---|---|---|---|
| POWER(nW) | 10.57069 | 10.01573 | 9.790378 | 9.403658 |
| SENSITIVE AREA(μm) | 6.923609 | 6.56012 | 6.412517 | 6.159223 |
| DELAY(pS) | 5.655906 | 5.358971 | 5.238394 | 5.031478 |
| READ DELAY(pS) | 285.5453 | 270.5541 | 264.4667 | 254.0202 |

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

| | | | | |
|---|---|---|---|---|
| WRITE DELAY(pS) | 17.20176 | 16.29866 | 15.93194 | 15.30263 |
| WSNM(mV) | 582.3048 | 551.7338 | 539.3198 | 518.0167 |
| RSNM(mV) | 96.53072 | 91.46285 | 89.40494 | 85.87345 |

In table IV the15T 4 terminal results were compared with existing technologies and yields in 1 to 2% variation in power, 0.2 to 0.6% in area and less than 1% effective in compared with existing 22nm technologies like CMOS, FINFET, CNTFET and GNRFET.

Table IV:15T with DRV

| Performance Metrics | CMOS | FINFET | CNTFET | GNRFET |
|---|---|---|---|---|
| POWER(nW) | 10.43856 | 9.8905636 | 9.667999 | 9.286113 |
| SENSITIVE AREA(µm) | 6.837064 | 6.478118 | 6.332361 | 6.082232 |
| DELAY(pS) | 5.585207 | 5.291984 | 5.172914 | 4.968584 |
| READ DELAY(pS) | 281.9759 | 267.1722 | 261.1608 | 250.845 |
| WRITE DELAY(pS) | 16.98673 | 16.09493 | 15.73279 | 15.11135 |
| WSNM(mV) | 575.026 | 544.8371 | 532.5783 | 511.5415 |
| RSNM(mV) | 95.32408 | 90.31957 | 88.28738 | 84.80003 |

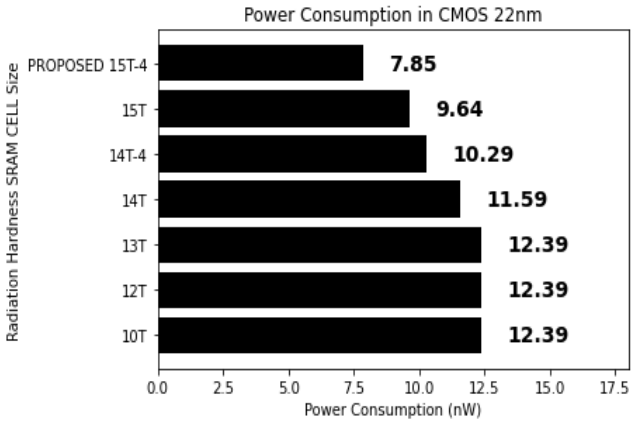



**Figure III: Power Consumption in CMOS 22nm technology**

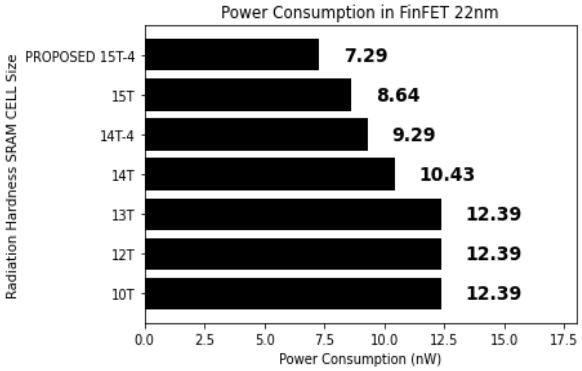



**Figure IV: Power Consumption in FinFET 22nm technology**

From figure III to figure VI, different technology-based FET power consumption was compared, and it is observed that GNRFET yields the best result compared with other technologies.

IJIREEICE ISSN (O) 2321-2004, ISSN (P) 2321-5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified ⁜ Impact Factor 7.047 ⁜ Vol. 10, Issue 6, June 2022

DOI: 10.17148/IJIREEICE.2022.10648

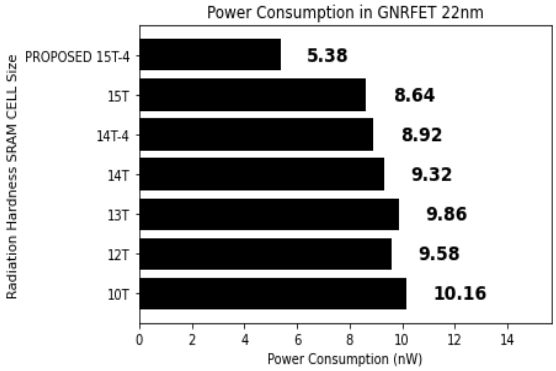



**Figure V: Power Consumption in GNRFET 22nm technology**

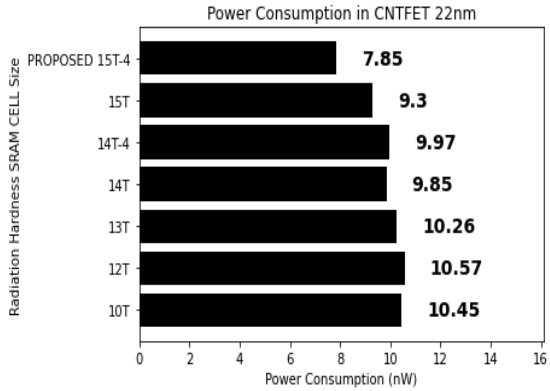



**Figure VI: Power Consumption in CNTFET 22nm technology**

## IV. CONCLUSIONS

Various technologies and the performance of designed memory cells are compared, which can be used for space applications. These memory cells possess high radiation limit hardness and reduce the corruption of data bits. The proposed model minimizes the hardness effect, and soft error correction is also implemented with minimal current requirement using an inbuilt design. As a result, the effective area was minimized by 7.8%, power reduced by 12.8%, and the delay factor reduced by 13.2% compared to existing approaches on the maximum scale. Out of all the technologies, 22nm GNRFET yields the best results on a comparative scale.

## REFERENCES

[1] M. Brown and B. Lakshmi, "Investigation of Radiation Hardened TFET SRAM Cell for Mitigation of Single Event Upset," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 1397-1403, 2020, DOI: 10.1109/JEDS.2020.3002265.

[2] T. Li, H. Liu, and H. Yang, "Design and Characterization of SEU Hardened Circuits for SRAM-Based FPGA," in IEEE Transactions on Very Large scale integration (VLSI) Systems, vol. 27, no. 6, pp. 1276-1283, June 2019, DOI: 10.1109/TVLSI.2019.2892838.

[3] A. Haran et al., "Single-Event Upset Tolerance Study of a Low-Voltage 13T radiation-hardened SRAM Bitcell," in IEEE Transactions on Nuclear Science, vol. 67, no. 8, pp. 1803-1812, Aug. 2020, DOI: 10.1109/TNS.2020.3002654.

[4] S. Pal, D. D. Sri, W. -H. Ki and A. Islam, "Highly Stable Low Power Radiation Hardened Memory-by-Design SRAM for Space Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 6, pp. 2147-2151, June 2021, DOI: 10.1109/TCSII.2020.3042520.

[5] Y. Han et al., "Radiation Hardened 12T SRAM With Crossbar-Based Peripheral Circuit in 28nm CMOS Technology," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 7, pp. 2962-2975, July 2021, DOI: 10.1109/TCSI.2021.3074699.

[6] C. Naga Raghuram, B. Gupta and G. Kaushal, "Double Node Upset Tolerant RHBD15T SRAM Cell Design for Space Applications," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 1, pp. 181-190, March 2020, DOI: 10.1109/TDMR.2020.2970089.

DOI: 10.17148/IJIREEICE.2022.10648

[7] M. S. M. Siddiqui, S. Ruchi, L. Van Le, T. Yoo, I. Chang and T. T. Kim, "SRAM Radiation Hardening Through Self-Refresh Operation and Error Correction," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 2, pp. 468-474, June 2020, DOI: 10.1109/TDMR.2020.2994769.

[8] C. Peng et al., "Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 2, pp. 407-415, Feb. 2019, DOI: 10.1109/TVLSI.2018.2879341.

[9] J. Wang, J. Prinze, A. Coronetti, S. Thys, R. G. Alia, and P. Leroux, "Study of SEU Sensitivity of SRAM-Based Radiation Monitors in 65-nm CMOS," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 913-920, May 2021, DOI: 10.1109/TNS.2021.3072328.

[10] D. Kobayashi et al., "Process Variation Aware Analysis of SRAM SEU Cross Sections Using Data Retention Voltage," in IEEE Transactions on Nuclear Science, vol. 66, no. 1, pp. 155-162, Jan. 2019, DOI: 10.1109/TNS.2018.2882221.

[11] Y. Han, X. Cheng, J. Han, and X. Zeng, "Radiation-Hardened 0.3–0.9-V Voltage-Scalable 14T SRAM and Peripheral Circuit in 28-nm Technology for Space Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 4, pp. 1089-1093, April 2020, doi: 10.1109/TVLSI.2019.2961736.

[12] C. I. Kumar and B. Anand, "A Highly Reliable and Energy Efficient Radiation Hardened 12T SRAM Cell Design," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 1, pp. 58-66, March 2020, DOI: 10.1109/TDMR.2019.2956601.

[13] A. Elwailly, J. Saltin, M. J. Gallagher, and H. Y. Wong, "Radiation Hardness Study of LG = 20 nm FinFET and Nanowire SRAM Through TCAD Simulation," in IEEE Transactions on Electron Devices, vol. 68, no. 5, pp. 2289-2294, May 2021, DOI: 10.1109/TED.2021.3067855.

[14] E. Wilson, S. Larsen, C. Wilson, C. Thurlow, and M. Wirthlin, "Neutron Radiation Testing of a TMR VexRiscv Soft Processor on SRAM-Based FPGAs," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 1054-1060, May 2021, DOI: 10.1109/TNS.2021.3068835.

[15] S. Pagliarini, L. Benites, M. Martins, P. Rech, and F. Kastensmidt, "Evaluating Architectural, Redundancy, and Implementation Strategies for Radiation Hardening of FinFET Integrated Circuits," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 1045-1053, May 2021, DOI: 10.1109/TNS.2021.3070643.

[16] J. Prinze, S. Thys, B. Van Bockel, J. Wang, V. De Smedt, and P. Leroux, "An SRAM-Based Radiation Monitor With Dynamic Voltage Control in 0.18- $\mu$ m CMOS Technology," in IEEE Transactions on Nuclear Science, vol. 66, no. 1, pp. 282-289, Jan. 2019, DOI: 10.1109/TNS.2018.2885693.

[17] S. Pal, S. Mohapatra, W. -H. Ki and A. Islam, "Design of Soft-Error-Aware SRAM With Multi-Node Upset Recovery for Aerospace Applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 6, pp. 2470-2480, June 2021, DOI: 10.1109/TCSI.2021.3064870.

[18] Q. Zhao, C. Peng, J. Chen, Z. Lin, and X. Wu, "Novel Write-Enhanced and Highly Reliable RHPD-12T SRAM Cells for Space Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 3, pp. 848-852, March 2020, DOI: 10.1109/TVLSI.2019.2955865.

[19] A. Yan et al., "Novel Speed-and-Power-Optimized SRAM Cell Designs With Enhanced Self-Recoverability From Single- and Double-Node Upsets," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, pp. 4684-4695, Dec. 2020, DOI: 10.1109/TCSI.2020.3018328.

[20] D. Kobayashi et al., "Data-Retention-Voltage-Based Analysis of Systematic Variations in SRAM SEU Hardness: A Possible Solution to Synergistic Effects of TID," in IEEE Transactions on Nuclear Science, vol. 67, no. 1, pp. 328-335, Jan. 2020, DOI: 10.1109/TNS.2019.2956760.

[21] N. R. CH, B. Gupta, and G. Kaushal, "Single-Event Multiple Effect Tolerant RHBD14T SRAM Cell Design for Space Applications," in IEEE Transactions on Device and Materials Reliability, vol. 21, no. 1, pp. 48-56, March 2021, DOI: 10.1109/TDMR.2021.3049215.

[22] E. Keren, S. Greenberg, N. M. Yitzhak, D. David, N. Refaeli, and A. Haran, "Characterization and Mitigation of Single-Event Transients in Xilinx 45-nm SRAM-Based FPGA," in IEEE Transactions on Nuclear Science, vol. 66, no. 6, pp. 946-954, June 2019, DOI: 10.1109/TNS.2019.2916151.

[23] L. Wen, Y. Zhang, and P. Wang, "Radiation-Hardened, Read-Disturbance-Free New-Quatro-10T Memory Cell for Aerospace Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 8, pp. 1935-1939, Aug. 2020, DOI: 10.1109/TVLSI.2020.2991755.

[24] W. Liao et al., "Impact of the Angle of Incidence on Negative Muon-Induced SEU Cross Sections of 65-nm Bulk and FDSOI SRAMs," in IEEE Transactions on Nuclear Science, vol. 67, no. 7, pp. 1566-1572, July 2020, DOI: 10.1109/TNS.2020.2976125.

[25] A. Pérez-Celis, C. Thurlow and M. Wirthlin, "Identifying Radiation-Induced Micro-SEFIs in SRAM FPGAs," in IEEE Transactions on Nuclear Science, vol. 68, no. 10, pp. 2480-2487, Oct. 2021, DOI: 10.1109/TNS.2021.3108572.