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A Review on Design of Comparators using 45nm Technology

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Abstract: Analog to Digital Converter (ADC) is a most useful devices for extracting the digital signals from the analog signals. The processing speed of successive approximation type ADC is depending highly on the operations of the comparators, which is the important parts of structure. In day todays digital ultratech world, low power consumption & speed are the major factor that need to be considered. High speed comparator is much affective to the overall performance of ADC. In order to design a better comparator that will function optimally in real environments without changing its characteristic. Factors like propagation delay, power dessipation, and voltage supply must be taken into account when designing a low power and voltage comparator. These factors are represented in this paper. This essay compares several comparators, including complex circuit, length of design, CMOS technology, and others. A 45nm-based comparator's design, followed by a Cadence Virtuoso simulation.

Keywords: Analog-to-Digital-Converter (ADC), Digital-to-Analog-Converter (DAC), Successive Approximation Register (SAR), Low Power, High speed clock frequency, Conventional Dynamic.

I. INTRODUCTION

Due to the benefits of digital communication, digital signals are currently used more frequently than analog ones. As a result, several analogs to digital converters are in use, such as flash ADC and SAR ADC. Comparators are used in huge numbers in a SAR ADC. Comparators are utilized nearly universally in ADCs, not just flash ADCs, as the fundamental building component for them. Depending on the input polarity, a comparator is a non linear circuit component that it makes difficult judgments.

The major distinction between a comparator and a linear circuit, such as an amplifier, is that a comparator may have different values at various times. Comparators, which are frequently found ADCs, communication system, memory sense amplifier, and some storage elements, are among the most crucial and basic parts in the design of analog and mixed signal circuits. They are referred to as decision-making circuits most often.

Fig. 1.1 displays the Comparator's block diagram. Comparators can primarily influence the power dissipation and speed of the overall ADC since they serve as the interface between the analog and digital domains in ADC system design. the circuit that contrasts the analog signal acquired by the DAC with the sampled analog input signal. As a result, the digital "0" or "1" that will be supplied to the SAR Logic is generated. Accuracy and speed are the determining variables for the comparator.

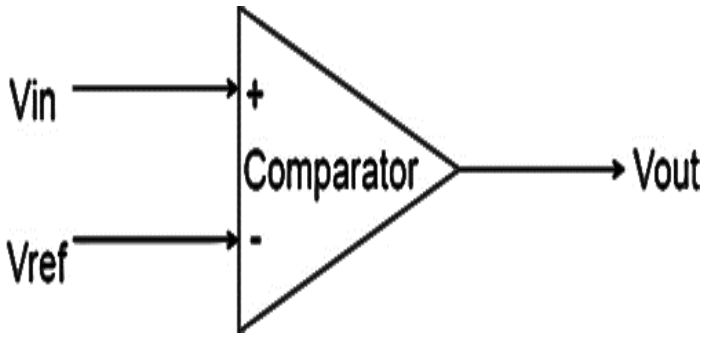

Fig 1.1 Comparator

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II. LITERATURE REVIEW

Anil Khatak et al., [1] In order for the ADC to analyze data fast, this interacts with the comparators, this is a critical component of the SAR ADC. Three criteria are used in this article to analyze & contrast different comparators: technology, supply voltage, and power. Depending on various temperature points, the Propagation delays, power dissipation of various comparators will be investigated. The comparison includes a number of different comparators, such as voltage supply, circuit complexity, length, and CMOS technology. Simulated 90 nm CMOS devices have been utilized using SPICE.

Shruti Pancholi et al., [2] Have presented the schematic design of a CMOS comparators with fast speed, low power dissipation, and Low noise is presented in this work. The simulation results demonstrate that this architecture is compatible with high-speed clock frequencies of 1000MHz. For a pipeline ADC, a CMOS comparator with S-edit design and simulation has been created. Here, just one comparator has been demonstrated and modelled. The comparator used 0.25mw of minimal power dissipation during operation. Tanner EDA software version 1 is used to simulate the comparator using 45nm CMOS technology.

Sanjay Kumar Jaiswal et al., [3] Have presented the, two distinct CMOS binary comparator designs are shown; one is more power efficient and uses less power. Two outputs, X and Y, are generated by the circuit. When A > B, X is engaged; when AB or A = B, it is not engaged. When A equals B, Y is activated; otherwise, it is not. Our methods involve creating an 8-bit comparator's symbol after initially designing a 1-bit comparator as a single component. The comparator is built using a CMOS circuit and the logic relationship between various input and output.

Ranjeet Kumar et al., [4] Have discussed the design of an 8-bit binary comparator utilizing 45nm CMOS technology. Less space and less transistors are required in this design, and power and execution time are also covered. X, Y, and Z are the circuit's three outputs. When A > B, Y, and Z are all active high, x is active high. When A = B, Z, y, and Z are all active low, x is active low. Create a 1-bit comparator using a pre - charge gate. By connecting them in series with a pass transistor in between, the concept of a 1-bit comparator has been expanded to produce an 8-bit comparator.

Suryasnata Tripathy1 et al., [5] have designed the 8 bit magnitude comparator is Designed and Implemented using Cadence virtuoso software. The architecture is designed on the basis of pass transistors logic circuit and static CMOS logic circuit and is implemented using 90 nm CMOS technology with the Cadence virtuoso software. This proposed topology's layout is created with the Layout XL editor of the Cadence EDA tool on the Cadence virtuoso platform.

Constantinos Efstathiou et al., [6] have introduced a new efficient majority logic magnitude comparator with full tree architecture. The proposed magnitude comparators use fewer majority gates and have a shorter critical path than previously published majority logic magnitude comparator designs.

Sahil Jakhara et al., [7] have proposed an energy efficient, fast, and low voltage dynamic comparators. The comparator's delay and offset voltage are determined via exhaustive statistical analysis. The comparator now operates at 3.07 GHz with a 0.3 W power consumption, which represents a considerable reduction in latency. This research also proposes a novel architecture for a high Speed, power efficient dynamic comparator for analogue to digital converters. As compared to other current architectures, a significant increase in performance and low power consumption has been seen in simulations using 180 nm technology and 1.8V supply voltage.

Shreeniwas Daulatabad et al., [8] have offered a novel double tail architecture-based comparator design for an 8-bit SAR ADC converter. ADC_converter with an R2R Ladder type DAC_converter, a novel comparator that was proposed, to simulate the circuit using a predictive technology model employing 70nm Technology, Tanner EDA tool is utilized. With a supply voltage of 1.2 volts and a clock frequency of 2GHz, the proposed ADC uses just 1.3mW of power. The recommended comparator, a double tail type, functions effectively at 1.2 volts of supply voltage and achieves 8-bit precision due to minimum MOSFET stacking and low kickback noise.

Fotios Ntouskas et al.,[9] this paper is focuses on the design of the magnitude and 2 s complementary comparators. It is suggested to use new OR based complete tree and simple tree magnitude comparator designs. After comprehensive experimental research, the suggested and realized comparator designs are tested in both high-performance and relaxed environments using standard cell technology. While running at the same speed as the present comparators, the suggested ones perform quicker and result in a substantial reduction in power consumption and space complexity. The suggested 2 s complementary comparator are more effective than the 2's complement comparator designs that are already in use, but they share the similar architecture, thus the similar complexity as their comparable Magnitude comparator.

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Chang Chua et al., [10] have introduced a novel prefix tree-based parallel binary comparator architecture that is low-power and area-efficient. An urgent need exists to optimize the binary comparator for very less power devices because of its widespread use in CPUs. Suggested binary comparator uses a new EX_OR_NOR gate as a pre. encoder to cut down on space, power, and latency. Using Cadence for CMOS 180nm technologies, simulation is run. 2 binary comparators designs having better performances are suggested in this research. Also, compared to previous methodologies, results in power reductions of up to 25%, area reductions up to 36%, and improvements to the delay performance of 27%.

Hasan Molaei et al., [11] have introduced, a new hybrid ADC with a decreased comparator is presented. The suggested_ADC performs a high-speed_low-power conversion using dynamic comparators. A new low-kickback noise comparator with a high pre-amplifier gain is introduced in order to lessen the offset and kickback noise effect of conventional dynamic comparators. Two_1.8 input V, 0.18 m CMOS_technology, 4 bit and 8-bit ADCs are constructed. The suggested ADC_performs a high speed, low power conversion in dynamic comparators.

Young-Ho Seo et al. [12] In this research, a novel approach for comparing the magnitude of several digital input signals is proposed. The logic circuit is also introduced at Register_Transfer_Level. The suggested approach employs a straight forward digital logic functions to provide information on the Largest (or lowest) values and positions for these inputs while comparing several inputs simultaneously. This method's drawback is that it uses more hardware resources than necessary. They provide a reusable approach for the overlapped logic operations to get around this. The suggested approach mainly focuses on raising operating clock frequency or to put it another way, cutting down on combinational delay time.

Roshani Gupta et al., [13] have described a fast and efficient 4-bit comparator that can be expanded to 32*2 bits utilizing floating-gate MOSFETs. The voltage of the floating-effective gate in FGMOS, as previously stated, is the weighted average of a number of input voltages capacitively connected to the floating-gate. In addition, the proposed 4-bit comparator circuit's performance has been compared to that of previous comparator circuits developed using the CMOS, Transmission gate, Pass transistor logic, and Gate Diffusion input techniques.

Vijay Savani et al., [14] have introduced, a dynamic latch comparator with a revolutionary architecture that can deliver high speed, less power, and a very small die area is introduced. The suggested comparator uses a novel reset method based on shared charge logic to achieve more speed and less power consumption. Simulations and analysis demonstrate that the delay time is drastically decreased as compared to a traditional dynamic-latched comparators. 90 nano meter C-MOS_tech.. is used for the design and simulation of the suggested circuit. Also, a thorough comparison of the suggested dynamic latch comparator and the conventional comparator's delay time is provided.

Rony Antony et al., [15] In a DSP processor, a floating-point value comparison is done by basic arithmetic operations. The parallel prefix tree design is used to its fullest extent by this comparator. When the compared bits are equivalent, it compares the most significant bit first before moving on to the less significant bit. The findings demonstrate how effectively the new comparator design handles all of the incorrect point integers. In these_suggested_comparators equates the point digit with a double precision and has the added benefit of handling invalid instances. Hence, high precision processes can employ this comparator.

Avaneesh K. Dubey et al., [16] have proposed a bulk driven method for constructing CMOS two-tail dynamic comparators. The suggested drives the inputs using loads that are bulk-driven using a gate-driven approach. An examination of the Delay & 0ffset caused by mis-match mathematically is shown for the suggested comparator. In order to control both kickback noise and offset voltage, a new, optimized control unit architecture is also suggested. At_0.8v of the input voltages at the 45 nano meter CMOS technology nodes, it is simulated in SPECTRE to validate the results. Over a traditional design, the suggested comparator achieves a 27% reduction in energy usage and an 87% reduction in latch delay. The outcome indicates that utilizing optimization technique, the offset voltage is decreased by 62%.

Amy Mariam George et al., [17] have presented a Parallel Prefix Radix 2 8-bit comparators with constant delay (CD) logic. Using a critical path timed PMOS transistor, the constant delay logic charges the output to logic zero before switching to logic one. CD logic is significantly faster than dynamic logic in its D-Q mode of operation. The comparator architecture is divided into two stages, the first of which employs low power pass transistor pre-encoding-circuitry, and the second of which employs high performance dynamic-CD-static logic method combination comparators.

Roman Sotner et al., [18] have focused on a newly developed generator uses a small amount of vo1tage controllable amplifiers and electrically controllable current conveyors or adjustable current amplifiers serve as the foundation for both

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passive and active components. Effects of statistical dispersion on key parameter of the non-ideal voltage gain of a programmable amplifier employed.

M. Vafaei et al., [19] have shown how to replace an outdated low power dynamic comparator with a SAR ADC at supply voltages of 0.2 V. The recommended low power comparator in this design, together with the use of power reduction methods, have reduced the SAR ADC's power consumption by 70%. has a self-power gating device built within it that limits how much power its opponent may consume? Moreover, a bootstrap switch is used in the recommended design to produce the 0.2 V supply voltages.

Roohollah Sanati et al., [20] have described a time-domain comparator with ultra-low-power-consumption that operates at low supply voltages. The main idea behind this work is to use a transistor's bulk terminal as one of the comparator's-subthreshold inputs. The suggested comparator consumes approximately 250 nW at a supply voltage of 1 V and has a resolution of less than 0.4 mv at a clock frequency of 2.5 MHz, according to the post-layout simulation results for 180-nm TSMC technology.

K.B. Maji et al., [21] demonstrated how to modify a SAR_ADC_with a brand-new low_Power_dynamic_comparator_at 0.2_V supply voltage. With the design of the suggested low power comparators and the application of power reduction techniques, the SAR ADC's power consumption has been decreased by 70%. isbuiltwith_a_self_power_gating_mechanism that reduces the power use for its rival.

V.Deepika et al., [22] have explained low power comparators_for high-speed application. It is based on the regenerative feedback used in the dynamic comparator and in non-clocked comparator. It was simulated in 90nm technology at 3.3V supply and the power consumption is reduced by 58%.

Ashima Gupta et al., [23] The digital design is far more resistant to process, voltage, and temperature fluctuations and needs less design work. The Cadence virtuoso analogue design environment was used to create the suggested comparator and simulate it. An analogue voltage comparator that was created utilizing digital design methods has been discussed. The simulation outcomes from the Cadence Virtuoso simulator using SCL 180 nm CMOS technology have been examined.

Mohammad Asyaei [24] have used the method_to_reduce_the_delay_caused_by parasitic_capacitance on_the_dynamic node, the enormous pull-down network in the recommended dynamic circuit is divided into smaller networks in this article. HSPICE is used to simulate both the suggested dynamic circuit and alternative circuit designs in a 45 nm CMOS technology model. The recommended circuits were used to build the 40_bit tag-comparators displayed below. According to simulation findings, the suggested circuit offers the same amount of noise protection while operating more quickly and efficiently.

Mohamed Morsi et al., [25] have presented a method that it was used to reduces the time delayed in the LC ADC systems. It is implemented 45 nano m and 130 nano meters_technology. It was designed by adding conventional comparator and one transistor. The main conclusion of this project is to it will decrease the time delay and low power consumption. The power was reduced to 348uW in proposed system and 452uW in proposed system.

III. SUMMARY AND OBSERVATION

A critical component of ADC design is the comparator design. In this paper, performance measures for comparators as well as several types of comparators, including open loop comparators, re-amplifiers used before latch comparators, dynamic comparators, and others, are explored. This article also identifies the de1ay & power dissipation of different category comparators. Additionally, it includes a comparison of several comparators, including voltage supply, circuit complexity, length, and CMOS technology, this will assist to discover the circuits which consumes less_power and which operates with fast speed.

IV. CONCLUSION

Several researchers have demonstrated in recent years that the mentioned design strategies are good design schemes for optimizing comparator performance. As a result, this paper merely provides an explanation of the Comparator's properties, architecture, and numerous factors such as delay, offset voltage, output impedance, and voltage gain that must be addressed in every design for different papers. Nevertheless, any topology is chosen according on the application and the needs. Further circuit improvements will be performed in the future to further minimize power consumption by adopting dynamic and analog implementations for this Comparator resolution module circuit for the decision.

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