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REVIEW ON POWER OPTIMIZATION TECHNIQUES FOR JOHNSON COUNTER DESIGN

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Abstract: Due to the ongoing reduction in chip size, power minimization is the primary design focus in VLSI circuits. The development of VLSI systems relies heavily on CMOS technology because it uses less power. Modern integrated circuit (IC) designers aim to create digital circuits with low power consumption in very large scale integration (VLSI) ICs. This is done to increase the circuit's battery life, especially if it is intended for wearable technology. Counters are frequently employed in digital circuits, and these counters demand a lot of power. Reduced power usage across the board is necessary to have an effective digital system. Thus, this paper aims to provide the various power optimization techniques that can be incorporated in Johnson Counter design in order to reduce the power dissipation of the counter. Also these techniques can be incorporated in other counter design as well.

Keywords: Complementary Metal Oxide Semiconductor (CMOS), Integrated Circuit (IC), Very Large Scale Integration (VLSI), Low power, Johnson Counter, Flip-Flop.

I. INTRODUCTION

One of the main problems with designing VLSI circuits is power consumption, and CMOS is the most common technology used. Dynamic and static components make up CMOS's power consumption. During the switching of transistor, regardless of transistor switching, static power is consumed together with dynamic power.

The primary sequential circuits that are typically employed in modern digital systems are counters and registers. Several data sequences are needed in these digital systems to conduct various actions, necessitating the creation of various counters. A critical element of high-performance digital systems is the requirement for low power architecture. Power dissipation has emerged as one of the main issues when the system feature size gradually decreases and frequency rises quickly. The chip's power dissipation increases with a high operational frequency. Mobile phones, laptops, and other battery-operated portable devices have contributed to the demand for power reduction in such systems. Hence it is necessary to design circuits that consume less power.

A sequential circuit known as a Johnson counter offers unique data sequences. The input of the first flip-flop is paired with the inverted output of the last flip-flop in this variation of the ring counter. Compared to the ring counter, it requires half as many stages. A specific data sequence that can be used in a variety of circumstances will be generated. The objective of this project is to design and implement a low power Johnson counter with better performance using few power optimization techniques. They can be used in all forms of digital logic and computing to count a particular event or pulse occurring in the circuit and to follow either a predetermined or random pattern, depending on the design.

II. LITERATURE REVIEW

Namrata Joshi et al.,[1] has proposed a 4-bit Johnson Counter using BICMOS (A modified ring counter known as a Johnson counter is one where the input of the first flip flop is paired with the inverted output of the last flip flop.) Technology using Cadence Virtuoso Schematic Editor. The results of this proposed counter were compared with conventional logic and MTCMOS (Multi-threshold CMOS) logic at certain frequencies and came to a conclusion that BICMOS circuit consumes less energy.

Nur Syuhadah Amran et al.,[2] has proposed a design of Johnson counter using clock gating technique. The proposed 4-bit Johnson Counter's clock gating approach is compared to another 4-bit Johnson Counter without clock gating mechanism. This led to the discovery that the Johnson Counter utilising the clock gating technique only consumes

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21.22µW of power, as opposed to the standard Johnson Counter's 67.09µW. Hence, when a clock gating approach is utilised, the power consumption is decreased by around 68.3%.

T. Suguna et al.,[3] has done a survey on power optimization techniques for low power VLSI circuit. Almost all design levels are covered by the numerous power optimisation approaches that were given in this paper. It can be said that crucial performance parameters like dynamic power, propagation delay, and PDP are closely related to one another. The majority of research has concentrated on developing adiabatic logic, which is a promising architecture for low power applications, to satisfy today's power needs. We can state that the adiabatic approach is a sophisticated way for power reduction and that it produces superior outcomes to traditional techniques.

K. Ram Bharatkumar et al.,[4] has implemented Johnson counter using Diode-Free Adiabatic Logic. Several strategies are compared with the Johnson counter like GDI (Gate Diffusion Input), TG, CPL (Combined Programming Language), 2PSAL, CMOS, DFAL (Diode-Free Adiabatic Logic). By using DFAL when compared to all other ways, there is a 60% energy savings.

R.Gurunadha.,[5] Several academics are particularly interested in the topic of power dissipation because it is a crucial performance parameter of any electronic system. A fundamental component of electronic systems known as a frequency divider dissipates a tremendous amount of power and uses a significant amount of energy. In this study, a frequency divider-by-3 circuit that outperforms static CMOS logic-based inverters and frequency divisions by 3 in terms of power dissipation and power delay product is designed using diode free adiabatic logic (DFAL). TSPICE simulator is used to confirm the implemented circuit's functionality. For all measured frequencies, it can be seen that the suggested inverter offers nearly 81.5% energy savings and 13.44 adiabatic gains. For all recorded frequencies, frequency divided by three results in an energy savings of around 91.24% and an adiabatic gain of 15.73.

Varsha Dewre et al., [6] developed a Johnson counter with a smaller transistor count and lower power dissipation than a clock gated counter design. It employs Gate Diffusion Input-based clock gated logic and pulse-triggered flip flops. The simulation findings show a reduction in power of up to 28.57% when compared to the standard design.

Garima Bhargave et.al.,[7] demonstrates the use of Power-Gating CPAL (Complementary Pass Adiabatic Logic), which saves more power in the frequency range of 5 MHz to 100 MHz than CMOS logic. According on the simulation results, the suggested architecture uses 10% to 15% less power than traditional CMOS logic.

Abhishek Rai et al.,[8] designed a 4-bit Johnson ring counter which was made using a negative edge triggered D flip-flop in a micro wind instrument at 90 nm technology. This will decrease the counter's area and energy requirements. Here, the semi-custom layout design dissipates 139 W while the auto generated layout design dissipates 25.095 W.

Bhima Venkata Sujatha et al.,[9] designed a 4-bit Johnson up-down counter that uses clock gating and the DDFF-ELM (Dual Dynamic node Hybrid Flip-Flop) to operate efficiently. According to the results of the simulation, the power dissipation of a Johnson counter with clock gating is 33.9% lower than that of a Johnson counter without clock gating.

Chandra shekhar kotikalapudi et al.,[10] has proposed a 4 bit up-down Johnson counter that uses a Dual Dynamic Node Pulsed Flip-flop (DDFF) employing logic module (DDFF-ELM) approach to reduce power consumption. Clock gating is then used to further reduce power consumption. Without clock gating, the proposed circuit consumes 344.24 w of power, but clock gating reduces it to 160.56 w.

Jitesh Shinde et al.,[11] has proposed one of the power-saving method called clock gating. Clock gating is the practise of turning on a logic block's clocks only when work has to be done in order to conserve power. This study examines the various clock gating methods that can be used to reduce power consumption in VLSI circuits at the RTL level as well as the problems that can arise when doing so. In the upcoming designs at 45nm and down, clock power will likely increase dramatically. Clock power currently accounts for 50–70% of total chip power. Traditionally restricted to the synthesis, placement, and routing stages, power optimisation has advanced to the system level and RTL phases.

M.R.Sangameswari et al.,[12] The excessive power dissipation that existed in the XCFF is eliminated by the DDFF. The flip-flops were compared, and it was discovered that DDFF exhibited lower power dissipation and comparable speed performances. Analysis was done on the performance of 4-bit Johnson up-down counters with standard MUX and 4-bit Johnson up-down counters with DML logic. Depending on the needs of the system, DML logic can operate in either static or dynamic modes. Static DML mode can be used to save energy, and dynamic DML mode can produce better performance.

Ranjana Yadav et al.,[13] has proposed a MTCMOS approach to design a low power Johnson Counter. Power delay products have undergone comparative analysis of power dissipation at specific frequencies, and the findings have been compared to traditional design. By employing the proposed Johnson counter at 600MHz, the power usage is 97u as opposed to 161u when using the standard approach.

Morasa Balaji et al.,[14] With the advance of each generation of the fabrication process a five-fold increase in leakage power dissipation is present. While the circuit is unused, leakage currents occur, wasting electricity. Techniques for effectively reducing leakage power are becoming essential for deep submicron and nanometre circuits. In this study, a 4-bit Johnson counter is created using the LECTOR approach and examined using several sleep analysis methods.

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To keep track of the circuit states, LECTOR doesn't require any extra control circuitry. Also, the LECTOR methodology uses the least amount of space feasible to significantly minimise power consumption, and this technique may be used to several integrated circuits to increase power efficiency.

C.Arunabala et al.,[15] has designed a voltage-dependent oscillator constructed utilising a 0.7-m CMOS technology, and a D flip flop that can handle data at high frequencies with little power consumption was put into practise and successful. Low power consumption designs use this kind of CMOS DFPFP. This design reduces power consumption from 12.87 nw to 8.82 nw, or 68.53% less, while reducing propagation latency from 138.6 ns to 68.9 ns, or 49.71% less.

Pragya Naik et al.,[16] has proposed a D flip-flop-based efficient 4-bit, 8-bit, and 16-bit ring counter and Johnson counter. It is optimised for the shortest possible combinational path delay (MCPD). Given that the propagation delay in the suggested counter is found to be lowest for Spartan 3, the proposed design exhibits superior performance in terms of speed. Power dissipation for both counters is lowest for Spartan 6 FPGA which uses 45 nm low power copper process technologies that offers the best compromise between cost, power, and performance. By using this type of FPGA (Spartan 6), we can reduce the power consumption and dissipation as the transistor size is reduced in this technology.

Divya Bora et al.,[17] Tanner EDA tool was used to build and simulate certain digital circuits, including logic gates, half adders, and full adders. Because BICMOS logic was used in the construction of all of these circuits, they all offer certain benefits including quick switching, high gain, the capacity to drive big loads, low output impedance, and low static power. Moreover, latch up condition can be entirely removed.

Swati Singh et al.,[18] has designed a Johnson counter using four master-slave Flip-Flops. Clock gating is used to operate all flip flops. The design uses both the clock gating approach and the MTCMOS technique to significantly reduce power consumption. In this proposed system, power dissipation has been reduced by 76.7%, and energy dissipation has been reduced by 76.80%. Using this suggested method, PDP is reduced by 59.40%.

Ms. Himanshi Sharma et al.,[19] developed a Johnson counter architecture that combines a power gating circuit and CPAL logic. Four D flip flops are used to implement a four bit architecture. When compared to traditional designs, the circuit created utilising CPAL logic dissipates a lot less power. The proposed device dissipates roughly 92% and 50% less power, respectively, than a traditional Johnson counter and a CPAL mod-8 counter.

Manish Kumar Soni et al.,[20] has designed a 4-bit Johnson counter that used fewer transistors and a negative edge-triggered master slave D flip flop. Power dissipation, latency, and transistor count have all been taken into account in the performance and cost analysis of the suggested counter. The proposed design is contrasted with the standard Johnson counter design. The proposed design is found to perform better in terms of both power dissipation and propagation latency. Compared to the traditional design, the proposed design's power dissipation has decreased to 0.2079 nW from 0.36618 nW.

Tanushree Doi et al.,[21] proposed a ring counter employing 90nm CMOS technology in the Cadence tool whose performance is compared to that of the traditional version. Since there are fewer transistors used in a pulsed latch than in a flip flop, less space is needed. The pulsed latch strategy reduces the power dissipation and power delay product by 15.54% and 27.37%, respectively.

Yogita Hiremath et al.,[22] has designed a 4-bit up counter using master-slave negative pulse-triggered D flip-flops. The master slave D flip-flop is constructed with 8 nand gates, an inverter, and a D flip-flop. Area, latency, and power consumption are used to evaluate the counter's performance. The estimated power of the counter *is* 97.90µW and delay is 20.39ns.

Saumya Pandey et al.,[23] designed a Johnson counter which consumed less power with the aid of a pulse-triggered flip flop and clock gated logic based on GDI. In comparison to the traditional Johnson counter and the clock gated Johnson counter, the proposed design exhibits power reductions of 66.73% and 44.76%, respectively. The proposed design has a power dissipation range of 36.68 W to 54.69 W for frequencies between 600 MHz and 1 GHz.

K.Srilatha et al.,[24] proposed a D Flip-Flop using Micro Wind and DSCH Tools that is CMOS based. For instance, a D flip-flop using 32nm technology for micro wind uses 0.20uW of power and takes up 56.4 um2 of space.

Rohith Nama et.al.,[25] proposed a circuit structure known as the "Power Gated Sleep Method", which is a novel cure for designers. Of all the techniques, this one exhibits the lowest speed power product. The method offers extremely low leakage power consumption with a great deal less speed, especially as it uses roughly 50% to 60% less power than the current. In order to increase area and power efficiency, it can be used in future ICs.

III. SUMMARY AND OBSERVATION

Digital electronics employ Johnson counters to store, process, or track the amount of occurrences that occurred inside the circuit. One of the circuits in digital sequential logic which can count several pulses is Johnson Counter. They are built using a large number of flip-flops and an extra clock signal. They are employed in all forms of digital logic and computation to keep track of the precise event or pulse constantly occurring in the circuit, and depending on the design,

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they may or may not follow a predetermined pattern. Johnson counters are employed as pattern recognizers and frequency dividers. It serves as a divider and synchronous decade counter circuit. In hardware logic design, it can be used to construct intricate finite state machines.

The Johnson Counter uses various techniques like lector, BICMOS logic, DFAL, clock gating approach to ensure that power consumption is minimised. From the literature survey, it is seen that clock gating saves up to 68.3% of the total power [2]. The lector technique is also an efficient technique which reduces overall power consumed by Johnson counter [14]. The goal of the project is to design a power efficient Johnson counter. It is done by first implementing a low power D Flip-Flop. Then the Johnson counter will be designed by using this D Flip-Flop. Thus by applying clock gating and Lector technique the power consumed by the Johnson counter will be reduced. The proposed system is then contrasted with the traditional Johnson counter. Moreover, the delay is computed.

IV.CONCLUSION

Johnson counters are used in numerous application and also nowadays low power devices are preferred over the devices that consume more power. Hence it is necessary to reduce its power. This paper provides a quick overview of the numerous methods that researchers have employed to lower the power demands of Johnson counters. From all these techniques, clock gating and Lector Technique will be used to reduce the power dissipated by Johnson Counter.

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