A Review on Implementation Of Bus Encoding And Decoding Scheme

Rithesh V Shetty[1], Shreepad[2], Sumanth Shetty[3], Bablu[4], Bhakthi Shetty[5]

Student, Electronics & Communication Engineering, MITE, Moodabidri, India[1-4]

Assistant Professor, Electronics & Communication Engineering, MITE, Moodabidri, India[5]

Abstract: Power computation is crucial for evaluating and enhancing the energy efficiency of contemporary computer systems. Systems for bus encoding and decoding are becoming essential instruments for enhancing the accuracy and efficacy of power analysis. In order to improve the accuracy and efficiency of power analysis, this abstract offers a thorough review of bus encoding and decoding systems created especially for power calculations.

Bus encoding algorithms for power computation modify data before it is transported across the bus in order to lower communication power consumption. Utilising encoding techniques such bus inversion coding, transition minimising codes, or differential signalling, redundant or repetitive data patterns are detected and efficiently represented to reduce power swings and dynamic power consumption. These encoding methods reduce bus activity and signal modifications.

Keyword: CMOS, Bus Encoding & Decoding, Power Computation, Energy Efficiency.

I.   INTRODUCTION

Power dissipation and switching frequency reduction techniques do the same. One can directly change the switching frequency of a design by changing how the numbers are represented, the number of counts, how they are encoded, and how they are stored in a data format. Capacitive charging and discharging and short-circuit performance are directly affected by switching activity, which is minimized at the logic level using energy-optimized methods.The choice of logic encoding, data representation, and implementation of Boolean functions has a significant impact on the power consumption of digital circuits.

In the CMOS process, the bus accounts for a large proportion of chip power consumption and is the main source of dynamic power consumption of the entire system. Off-chip and on-chip global bus lines in VLSI (Very Large Scale Integration) circuits often have large capacitive loads. Reducing bus switching is a useful strategy for reducing bus power consumption because switching activity and power consumption are inversely related.Many encoding and decoding algorithms are available to reduce switching activity on the data bus. This includes basic techniques such as Bus Inversion (BI) and Bus Inversion Transition Signaling (BITS), which typically require additional bus lines.

The major objective of our research is to reduce power dissipation without introducing more bus lines while minimising switching activity on the bus. Especially for non-equiprobable input lines, by minimising the number of transitions by employing different techniques we can transfer the data through an efficient way. We can compare the power, area, and delay properties of different techniques and choose which one is efficient for the process.

Basic existing solution for low power data encoding and decoding schemes :

Basic digital system for low power data bus encoding and decoding schemes shown in figure 1. This basic digital system consists of encoder and decoder block in both source and destination side which are having bidirectional data lines.

In this system when source wants to send the data it will pass into encoder, encoder will encode the data so that reduce the number of switching activity. The encoded data passes through the data line and received by the decoder, which will decode received data to its original form. And we will receive the original data at the receiver side with much reduction in switching power.
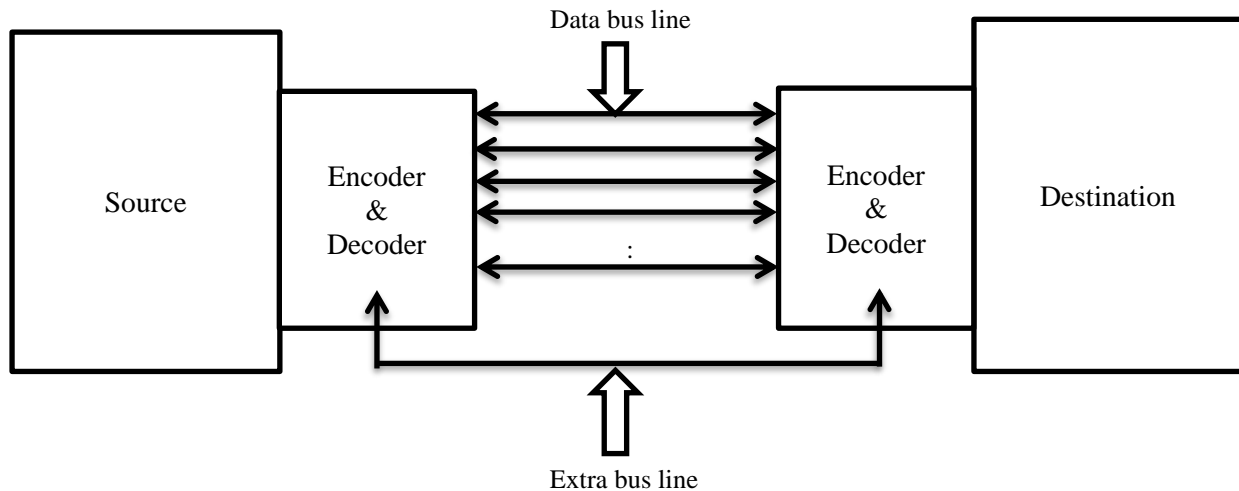
Fig.1. Basic system of data bus encoding and decoding

II.   LITERATURE REVIEW

[1] presents the Adaptive Bus Encoding (ABE) technique used in this study to provide a power-efficient encoder architecture for lowering transitions in off-chip buses. The ABE mechanism is suited for random and less sequential data streams since it functions without prior knowledge of incoming data streams. To avoid data loss during data recovery, the suggested solution makes use of spatial redundancy. For high-speed communication, the ABE framework reduces transitions in highly capacitive off-chip buses, which results in less power being wasted and better power efficiency. This method seeks to reduce the dynamic power consumption of the encoding circuitry, which will lead to effective data transfer on off-chip buses.

The author has introduced a coding technique in **[2]** that reduces power consumption in FFT (Fast Fourier Transform) structures by reducing switching activity. The technique involves sequentially creating conditionally coded blocks in the inputs of the FFT structure, converting them to low-switching activity blocks using the proposed method, and concatenating them in a sequential order to produce optimized output. The scheme is applied recursively after each concatenation to further improve efficiency. Experimental results show a significant reduction in switching activity, leading to 35% power savings for a 16-bit bus compared to 2's complement encoding. Hardware implementation used the Magma© tool .

[3]   Highlights the majority of the energy used in computer system buses is used to switch each line's voltage from high to low or vice versa. By lowering the average number of transitions between bus uses, bus encoding systems seek to increase energy efficiency. We offer new techniques for their implementation and deduce in closed form the performance of optimal and sub-optimal low-weight line codes created for this purpose. Then, we demonstrate that several low-complexity sub-optimal systems perform just slightly worse than optimal ones. For instance, by adding 8 lines to a 128 line bus, we can save 19.4% with appropriate inferior methods and 20.7% with the best scheme.

In **[4]** the growing interest in reversible logic is taken as a means to reduce power dissipation in low-power digital design. Reversible logic has diverse applications in advanced computing, CMOS design, optical information processing, DNA computing, bio-informatics, quantum computation, and nanotechnology. The paper proposes a Bus-Invert coding method on reversible logic using different gates such as Feynman, Feynman double gate, BJN, Sayem, and SCG gates. The proposed method lowers bus activity, resulting in a 50% reduction in I/O peak power dissipation and up to 25% reduction in I/O average power dissipation. The proposed circuits are simulated using Xilinx Isim simulator and implemented on Xilinx Spartan3 FPGA platform .

[5] Presents study on GPU implementations for Deflate coding, a popular lossless data compression technique, for both encoding and decoding. Deflate encoding and decoding are sequential, making parallel acceleration with GPUs difficult. The study offers the Single Kernel Soft Synchronization (SKSS) technique to optimise GPU processing resources, combined with the usage of several tiny hash tables for concurrent matching of subsequences in the dictionary by numerous threads. To speed up concurrent Huffman decoding, Huffman coding using gap arrays is also used. When compared to parallel/sequential Deflate encoding and decoding on Intel X86 multicore CPUs with several threads or a single thread, the GPU version of Deflate decoding delivers considerable speedups, according to performance evaluation on an NVIDIA A100 GPU, ranging from .

The study in **[6]** provides structures for big low-power cooling (LPC) codes, which are coding systems for managing state transitions in on-chip buses to mitigate joule heating and reduce power consumption. The (n, t, w)-LPC codes considered in this work prevent state transitions on the t hottest wires to regulate peak temperature and allow at most w state transitions in each transmission to reduce average power usage. With a focus on big codes, the study offers a number of LPC code designs that can be effectively encoded and decoded. The proposed constructions' encoding and decoding times are also examined.

In order to minimize the transition between data bits in interconnects and cut down on power loss from dynamic switching, this research in **[7]** introduces three unique data encoding techniques. The suggested approaches conduct half inversion or complete inversion on a single byte of data and estimate bit transitions in pairs of data bits, resulting in a 50% reduction in switching activity. The Verilog HDL models for the encoder and decoder for the schemes are put into an ASIC flow that targets 32 nm technology. With an overhead area of 210 cells and an encoding delay of 340 ps, the overall power dissipation of the encoding approach is 1.04 W. The suggested data encoding and decoding approaches are appropriate for low-power applications because the RTL code implementation requires a total area of 34980 units. In **[8]** In order to reduce power consumption caused by coupling effects in on-chip interconnects, this research suggests a bus encoding approach. The plan involves turning off the middle two data lines in each group of four bits, and it offers a way to reduce self-transitions and correlated switching inside the subsets. In comparison to the Bus-Invert approach for 4-bit data lines, experimental results demonstrate that the suggested strategy decreases self-transitions by 20%, increases the number of silent lines by 9%, and reduces power consumption by 46%. Bus encoding, crosstalk delay, coupling effect, and low power design are some related terms.

The decoding algorithm for a class of Reed-Muller (RM) subcodes based on the sum of smaller RM codes is presented in the paper **[9]** as being low-complexity and low-latency. The input sequence is organised as a multidimensional array, and smaller RM encoders are used for the encoding process. For smaller RM codes, decoding is carried out using a low-complexity decoder. The suggested approach works with upcoming low-rate communication scenarios' low-capacity channels. Hard decoding is outperformed by an effective soft-input soft-output (SISO) iterative decoding technique. For blocks of length n, complexity is $\mathcal{O}(n \log n)$ and delay is $\mathcal{O}(n \log n)$. lays up a broad framework for effective decoding of RM codes.

The distributed filtering problem based on encoding-decoding for time-varying saturation systems with constrained bit rate is addressed in the study of paper **[10]**. The digital channel's guidelines for bandwidth distribution are reflected in the limited bit rate model. To increase communication dependability, data signals are transmitted via the encoding-decoding technique at a restricted bit rate. The goal of the research is to recursively present an upper bound (UB) of the filtering error covariance (FEC) by solving matrix difference equations. The distributed filter design is based on measurements taken after the encoding-decoding process. By assuring the boundedness of the UB of the FEC and minimising the trace of the UB matrix, the distributed filter gain is parameterized. An example of a numerical simulation is given to show how well the suggested distributed filtering approach works.

III. SUMMARY

The collection of papers explores various encoding and decoding techniques in different domains, with a common emphasis on power efficiency, low complexity, and improved performance. The papers cover a range of topics including power-efficient encoding for buses, low-power FFT structures, energy-efficient bus encoding schemes, reversible logic-based encoding and decoding, GPU implementations of encoding and decoding algorithms, low-power cooling codes, reconfigurable data encoding schemes, low-complexity decoding methods, and encoding-decoding-based distributed filtering methods.

Some of the notable contributions include the design and implementation of a power-efficient encoder for transition reduction in off-chip buses, the introduction of low-power FFT structures using conditionally coded blocks, and the analysis and design of energy-efficient bus encoding schemes. Additionally, papers discuss the design and synthesis of bus invert encoding and decoding techniques using reversible logic, GPU implementations of deflate encoding and decoding algorithms, and low-power cooling codes with efficient encoding and decoding.

Other works focus on reconfigurable data encoding schemes for on-chip interconnect power reduction, low-complexity decoding of Reed-Muller subcodes, and encoding-decoding-based distributed filtering for time-varying saturated systems with constrained bit rate. Overall, the papers collectively contribute to the field of encoding and decoding techniques by proposing innovative solutions to improve power efficiency, reduce complexity, and enhance performance in various application domains.

IV.   CONCLUSION

In conclusion, the collection of papers highlights the significance of encoding and decoding techniques in achieving power efficiency, low complexity, and improved performance. The works propose innovative approaches such as adaptive bus encoding, low-power FFT structures, and energy-efficient schemes to minimize power consumption. They also address the need for low complexity by presenting techniques like reversible logic-based encoding and decoding. Additionally, the papers explore specific application domains such as data compression, on-chip interconnect power reduction, and distributed filtering. Overall, these contributions provide valuable insights and pave the way for further advancements in encoding and decoding methods for efficient and optimized data processing.

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