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Study of stacked high-k Gate-All-Around FET

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Abstract: In this paper, the characteristics of Gate-All-Around Field Effect Transistor (GAA FET) with stack high-k are studied by using the Silvaco Atlas simulations. By using of high dielectric constant material in the place of gate oxide reduces the leakage current and improve the Short Channels Effects (SCEs) like Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS). Gate dielectric material of HfO_2 along with SiO2 are used to analyze various electrical characteristics at 22nm GAA FET. The analysis included the ON current, threshold voltage, DIBL, SS, leakage current at 22nm gate length.

Keywords: Dielectric material, subthreshold slope, DIBL

I. INTRODUCTION

Moore's law has dictated that the transistor size must be shrunk in order to improve the electronics industry during the past few decades. Scaling of traditional Metal Oxide Field Effect Transistor (MOSFET) devices, however, is constrained by the lack of complete control over SCEs, tunneling of the gate insulator, and doping concentrations. Scaling MOSFETs is primarily caused by faster and denser packing [1-2]. Scaling has various undesirable effects that are more pronounced in traditional MOSFETs. They are surface scattering and mobility deterioration, avalanche breakdown, hot electron effect, DIBL, threshold voltage lowering, and punch through. Short channel effects are also known as negative effects. As devices get smaller, there are more SCEs with traditional MOSFETs. Researchers have proposed several of different MOSFET solutions for getting overcome these issues, including DG FinFET, Trigate, and Foregate. In the subthreshold region, DG FinFET integrated with a high-k gate dielectric is a promising device [3–4]. The goal of this work is to study the electrical characteristics of Gate-All-Around Field Effect Transistor (GAA FET) including threshold voltage, DIBL, SS, leakage current, mobility, and surface scattering at the 22nm GAA FET, with reference to high-k dielectric material. The semiconductor industry has been working to include high-k gate dielectrics into the double gate transistor production process in order to reduce leakage current and power consumption. In DG FinFET, gate dielectrics are utilized to stop current from passing through the gate. larger gate dielectric materials improve the electrical properties of the devices while also having low leakage current and larger drain current [5–6]. Furthermore, nanoscale devices prefer greater gate dielectric.

Investigated of electrical properties of the DG FinFET n-channel structure and their reactivity high-k materials of the gate with GaAs arsenide as channel substance [7]. Due high-k material in channel the device is enhance the ON currents and better electron mobility thereby device can improve performance and speed at low supply voltage. By reducing the dimensions of devices in order to follow Moore's law International Roadmap for Semiconductors (ITRS), enhance the performance and speed of FinFET at low power supply is possible by utilizing material of the channel other than silicon [8]. The performance of several high-k dielectric materialss as the oxide of the gate for a DG FinFET based on GaAs were investigated [9]. A comparison between DG FinFET and traditional MOSFET in terms of reduced leakage current was done at 60nm with various types of high-k dielectrics. The 60nm FinFET is designed for both high-k and low-k dielectrics. SiO_2 and HfO_2 are used in this situation as high-k and low-k materials, respectively [10]. To advance CMOS technology, which can enhance DGFinFET performance, new device materials are necessary. Various high-k dielectric materials as gate oxides in a SOI FinFET and the performance potential of gate dielectrics for Si-based DG FinFET, are investigated [11]. Electrical properties of nanoscale n-channel double gate FinFET structures and how they are influenced by the gate dielectrics used in the channel region, either of silicon, germanium, and polymorphs of silicon carbide. Investigate of nanoscale DG FinFET using silicon, germanium, or silicon carbide polymorphs as the channel material. Gate dielectrics, effects on electrical properties have been studied [12]. Due to its high transconductance (gm), increased threshold voltage (Vth), decreased DIBL and SS, and increased threshold voltage (Vth), high-k dielectrics demonstrate the best material and can restore other dielectric material.

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The scaling of the devices is made possible by the use of high gate dielectrics. By Consideration of all advantage of high-k dielectric material in DG FinFETs, the dielectric material of HfO_2 having high permittivity is taken and stacked with SiO_2 are implant in the GAA FET. In this work, investigates the electric properties of GAA FET with stack high-k.

II. DEVICE STRUCTURE

The two devices are designed using Slivaco TCAD in three dimensional. Device A represents GAA FET device, while the Proposed Device B incorporates a GAA FET with a stacked high-k dielectric, as illustrated in Figure 1

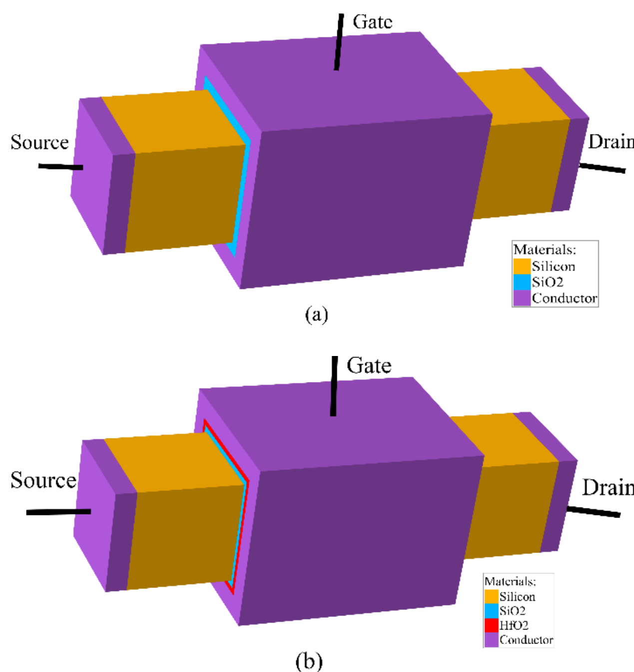

Fig. 1 a) GAA FET, b) GAA FET with stack high-k

The device A is GAA FET which is design by wrapping the SiO_2 on the channel and the gate metal is surrounded by the oxide layer. Device B is designed by replacing the SiO_2 layer in the device A with stack high-k. So here the insulating layer of SiO2 thickness is reduced to 0.5 nm and on top high-k material of HfO_2 is placed with thickness of 0.5 nm is used.

TABLE 1 DEVICE PARAMETERS

Parameter	values
Gate Length	22 nm
Thickness of oxide	1 nm
Length of Drain/Source	10 nm
Permittivity of HfO_2	25
Doping concentration of Drain/Source	1×10^{18} cm^{-3}
Doping concentration of Channel	1×10^{15} cm^{-3}

A direct metal contact on oxide layer is given with a work function of 4.6. High-k dielectric of HfO_2 along with SiO_2 is used as an oxide to control the I_{OFF} value. To effectively control the leakage current, a high-k dielectric material, specifically HfO_2 having high permittivity, is employed as the oxide layer. In order to facilitate a smooth interface between the silicon substrate and the oxide layer, SiO2 is utilized near the channel region. On top of SiO_2, the high-k of HfO_2 is placed to provide the better interfacing between the oxide layers. This hierarchical arrangement of oxide layers on a silicon substrate is known as stack high-k. Here SiO_2 provides the interface with the silicon substrate and HfO_2 in the insulating layer to optimize the device's performance and functionality.

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III. RESULT

The simulation results of two devices are discuss and comparing the electrical characteristics of both the devices. The physical thickness of high-k material is high so the threshold voltage is slightly increased in device B to form the channel that are shown in Fig. 2.

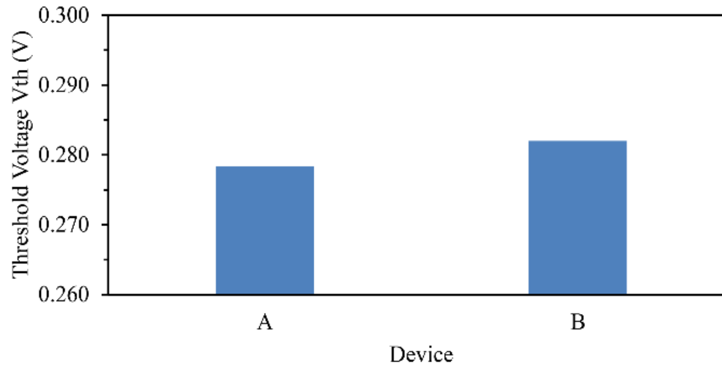

Fig. 2 Threshold voltage variation

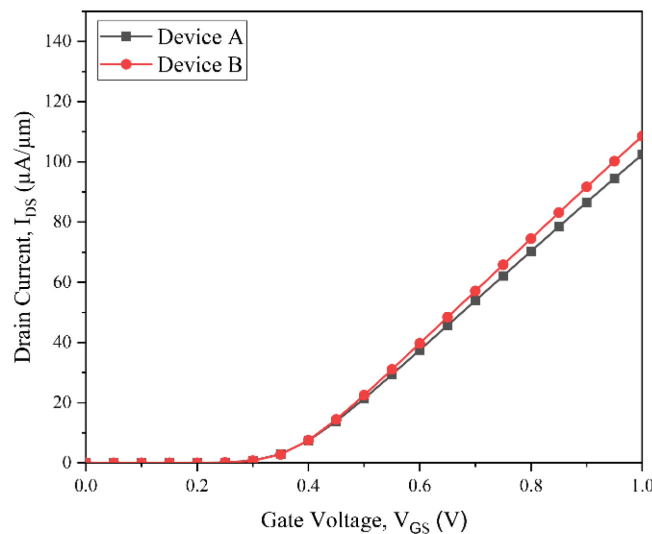

Fig. 3 Transfer characteristics

Fig. 3 shows the transfer characteristics of two devices are plotted on linear to observe the ON current. In this, using of high-k material of HfO_2 in oxide layer, in device B reduces the leakage current through the gate quantum tunneling which results in increases the ON current. In device B, the I_{ON} ~108 µA/µm which is higher than the device A.

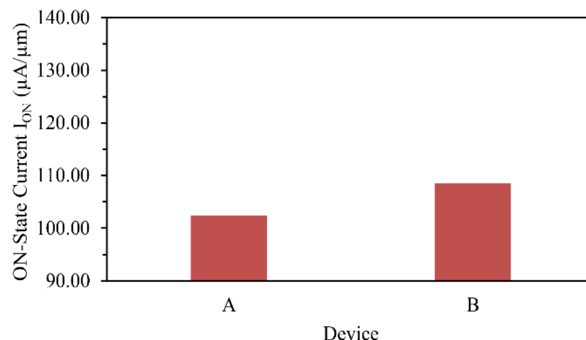

Fig. 4 Comparison of ON state current

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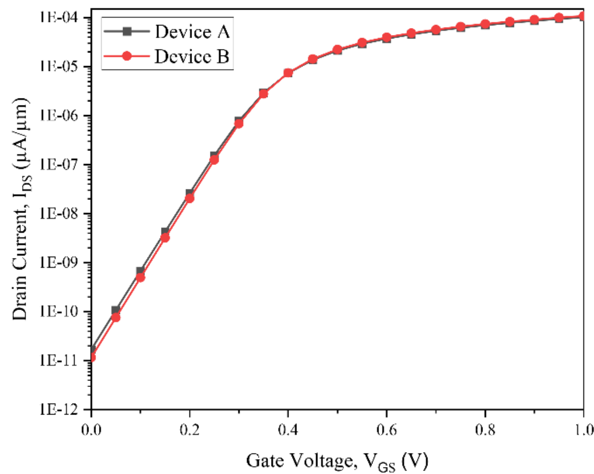

Fig. 5 Transfer characteristics on logarithm scale

Fig. 5 shows the transfer characteristics plotted on logarithm to find the leakage current that can be seen in log scale. In this, the subthreshold leakage is clearly observed that in device B, the leakage current is reduced by gate quantum tunnelling. Here the high-k material of HfO_2 have the high permittivity so the physical thickness is more which reduces the leakage current. Using of stack high-k reduces undesired current flow in the off state and enhancing Device B's efficiency. The leakage current in device B is approximately ~11.61 pA/µm.

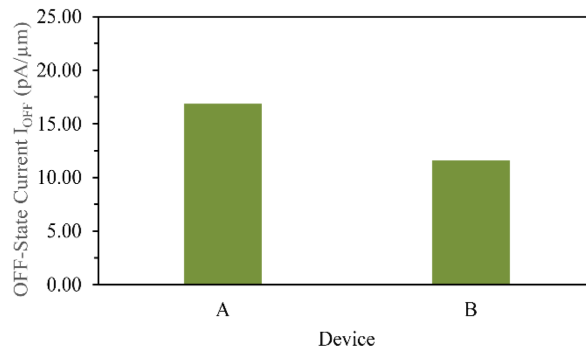

Fig. 6 Comparison of OFF state current (I_{OFF})

In device B, the I_{ON}/I_{OFF} ratio is very high as the ON current is high and leakage is less as compared to device A. The I_{ON}/I_{OFF} ratio in device B is nearly ~93.50×10^5 A which is very high. The subthreshold slope is providing the transition period between the OFF and ON of FET devices. Device B exhibits a lower subthreshold slope, indicating more control on leakage current. Here the leakage of device B is less so the subthreshold slope is also reduced. In device B, approximately ~61.25 mV/Dec of subthreshold slope is observed and it is almost reaching to ideal value.

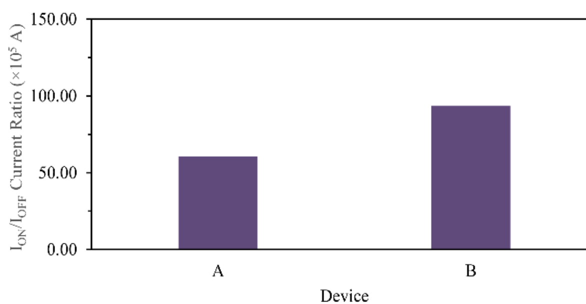

Fig. 7 Comparison of I_{ON}/I_{OFF} ratio

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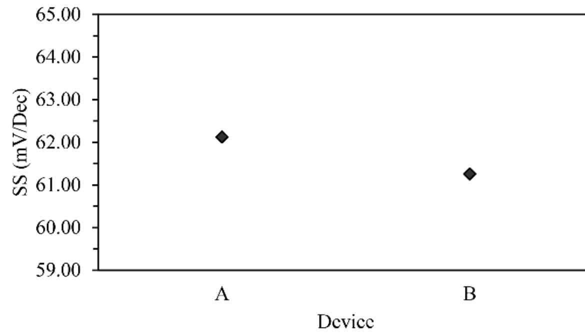

Fig. 8 Comparison of subthreshold slope

DIBL (Drain-Induced Barrier Lowering) is a phenomenon where the threshold voltage decreases as the applied drain voltage increases, leading to an increase in DIBL. Fig.9 is demonstrating that Device B exhibits a lower DIBL compared to Device A. This indicates that the reduction in threshold voltage with increasing drain voltage is less in Device B. The lower DIBL observed in Device B can be attributed to its higher threshold voltage, indicating that Device B experiences a smaller decrease in threshold voltage with increasing drain voltage. A DIBL of ~16.44 mV/V is observed in device B.

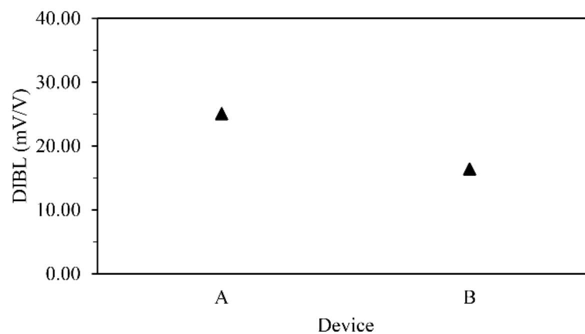

Fig. 9 Comparison of DIBL ratio

The output characteristics are plotted at $V_{gs} = 0.5$ V & $V_{gs} = 0.8$ V that are illustrated in Fig. 10. In device B, the drain current is higher than the device A. From the graph, it is evident that Device B exhibits a higher current flow compared to Device A at both voltage levels. This higher current flow in Device B can be attributed to the utilization of stack high-k, which effectively reduces leakage current. The implementation of HfO_2 leads to improved current performance and efficiency, resulting in a higher flow of current in Device B compared to Device A.

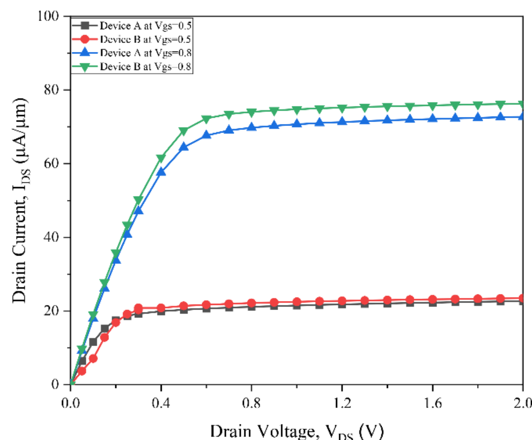

Fig. 10 Output characteristics

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IV. CONCLUSION

In this paper, the electrical characteristics of GAA FET structure have been studied and analyzed by applying gate dielectric materials of HfO_2 with permittivity of 25. HfO_2 as gate dielectric material along with SiO2 is used for proper interfacing and minimize the leakage current through gate quantum tunnelling. Using of stack high-k, enhancement in threshold voltage, and reduced short channel effects such as SS and DIBL. HfO_2 exhibits reduction of leakage current, SS, DIBL and mobility of channel and increase in the threshold voltage. HfO_2 improved device performance, better control of gate over the channel, reduction of the effective leakage current and offer high amplification values. Using of a high-k dielectric material in Device B, offering potential benefits and performance enhancements over the SiO_2-based insulating layer used in Device A.

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