IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.102 ⁘ Peer-reviewed & Refereed journal ⁘ Vol. 13, Issue 4, April 2024

DOI: 10.17148/IJARCCE.2024.13401

Design and Implementation of a Digital Matched Filter for Square Pulses Signals using FPGA

Dr. Kamal Aboutabikh[1], Dr. Amer Garib[2]

Faculty of Informatics Engineering, Ittihad Private University, Damascus Syria.[1,2]

aboutabikh59@gmail.com

Abstract: In this paper, we discuss a practical mechanism of digital matched filtering which maximizes of output SNR for square, triangular , Gaussian pulse signals and other pulse signals in presence of additive white Gaussian noise (AWGN) by using a digital matched filter (DMF) corresponding to time domain convolution algorithm of input and reference signals using Cyclone II EP2C70F896C6 FPGA from ALTERA placed on education and development board DE2-70 with the following parameters: sampling frequency $F_{sam} = 50MHz$, pulse width $\tau_S = 6\mu s$, pulse period $T = 12\mu s$, samples number (length of reference signal) is 300, the ratios of signal to the noise at the input of the filter is $SNR_{INP} = 1/1, 1/2, 1/3, 1/8$, processing gain factor is 25dB.

The results of filter operation are evaluated using a digital oscilloscope to display the input and output signals for different SNR_{INP}.

Keywords: DMF , Square Pulse , DPNG , DDFS , FPGA.

I. INTRODUCTION

Digital matched filtering is widely used to process radio pulse, square pulse, LFM pulse, BPCM signals in modern radars, modern communications GSM, GPS receivers, and others, so the filter which realizing the digital matched filtering algorithm considers the basic and important element in the receiver. This filter defines the basic features for the receiver such that, signal extracting capability from noise, receiver sensitivity, jamming resistance [1].

Nowadays, different digital processing algorithms are used, such that digital convolution algorithm in time domain, and digital convolution algorithm in frequency domain [2].

Complex digital convolution algorithm between input and reference signals considers the most rapid and practical one, and operates in real time, so we will introduce the mathematical model for this algorithm [3].

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

-Using the digital matched filtering for square pulses signal on the background of additive white Gaussian noise effect.

-Using modern digital techniques to design the digital matched filter which allow getting on the desired processing gain factor under effect of interference and additive white Gaussian noise signals.

-Using parallel digital convolution algorithms which makes the processing operation within the real time.

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the DMF for square pulses signal on the background of additive white Gaussian noise, the following tools and software are used:

-Cyclone II EP2C70F896C6 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE2-70 [4].

-DDFS which is considered as highly accuracy techniques in square pulses signal synthesizing and DPNG to synthesize white noise and they were designed on FPGA chips.

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.102 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 13, Issue 4, April 2024

DOI: 10.17148/IJARCCE.2024.13401

-Digital FIR filters of Highly accuracy specifications in filtering and stability and linear phase response.

-VHDL programming language with Quartus II 9.1 design environment.

-MATLAB11 programming environment for digital filter designing and filter coefficients computing.

-GDS-1052 digital oscilloscope with Free Wave program to take the results.

-PC computer for designing and injecting the design in the chip.

IV. DIGITAL CONVOLUTION ALGORITHM IN TIME DOMAIN FOR DMF

Fig. 1 shows the analog square pulses signal according, the width of these pulses is τ_S and the period is T, this signal is given by the following relation [5]:

$$S(t)=\begin{Bmatrix}1 & for & 0\le t\le \tau_S \\ 0 & for\ another\, t & \end{Bmatrix} \quad (1)$$

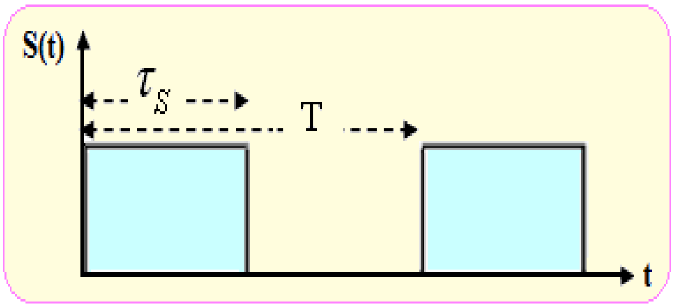

Fig. 1: Square pulses signal

The square pulses are synthesized by DDFS according to the Fig. 2 using a digital accumulator and clock pulses of frequency 50MHz. the frequency code which accept $T=12\mu s$ is computed according to the following relation [6]:

$$F_{SQ}=\frac{1}{T}=\frac{F_{CLK}.L_{SQ}}{2^n} \quad (2)$$

Where:

n: the number of phase accumulator bits (n=32 bits), F_{CLK}: clock pulses frequency (F_{CLK}=50MHz), L_{SQ}: frequency code according to F_{SQ}, T: square pulses period where: $T=12\mu s,\ F_{SQ}=1/T=83.333KHz$, Then:

$$L_{SQ}=\frac{2^n}{F_{CLK}*T}=\frac{2^{32}}{50*10^3*12*10^{-3}}=7158278$$

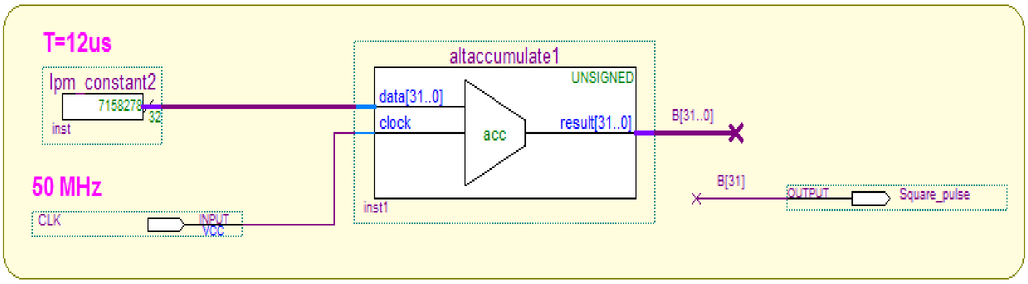

Fig. 2: Square pulses signal diagram using Quartus II 9.1

ISSN (O) 2278-1021, ISSN (P) 2319-5940
International Journal of Advanced Research in Computer and Communication Engineering
Impact Factor 8.102 ⁙ Peer-reviewed & Refereed journal ⁙ Vol. 13, Issue 4, April 2024
DOI: 10.17148/IJARCCE.2024.13401

The digital matched filter order for square pulses signal is defined by the taken samples number within the pulse width according to the following relations [7]:

$$M = \frac{\tau_S}{T_{sam}} = \frac{T/2}{T_{sam}} = \frac{T}{2.T_{sam}} \qquad (3)$$

So, the filter order N equals to:

$$M = \frac{\tau_S}{T_{sam}} = \frac{T/2}{T_{sam}} = \frac{T}{2.T_{sam}} = \frac{12}{2*20*10^{-3}} = 300$$

Where:

M: samples number (filter delay stages), so the filter order N is given by the following relation:

$$N=M-1 \qquad (4)$$

The square pulse of width (τ_S) is replaced by the digital samples number M using the sample pulses of period T_{sam} according to the diagram shown in Fig. 3.

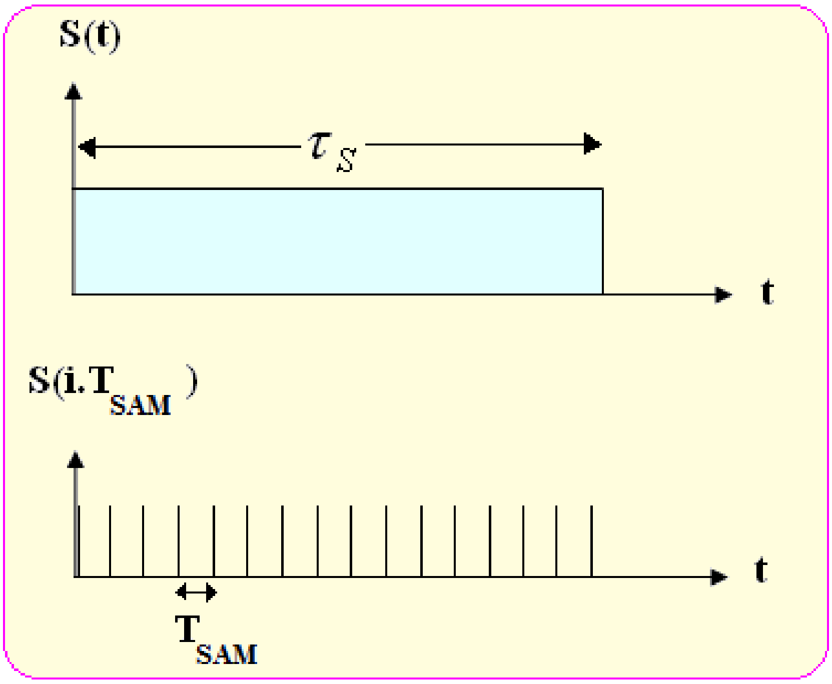

Fig. 3: The filter order identify

The response of filter can be represented according to convolution function in time domain by the following relation [8]:

$$Y(n) = \sum_{m=0}^{M-1} \{S(n-m).H(m)\} \qquad (5)$$

Fig. 4 shows the digital convolution algorithm diagram between the input signal and the reference signal of M length.

ISSN (O) 2278-1021, ISSN (P) 2319-5940
International Journal of Advanced Research in Computer and Communication Engineering
Impact Factor 8.102 ⁘ Peer-reviewed & Refereed journal ⁘ Vol. 13, Issue 4, April 2024
DOI: 10.17148/IJARCCE.2024.13401

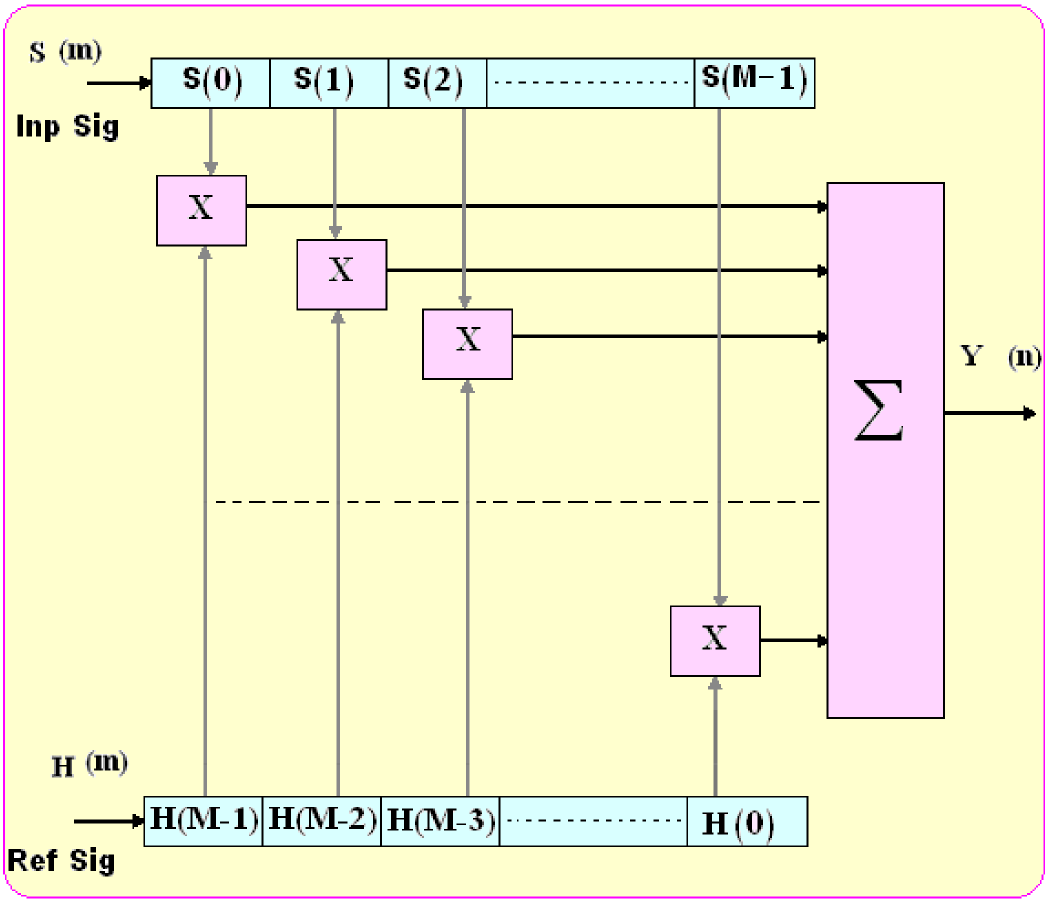

Fig. 4: Time convolution algorithm $Y(n)$ for input and reference signals with length M

Fig. 5 shows the studied diagram of DMF for a digital convolution algorithm $Y(n)$ [9]. It consists of:

-Direct digital frequency synthesizer (DDFS) to create the square pulses signal with required specifications .

-Digital pseudo-noise generator (DPNG) to synthesize additive white Gaussian noise signal [10].

-DMF with digital convolution algorithm in time domain.

-DAC of 8-bits to transform the signal samples from digital to analog form for input and output signals of the digital matched filter.

-PC to link DE2-70 through USB port to inject the design in Cyclone II EP2C70F896C6 FPGA chip [4].

-Digital oscilloscope GDS-1052U with USB port for taking the input and output signal Fig.6 of DMF in time domain for different cases of SNR_{INP}. This research is carried out for the square pulses signal and DMF of the following specifications.

V. THE SQUARE PULSES SIGNAL SPECIFICATIONS

-Processing is done at video frequency.

-Signal type is square pulses.

-Modulation type is without modulation.

-Sampling frequency is: $F_{sam} = 50MHz, T_{sam} = 0.02\mu s$.

International Journal of Advanced Research in Computer and Communication Engineering
Impact Factor 8.102 ⁙ Peer-reviewed & Refereed journal ⁙ Vol. 13, Issue 4, April 2024
DOI: 10.17148/IJARCCE.2024.13401

-Pulse width is $\tau_S = 6\ \mu s$.

-Pulse period is $T = 12\,\mu s$.

-Samples number (reference signal length): $M = \tau_S / T_{sam} = 6/0.02 = 300$.

-The single delay step: $\delta\tau = T_{sam} = 20ns$.

- $SNR_{INP} = 1/1, 1/2, 1/3, 1/8$

VI. DMF SPECIFICATIONS

-The length of processing word for the input signal is signed 8-bits.

-The used digital multipliers number is 300 with 9x9 bits.

-The shift registers number is 2*300 SR with 8-bits according to the Fig. 6.

-Adder has 300 inputs with 16-bits, and one output with 27-bits.

-Different logic and mathematic operations (AND, NOT, XOR, etc).

-The capacity of used memory is 10 KB.

-DMF order is N=M-1=300-1=299.

-Input data flow speed 8bit every 20ns:

8x50x1000000/(8x1024x1024)=48 MBPRS

-Processing speed is 300 multiplying, adding, shifting and conversion operations through 20ns which equal (15) billion operations per second by using parallel processing (adding, shifting, multiplying, and dividing 300 digital samples with 8-bits length through one period for sampling pulses, that is, 20ns), this equivalent to 15 GHz processor clock frequency, so the processing is done simultaneously on-line.

-Processing gain on the filter output is [7]:

$$K_{MF} = \frac{SNR_{OUT}}{SNR_{INP}} = 10\log(M) \qquad (6)$$

Then:

$$K_{MF} = SNR_{OUT} / SNR_{INP} = M \Rightarrow$$
$$K_{MF}(dB) = 10\log M = 10\log 300 = 25dB$$

Fig. 6 shows a digital convolution algorithm with M=300 in case of constant parameters signal (frequency), so the sample values of the reference signal are recorded for once time in shift registers H(0)….H(299) during the pulse width by Single M signal, the input signal samples are recorded for once time in symmetric form with the input signal, then the time convolution is computed between the two signals every sample pulse .

There is a possibility to develop this algorithm through serial connection for several algorithms in order to get high filter order and processing gain factor up to 36dB.

International Journal of Advanced Research in Computer and Communication Engineering
Impact Factor 8.102 ⁒ Peer-reviewed & Refereed journal ⁒ Vol. 13, Issue 4, April 2024
DOI: 10.17148/IJARCCE.2024.13401

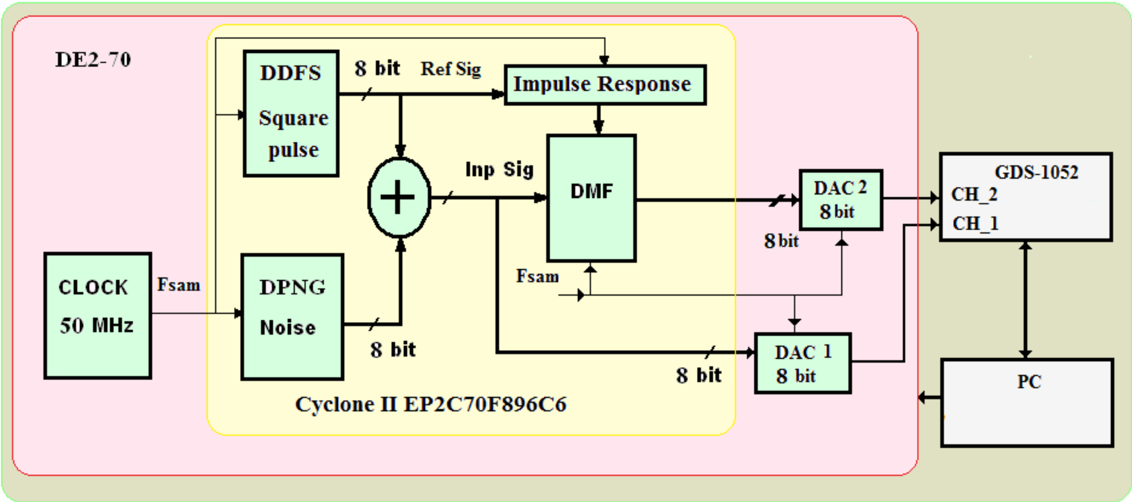

Fig. 5: The research and studying diagram for DMF

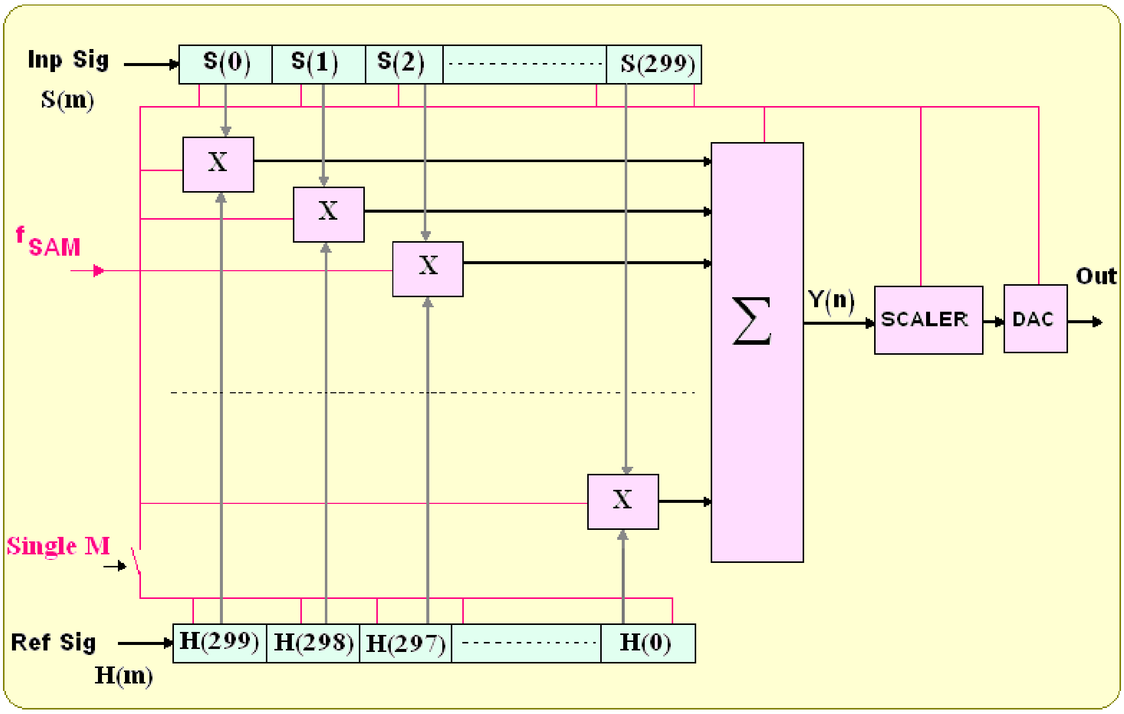

Fig. 6: digital convolution algorithm for DMF in time domain of length M=300

VII. THE ALGORITHM OF NOISE INTERFERENCE SIGNAL GENERATION(DPNG)

This signal is of white noise type and has amplitude equals to 100% ,200% ,300% ,800% from the square pulse signal amplitude and exists within the filter pass bands and is considered as the fifth interference signal.

To generate the white noise signal, a digital pseudo noise generator DPNG is used, which consists of a shift register of k=60 bits and clock pulses of frequency equals to sampling frequency of 50MHz with maximum periodic time (T_{DPNG}) for the generated series [10]:

$$T_{DPNG} = (2^k - 1) * T_{sam} \qquad (7)$$

 ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.102 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 13, Issue 4, April 2024

DOI: 10.17148/IJARCCE.2024.13401

$$\text{For } k = 60, T_{sam} = 0.02\mu s \quad \Rightarrow$$
$$T_{DPNG} = (2^{60} - 1) * 0.02 * 10^{-6} = 2.3 * 10^{10} s$$

Or:

$$T_{DPNG} = 2.3 * 10^{10} / (3600 * 24 * 365) = 731.2\, Year$$

Where k the number of shift register bits.

According to the diagram shown in Fig. 7, which consists of the following parts:

-Shift register of 60 bits and clock pulses with sampling frequency of 50MHz.

-Feedback circuit by using XOR gate and NOT gate.

The Fig. 8 shows the formed noise signal.

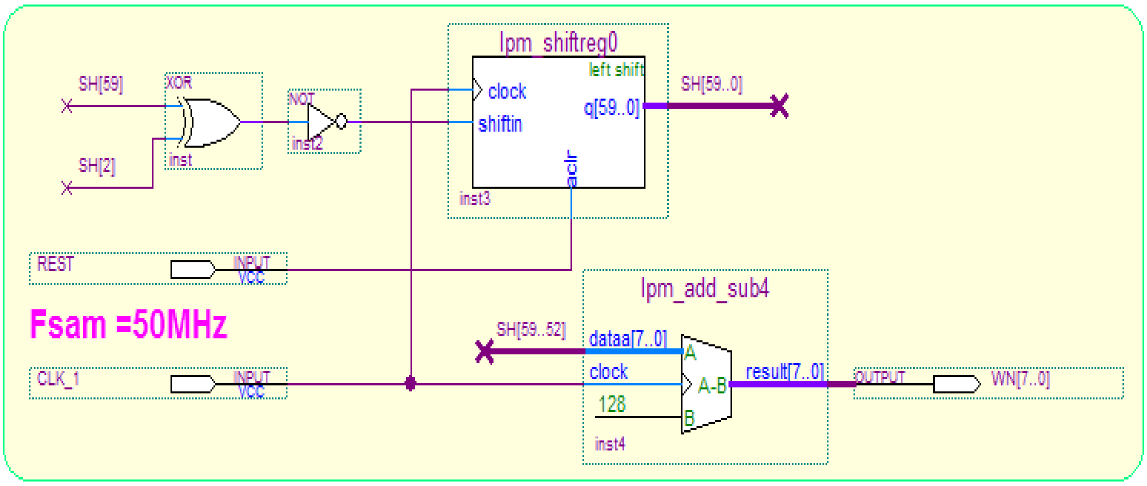

Fig. 7 The digital pseudo noise generator (DPNG) diagram

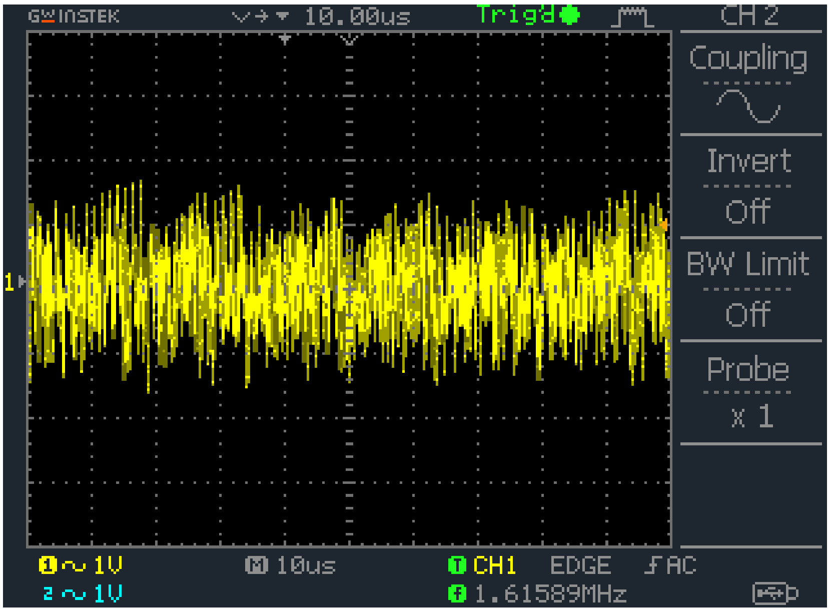

Fig. 8 The white noise signal of F_{sam}=50MHz on the oscilloscope screen

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.102 ⪤ Peer-reviewed & Refereed journal ⪤ Vol. 13, Issue 4, April 2024

DOI: 10.17148/IJARCCE.2024.13401

VIII. PRACTICAL RESULTS

The practical design results in time domain for input and output signals of the DMF were taken by digital oscilloscope of type GDS-1052U.

Fig. 9 shows on the channel1 of the oscilloscope the square pulses signal without noise effect on the DMF input and on the channel2,the same signal is shown but on the output of the filter. From this Fig.7 we note that the pulse width on the output of the filter is twice increased considering that the designed filter is definitely specialized to this signal.

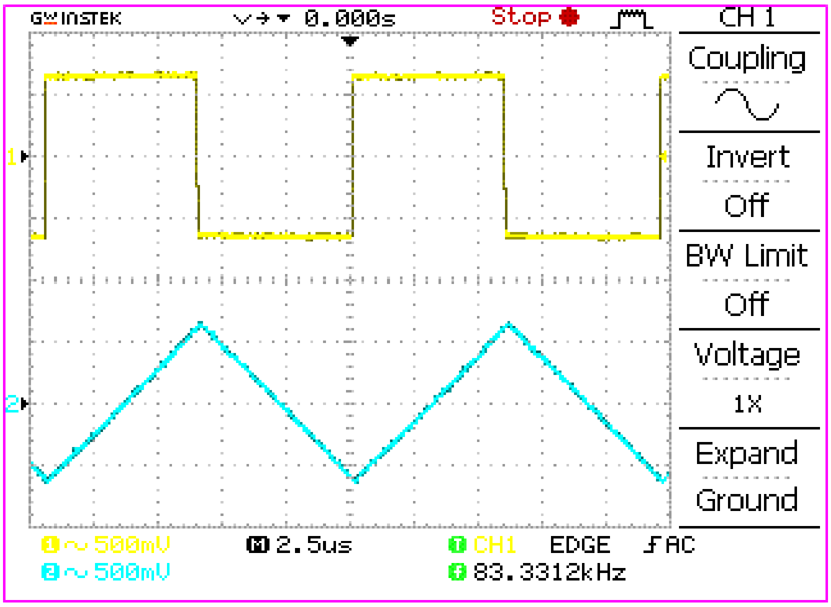

Fig. 9: The input and output signals of the DMF without noise case

Fig. 10 shows on the channel1 of the oscilloscope the square pulses signal under effect of noise of SNR_{INP}=1/1, which applied on the DMF input and on the channel2, the same signal is shown but on the DMF output. We note from this Fig.8 , that the signal was extracted on the filter output concerning that the filter is designed for this signal, and it may possible to filter the signal with level less than the previous case, because of AWGN existence with SNR_{INP}=1/1.

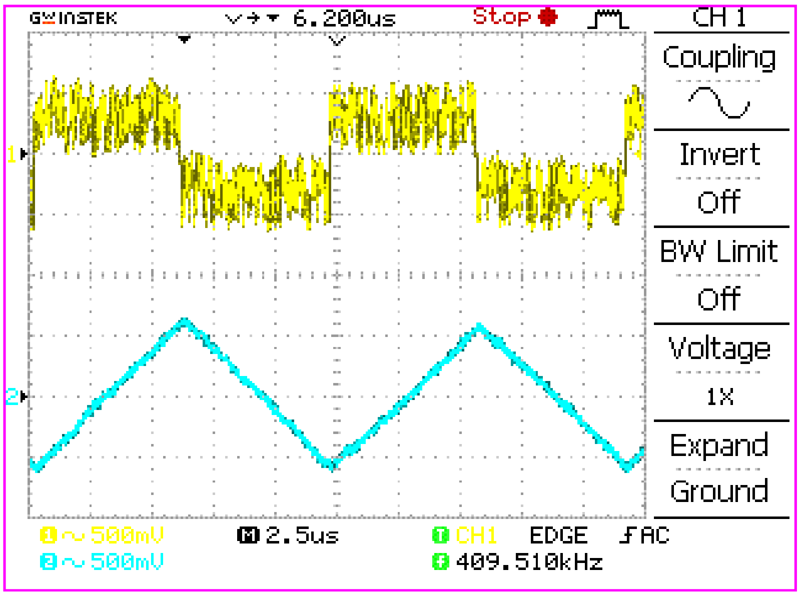

Fig. 10: The input and output signals of the DMF in case of SNR_{INP}=1/1

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.102 ⁚ Peer-reviewed & Refereed journal ⁚ Vol. 13, Issue 4, April 2024

DOI: 10.17148/IJARCCE.2024.13401

Fig. 11 shows on the channel1 of the oscilloscope the square pulses signal under effect of noise of SNR $_{INP}$=1/2, which applied on the DMF input and on the channel2, the same signal is shown but on the DMF output. We note from this Fig.11 , that the signal was extracted on the filter output concerning that the filter is designed for this signal, and it may possible to filter the signal with level less than the previous case, because of AWGN existence with SNR_{INP}=1/2.

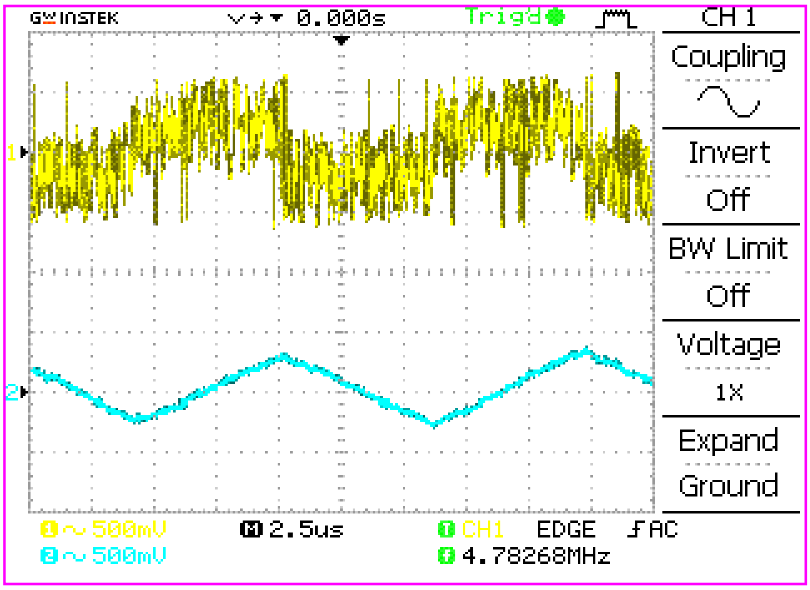

Fig. 11: The input and output signals of the DMF in case of SNR_{INP}=1/2

Fig. 12 shows on the channel1 of the oscilloscope the square pulses signal under effect of noise of SNR $_{INP}$=1/3, which applied on the DMF input and on the channel2, the same signal is shown but on the DMF output. We note from this Fig.12 , that the signal was extracted on the filter output concerning that the filter is designed for this signal, and it may possible to filter the signal with level less than the previous case, because of AWGN existence with SNR_{INP}=1/3.

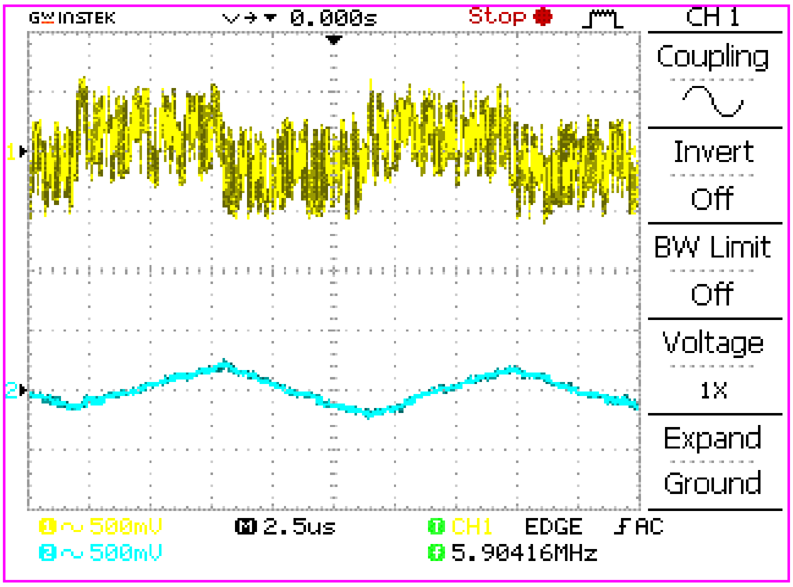

Fig. 12: The input and output signals of the DMF in case of SNR_{INP}=1/3

Fig. 13 shows on the channel1 of the oscilloscope the square pulses signal under effect of noise of SNR $_{INP}$=1/8, which applied on the DMF input and on the channel2, the same signal is shown but on the DMF output. We note from this Fig.13 , that the signal was extracted on the filter output concerning that the filter is designed for this signal, and it may possible to filter the signal with level less than the previous case, because of AWGN existence with SNR_{INP}=1/8.

International Journal of Advanced Research in Computer and Communication Engineering
Impact Factor 8.102 ⋇ Peer-reviewed & Refereed journal ⋇ Vol. 13, Issue 4, April 2024
DOI: 10.17148/IJARCCE.2024.13401

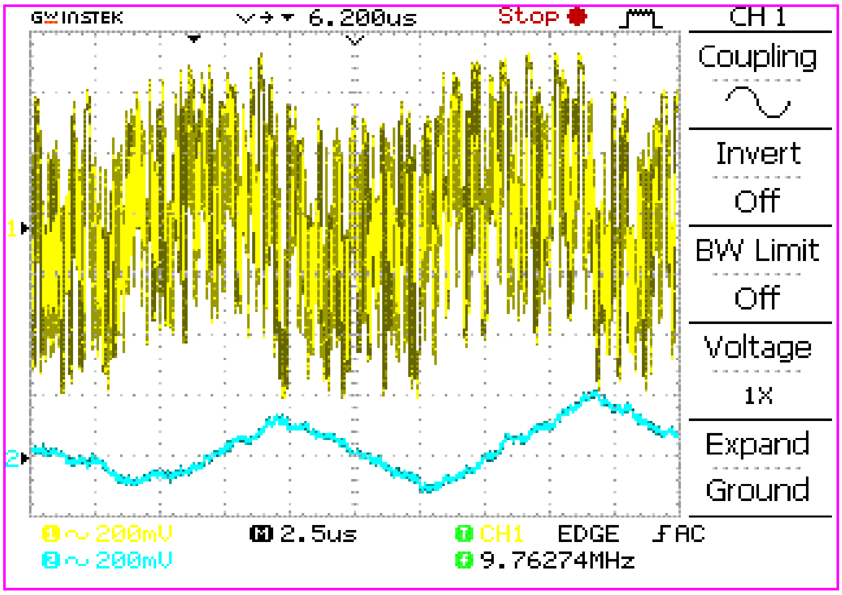

Fig. 13: The input and output signals of the DMF in case of SNR_{INP}=1/8

IX. CONCLUSIONS

-The using of modern digital techniques of kind FPGA permit of design digital matched filters by digital convolution algorithms between input signal and the pulse response of the filter to obtain the required specifications with required processing gain, these techniques have high accuracy in design and performance speed (until to 250MHz),and the high integrated level (hundred thousands of digital integrated functions within one digital chip FPGA).

-FPGA techniques permit of developing DMF algorithm through serial connection of some algorithms of 300 order or more in input and output to obtain a big signal base and processing gain reach until 36 dB, this makes the square pulses have a high effectiveness by noise and jamming existence.

-From practical results which obtained, we note the possibility of receiving and processing a signal in cases of SNR_{INP}=1/8 << 1, and this means that the signal on the filter input is not seen at all, but on the filter output, the signal is so clear because of digital matched filtering operation which achieve a matched processing gain proportional to samples number:

$$K_{MF}(dB) = 10\log M$$

-By increasing (M) it may be increase the processing gain and extract the signal under worse conditions than SNR<1/8.

-Changing the square pulse specifications, the DMF specifications will be change, so every square pulse has a special DMF. To make the filter structure (algorithm) constant when the square pulses specifications change, the ratio between the pulse width and the sample pulses period should be constant, this means [7]:

$$M = \tau_S / T_{sam} = const \qquad (8)$$

That is, for the designed filter where $T_{sam} = 0.02\mu s$, $\tau_S = 6\mu s$, so : $M = \tau_S / T_{sam} = 6/0.02 = 300$

For $F_{sam} = 60MHz$, the pulse width must be $\tau_S = 300x(1/60) = 5\mu s$.

For $F_{sam} = 50MHz$, the pulse width must be $\tau_S = 300x(1/50) = 6\mu s$.

For $F_{sam} = 30MHz$, the pulse width must be $\tau_S = 300x(1/30) = 10\mu s$.

$$\boxed{M = \tau_S / T_{sam} = \tau_S . F_{sam} = \text{constant} = 300}$$

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.102 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 13, Issue 4, April 2024

DOI: 10.17148/IJARCCE.2024.13401

$F_{sam}[MHz]$	10	20	25	30	50	60
$T_{sam}[\mu s]$	0.1	0.05	0.04	0.033	0.02	0.016
$\tau_S[\mu s]$	30	15	12	10	6	5
$T[\mu s]$	60	30	24	20	12	10
DMF	The same filter					
Filter coefficients	Variable					

-This algorithm of digital matched filtering successfully works whatever the type of impulses (square , triangular , Gaussian ,...., etc).

REFERENCES

[1]. C. S.Rawat, Deepak Balwani , Dipti Bedarkar , Jeetan Lotwani, Harpreet Kaur Saini , Implementation of Barker Code and Linear Frequency Modulation Pulse Compression Techniques in Matlab International Journal of Emerging Technology and Advanced Engineering, Volume 4, Issue 4, April 2014(105-111).

[2]. Zoran Golubi cic, Slobodan Simic c , Aleksa J. Zejak , Design and FPGA implementation of digital pulse compression for band-pass Radar signals, Journal of Electrical Engineering, VOL. 64, NO. 3, 2013, 191–195.

[3]. Introduction to matched filters John C. Bancroft CREWES Research Report . Volume 14 (2002).

[4]. www.altera.com.

[5]. „Radartutorial“ (www.radartutorial.eu)

[6]. GOLDBERG B. 1999- Digital Frequency Synthesis Demystified, LLH Technology Publishing, united states, 334.

[7]. K. Aboutabikh , M B.abiker Idris , I. Haidar, Digital matched filtering for radio pulse signals in the presence of additive white Gaussian noise using FPGA,International Journal of Technical Research and Applications ,Volume 3, Issue-5 (September-October 2015), PP. 127-132.

[8]. Steve Winder .2002-Analog and Digital Filter Design ,second edition , Elsevier Science (USA),450.

[9]. K. Aboutabikh , N. Aboukerdah , Design and implementation of a multiband digital filter using FPGA to extract the ECG signal in the presence of different interference signals /Computers in Biology and Medicine Journal/ Vol 62 (July 2015) 1-13.

[10]. Afaq Ahmad, Sayyid Samir Al-Busaidi and Mufeed Juma Al-Musharafi. On Properties of PN Sequences Generated by LFSR – a Generalized Study and Simulation Modeling. Indian Journal of Science and Technology-2013.

BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR, university of communication in Leningrad, holds a degree assistant professor in 2009 from Aleppo university.

Lecturer at Department of Biomedical Engineering, Al Andalus University For Medical Sciences-Syria, Tishreen University-Syria, Corduba Private University- Syria, Kassala University-Sudan and Ittihad Private University- Syria.

Publish a lot of research in the field of digital communication and digital signal processing in the universities of Syria and in the European and Indian journals. Working in the field of programming FPGA by using VHDL and design of Digital Filters.

Dr Amer Garib holds a PhD in communication engineering in 1994 from the USSR, university of communication in Leningrad. Lecturer at Department of Faculty of Informatics Engineering , Ittihad Private University- Syria.

Publish a lot of research in the field of digital communication in the universities of Syria and in the Indian journals.

Working in the field of Digital Communication Systems and design of Antenna Systems

