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Design and implementation of Frequency Hopping Spread Spectrum (FHSS) system using FPGA

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Abstract: Frequency hopping techniques are used in CDMA communication systems, where several hopping frequencies are allocated for each user within a specific frequency range for all users. The number of frequencies within a certain frequency range is fixed so that the interference noise is reduced.The frequency hopping algorithm for these frequencies varies from one user to another. In this paper, we propose a practical method for a frequency hopping system using a programmable hopping algorithm stored in ROM for the case of slow FHSS and fast FHSS, and for three users and eight frequencies , this system is designed using a cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 with the following parameters:
-Clock frequency: F_{CLK}=50MHz
-Modulation type of signal is : 2FSK.
-Frequency range: (0.011 Hz…10 MHz).
-Frequency Resolution: (0.011 Hz).
-Signal amplitude (5V).
-Controlled parameters: values of hopping frequency, number of hopping frequencies, type of FHSS .
-Update capability: changing hopping frequency algorithm, changing modulation type: BPSK, MFSK, increase frequency range up to 20MHz , changing data frequency and hopping frequency.

Keywords: FHSS, CDMA , FSK, FPGA, DDFS, SFHSS, FFHSS.

I. INTRODUCTION

The principle of spreading spectrum using FHSS can be explained according to the diagram shown in figure (1) for three users and eight frequencies (F_1,F_2, F_3, F_4, F_5, F_6, F_7, F_8) .

At moment (T_1) , the first user works on frequency (F_2) , the second user works on frequency (F_5), and the third user works on frequency (F_7).

At moment (T_2) , the first user works on frequency (F_1) , the second user works on frequency (F_2) , and the third user works on frequency (F_4).

At moment (T_3) , the first user works on frequency (F_5) , the second user works on frequency (F_7) , and the third user works on frequency (F_8).

At moment (T_4), the first user works on frequency (F_1) , the second user works on frequency (F_3) , and the third user works on frequency (F_6) ,… etc , where each symbol (or several symbols) of the data signal is transmitted for every user according to a deferent frequency from the other users at the transmitting side.

Frequency hopping is achieved in two ways: slow FHSS and fast FHSS.
-Slow frequency hopping spread spectrum (SFHSS) - one or more data symbols are transmitted in the time interval between frequency hops [1] , in this case:
-For slow FHSS :

$$T_{H\ SLOW} >> T_S \Rightarrow T_{H\ SLOW} / T_S >> 1 \qquad (1)$$

Where:
$T_{H\ SLOW}$: hopping period for slow FHSS ,T_S :symbol duration.

$$\text{For } (F_{H\ SLOW} = 1\,\text{Hz} \Rightarrow T_{H\ SLOW} = 1\text{sec}\ , T_S = 0.25\text{sec}) \Rightarrow T_{H\ SLOW} / T_S = 1/0.25 = 4$$

-Fast frequency hopping spread spectrum (FFHSS) – more than one frequency hop during each transmitted symbol [1] , in this case:

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-For fast FHSS :

$$T_{H\ FAST} << T_S \Rightarrow T_{H\ FAST} / T_S << 1 \qquad (2)$$

Where:
$T_{H\,FAST}$: hopping period for fast FHSS ,T_S :symbol duration.

$$\text{For } (F_{H\ FAST} = 16Hz \Rightarrow T_{H\ FAST} = 0.0625\text{sec}, T_S = 0.25\text{sec}) \Rightarrow T_{H\ FAST}/T_S = 0.0625/0.25 = 0.25$$

In reference [2] , the FHSS is designed for one user and BPSK modulation and eight frequencies , while in this research we have tree users , eight frequencies and 2FSK,4FSK , BPSK modulation and capability of changing the hopping algorithm.

In reference [3] , the FHSS is designed for one user and fast FHSS only ,while in this research we have tree users , eight frequencies and 2FSK,4FSK , BPSK modulation and capability of changing the hopping frequency algorithm.

In reference [4] , the FHSS is designed for one user and BPSK modulation and eight frequencies , while in this research we have tree users , eight frequencies and 2FSK,4FSK , BPSK modulation and capability of changing hopping frequency algorithm.

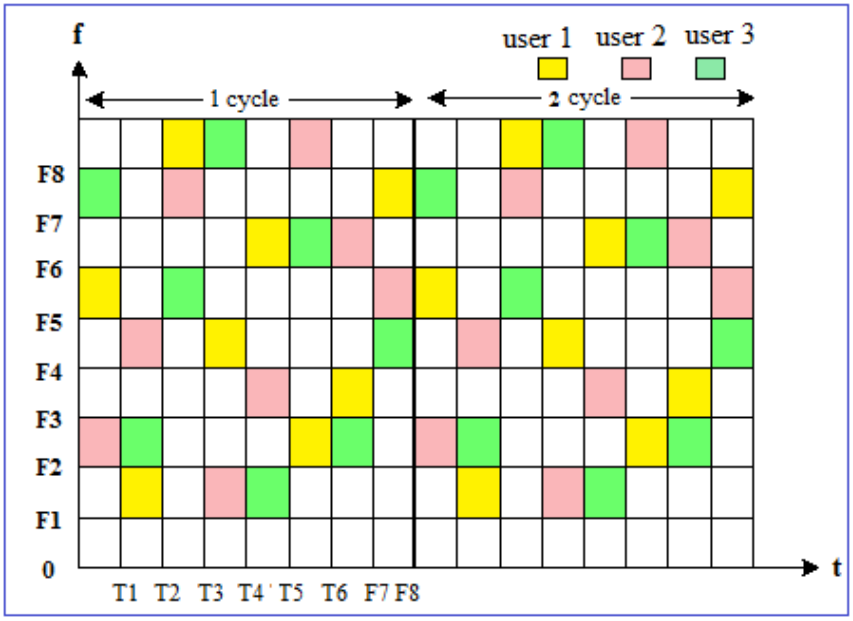

Figure (1) principle of spreading the spectrum using FHSS for three users and eight frequencies.

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

- The design and implementation of a frequency hopping spread spectrum (FHSS) system using an FPGA was achieved considering high accuracy in the design process, high speed of performance, and appropriate technological resources for the number of three users and eight frequencies, where each user has his own hopping algorithm with the ability of changing the hopping type (slow or fast).

-Using the digital DDFS with digital 2FSK modulation , digital square generator of data ,digital hopping impulse generator , it makes the FHSS design process flexible, accurate and highly efficient.

-Changing hopping frequency within different values explains the difference between SFHSS systems and FFHSS systems, this factor determines the number of users in the communications system and thus the effectiveness of this system.

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the FHSS for different hopping frequencies, the following tools and software are used:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [5].

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-DDFS which is considered a highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [6].
-Design Environment MATLAB R2008a
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing, and for injecting designs into the FPGA chip.
The block diagram of the laboratory experiment platform is shown in figure (2)[7].

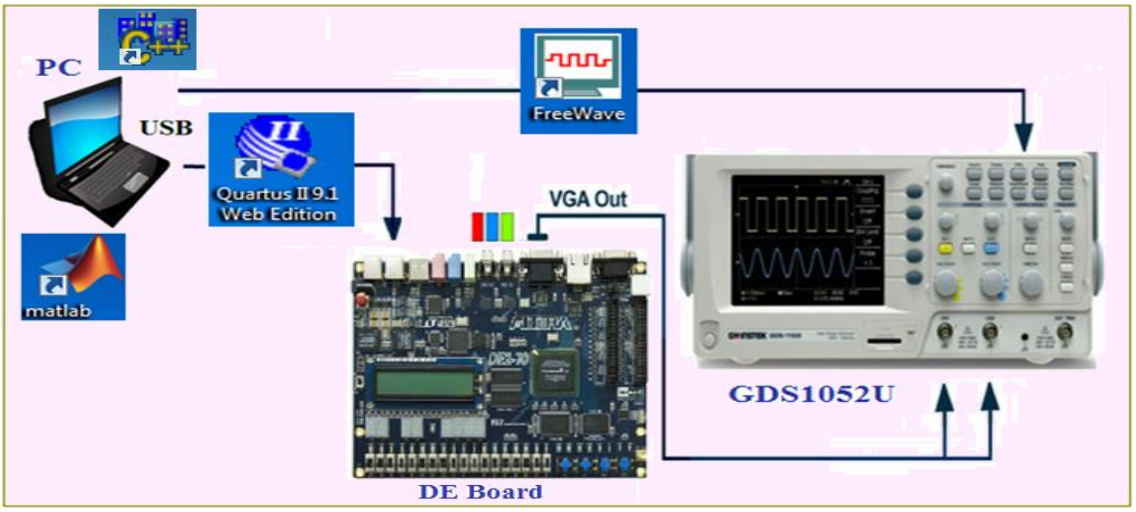

Figure (2) Block diagram of the laboratory experiment platform

IV. BLOCK DIAGRAM OF A FHSS SYSTEM

The block diagram of the FHSS system is shown in figure (3) . It consists of :
-Clock generator with: F_{CLK}=50 MHz.
-Bits numbers of DDFS Phase Accumulator: n=32 bits
-A first frequency divider with a division factor (N_1) to obtain the frequency of the data signal (DATA) F_{DATA}=4 Hz, from clock generator for FHSS system .
-A second frequency divider with a division factor (N_2) to obtain the slow hopping frequency $F_{H\ SLOW}$ =1 Hz from clock generator for slow FHSS system .
-A third frequency divider with a division factor (N_3) to obtain the fast hopping frequency $F_{H\ FAST}$=0.0265HZ from clock generator for fast FHSS system .
-Algorithm hopping table for edge user (ROM 8 X 32 bits) .
-2FSK modulator.
-DDFS to generate the carrier signal for the 2FSK.
-For a FHSS system, to work properly there must be a synchronization between data pulses and frequency hopping pulses for all users.

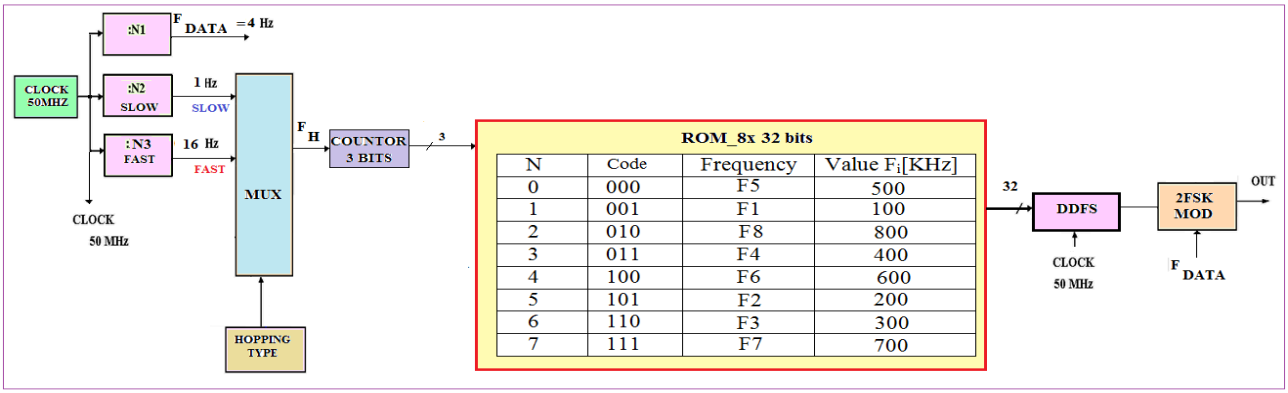

Figure (3) block diagram of FHSS system

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Algorithm of FHSS for three users and eight frequencies is shown in table (1), and algorithm of slow FHSS with 2FSK modulation for three users and eight frequencies is shown in figure (4) ,and algorithm of fast FHSS with 2FSK modulation for three users and eight frequencies is shown in figure (5).

The frequency code (L) is calculated according to the fallowing equation [8]:

$$F_{OUT} = \frac{F_{CLK} * L}{2^n} \Rightarrow L = \frac{2^n . F_{OUT}}{F_{CLK}} \qquad (3)$$

$$L = \frac{2^{32} * F_{OUT}[\text{KHz}]}{50 * 10^3 [\text{KHz}]}$$

$$F_{OUT} = 100,200,300,400,500,600,700,800 \ KHz$$

Table (1) :hopping algorithms for tree users

N	Code	T	Value F_i[KHz] for the first user	Value F_i[KHz] for the second user	Value F_i[KHz] for the third user
0	000	T1	**500**	**200**	**700**
1	001	T2	**100**	**400**	**200**
2	010	T3	**800**	**700**	**500**
3	011	T4	**400**	**100**	**800**
4	100	T5	**600**	**300**	**100**
5	101	T6	**200**	**800**	**600**
6	110	T7	**300**	**600**	**200**
7	111	T8	**700**	**500**	**400**

Calculation Results of frequency codes are set in table (2). L values, and hopping algorithm for the first user are set in table (3). L values, and hopping algorithm for the second user are set in table (4). L values, and hopping algorithm for the third user are set in table(5).

Table (2): frequencies codes of FHSS

Addr	0	1	2	3	4	5	6	7
F_{OUT}[KHz]	100	200	300	400	500	600	700	800
L	8589935	17179870	27569805	34359740	42949675	51539610	60129545	68719480

Table (3) : L values , and hopping algorithms for first user

N	Code	T	F	Value F_{OUT}[KHz] for the first user	Values L for the first user
0	000	T1	F5	500	42949675
1	001	T2	F1	100	8589935
2	010	T3	F8	800	68719480
3	011	T4	F4	400	34359740
4	100	T5	F6	600	51539610
5	101	T6	F2	200	17179870
6	110	T7	F3	300	27569805
7	111	T8	F7	700	60129545

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Table (4) : L values , and hopping algorithms for second user

N	Code	T	F	Value F_i[KHz] for the second user	Values L for the second user
0	000	T1	F2	200	42949675
1	001	T2	F4	400	8589935
2	010	T3	F7	700	68719480
3	011	T4	F1	100	34359740
4	100	T5	F3	300	51539610
5	101	T6	F8	800	17179870
6	110	T7	F6	600	27569805
7	111	T8	F5	500	60129545

Table (5): L values , and hopping algorithms for third user

N	Code	T	F	Value F_i[KHz] for the third user	Values L for the third user
0	000	T1	F7	700	42949675
1	001	T2	F2	200	8589935
2	010	T3	F5	500	68719480
3	011	T4	F8	800	34359740
4	100	T5	F1	100	51539610
5	101	T6	F6	600	17179870
6	110	T7	F2	200	27569805
7	111	T8	F4	400	60129545

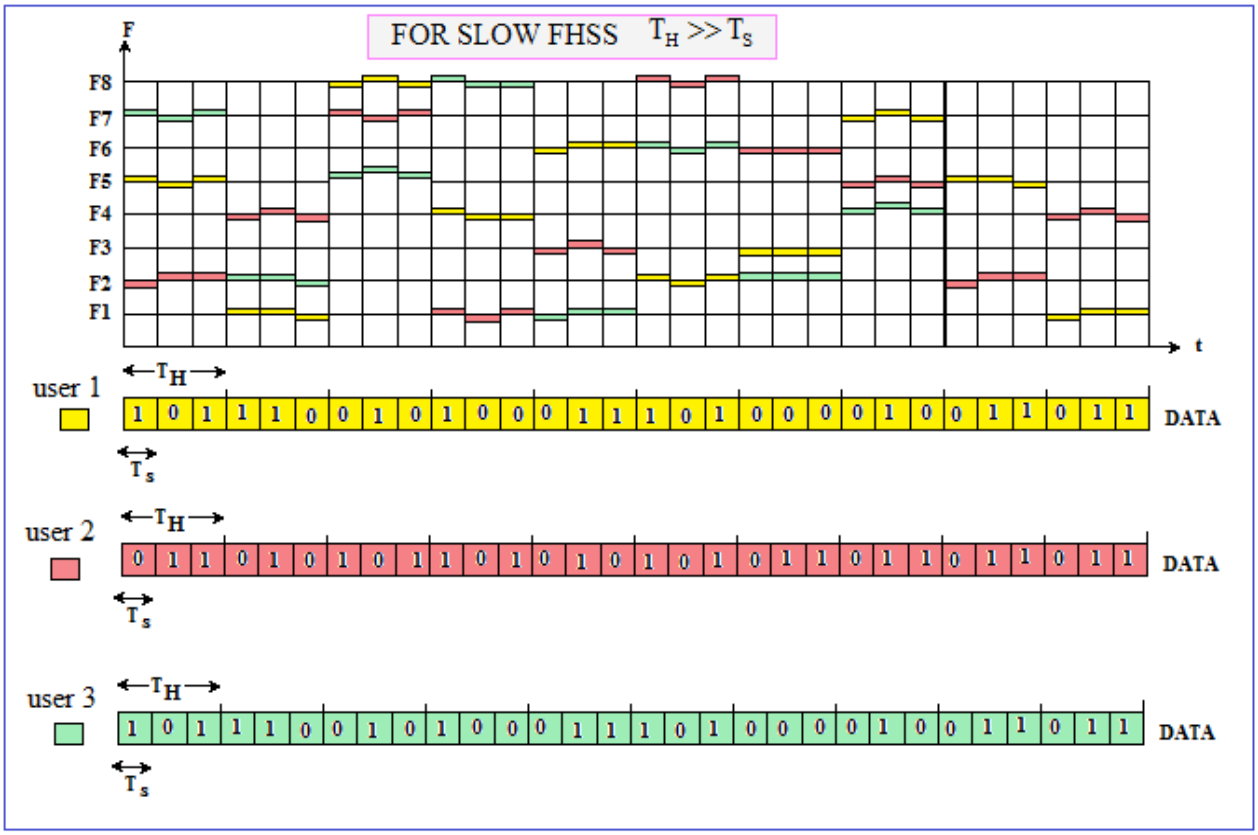

Figure (4) algorithm of the slow FHSS for 2FSK modulation for three users and eight frequencies

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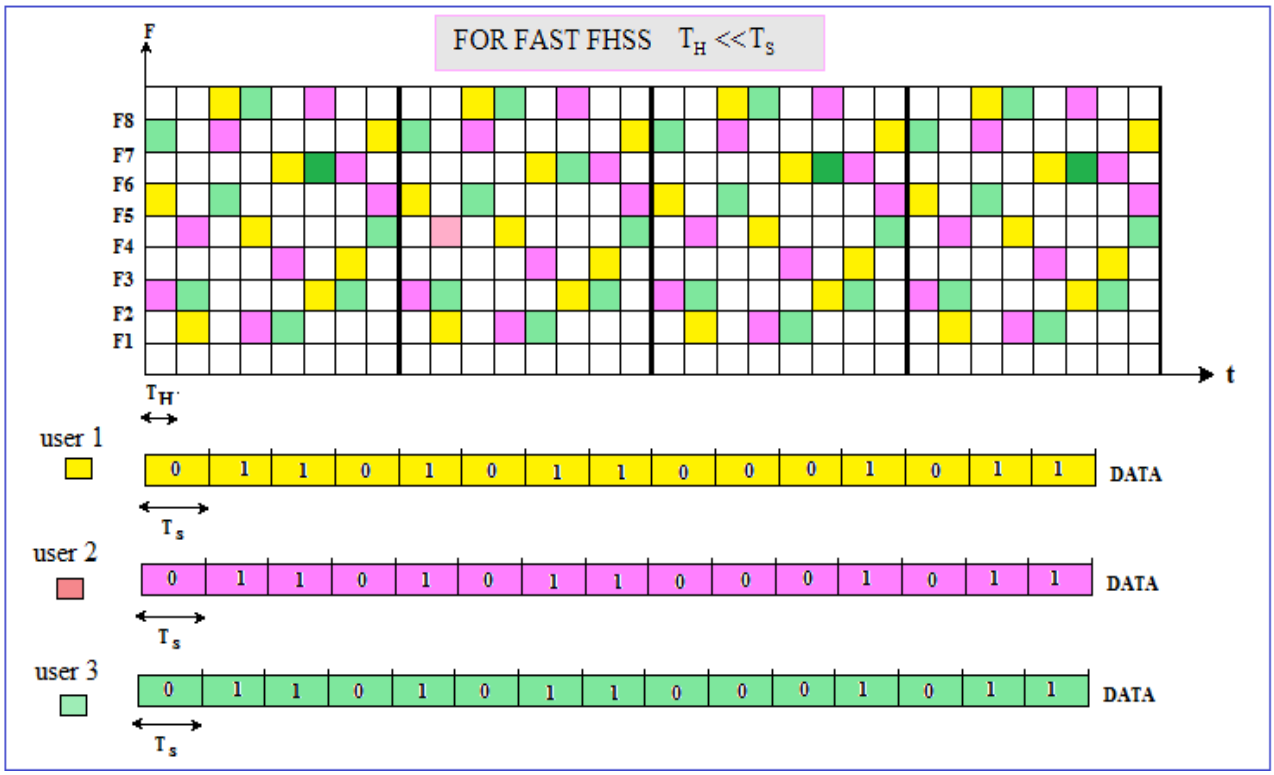

Figure (5) algorithm of the fast FHSS for 2FSK modulation for three users and eight frequencies.

V. FUNCTIONAL DIAGRAM OF A FHSS

DDFS technology allows flexible, accurate and rapid changing of the frequency and phase of the signal. Besides, it allows the frequency hopping process to be achieved according to a specific algorithm through the use of a binary counter and a hopping algorithm memory that contains frequency codes according to the block diagram shown in figure (6).

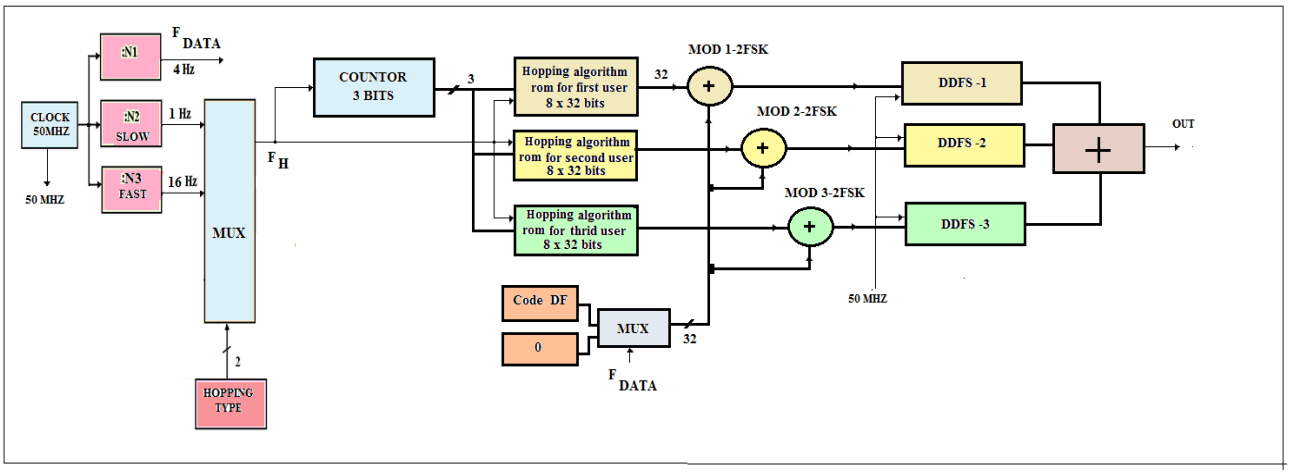

Figure (6) Functional diagram of a spectrum spreader FHSS for three users and eight frequencies.

The functional diagram of FHSS system in Quartus II 9.1 design environment is shown in figure (7) [8] where:
-Hopping type: slow , fast.
-Number of users: three.
-Number of frequencies: eight.
-Hopping algorithm for first user is shown in table (3), hopping algorithm for second user is shown in table(4), and hopping algorithm for third user is shown in table(5).

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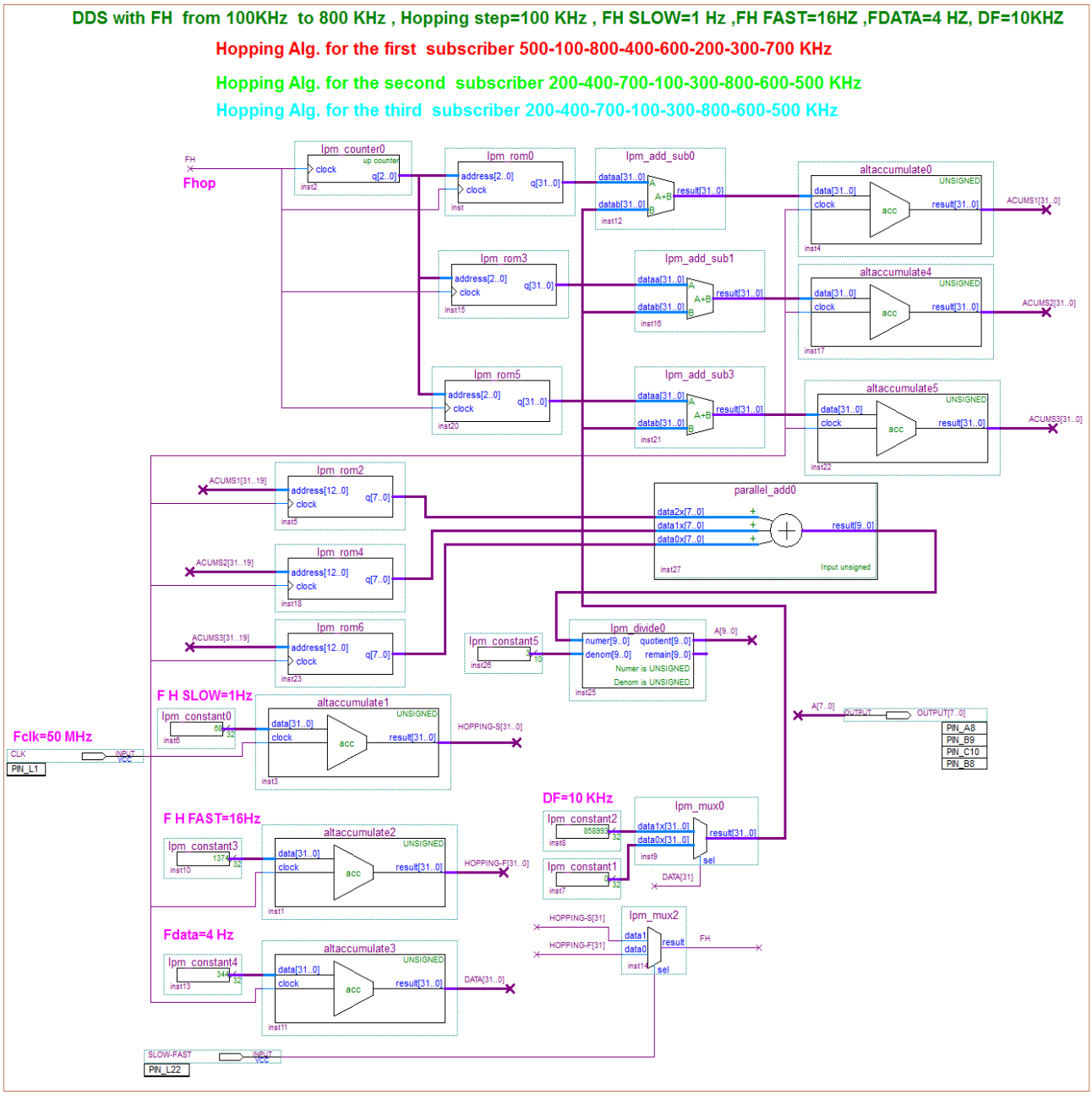

Figure (7) functional diagram of FHSS in Quartus II 9.1 design environment for three users and eight frequencies.

-Frequency of the data signal generator (DATA) is calculated according to the following equation [6]:

$$F_{DATA} = \frac{F_{CLK} * L_{DATA}}{2^{n}} \qquad (4)$$

Where: $F_{DATA} = 4\text{Hz}$

$$L_{DATA} = \frac{F_{DATA} * 2^{n}}{F_{CLK}} = \frac{4 * 2^{32}}{50 * 10^{6}} = 344 \Rightarrow T_S = 1/F_{DATA} = 1/4 = 0.25 \text{ sec}$$

For slow FHSS: $F_{H\_SLOW} = 1Hz$

$$F_{H\_SLOW} = \frac{F_{CLK} * L_{H\_SLOW}}{2^{n}} \qquad (5)$$

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$$L_{H\ SLOW} = \frac{F_{H\ SLOW} * 2^{n}}{F_{CLK}} = \frac{1*2^{32}}{50*10^{6}} = 86 \Rightarrow T_{H\ SLOW} = 1/F_{H\ SLOW} = 1/1 = 1\text{sec}$$

For fast FHSS: $F_{H\ FAST} = 16Hz$

$$F_{H\ FAST} = \frac{F_{CLK} * L_{H\ FAST}}{2^{n}} \qquad (6)$$

$$L_{H\ FAST} = \frac{F_{H\ FAST} * 2^{n}}{F_{CLK}} = \frac{16*2^{32}}{50*10^{6}} = 1374 \Rightarrow T_{H\ FAST} = 1/F_{H\ FAST} = 1/16 = 0.0625\ \text{sec}$$

The functional diagram of data generator and hopping generator of FHSS system in Quartus II 9.1 design environment [9] is shown in figure (8).

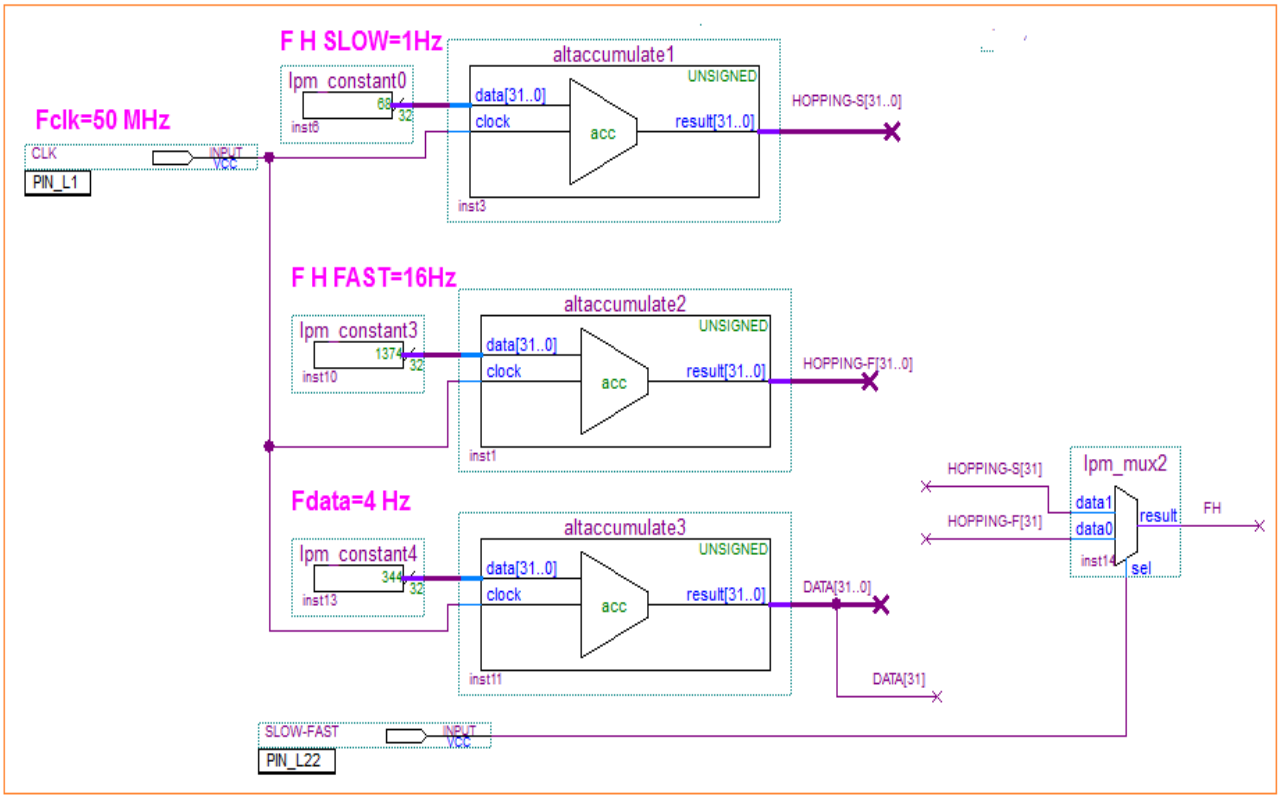

Figure (8) functional diagram of the clock signals of FHSS in Quartus II 9.1 design environment

VI. BLOCK AND FUNCTIONAL DIAGRAM OF A 2FSK MODULATOR

The block diagram of the 2FSK modulator [5] is shown in figure (9) and the functional diagram of the 2FSK modulator [7] is shown in figure (10),where:

-Bits numbers of Phase Accumulator : n=32 bits
-Clock frequency : F_{CLK}=50MHz.
-F_{OUT}=100,200,300,400,500,600,700 , 800 KHz.
-Frequency Deviation of 2FSK is : DF=10KHz.
-Size of DDFS ROM: 13KB.
-DAC :with 8 bits.

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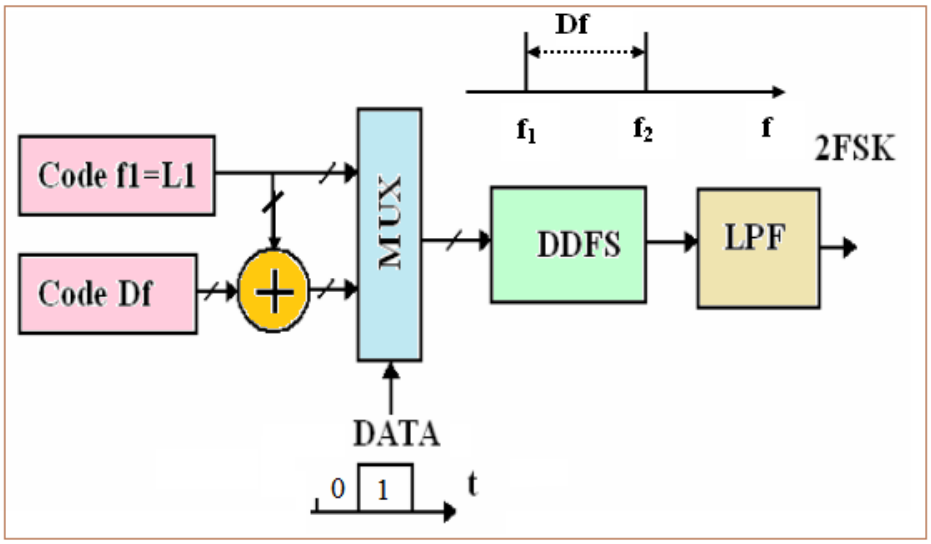

Figure (9) block diagram of the 2FSK modulator

- Operating frequency of the DDFS is calculated according to the following equation [9] , and frequency resolution is :

$$\delta f = \frac{F_{CLK}}{2^n} \qquad (7)$$

$$\delta f = \frac{F_{CLK}}{2^n} = \frac{50*10^6}{2^{32}} = 0.011\text{Hz}$$

$$F_{OUT} = \frac{F_{CLK} * L}{2^n} \qquad (8)$$

Where:

$$L = \frac{2^n * F_{OUT}}{F_{CLK}} \qquad (9)$$

For: n=32 bits and F_{OUT}=100 KHz to:

$$L = \frac{2^n * F_{OUT}}{F_{CLK}} = \frac{2^{32} * 100}{50000} = 8589935$$

- Code of DF=10 KHz for 2FSK modulation is calculated according to the following equation [5]:

$$L_{DF} = \frac{2^n * DF}{F_{CLK}} = \frac{2^{32} * 10}{50000} = 858993$$

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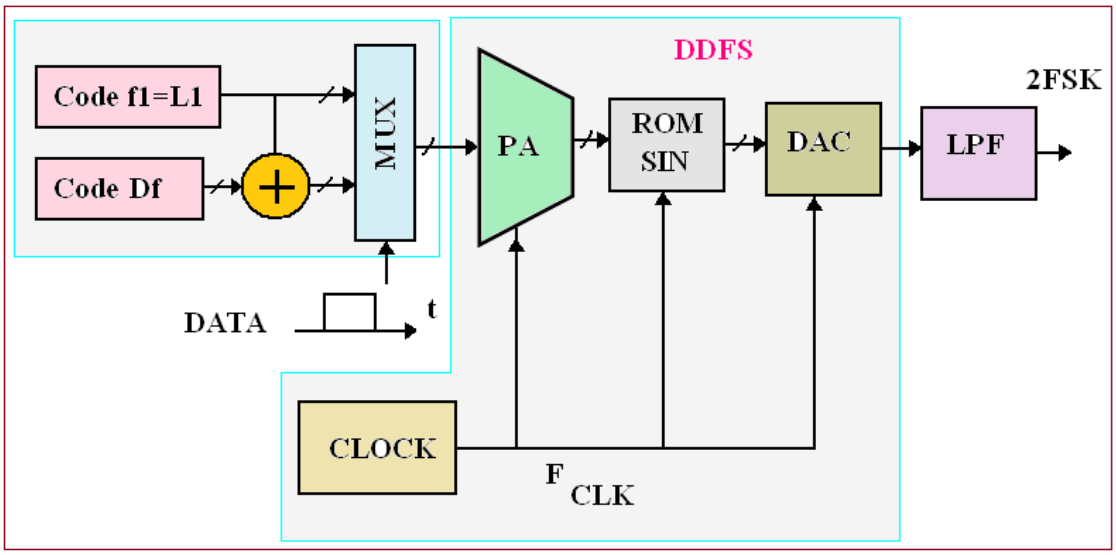

Figure (10) functional diagram of the 2FSK modulator

The functional diagram of the DDFS-2FSK in the Quartus II 9.1 design environment is shown in Figure (11), where: F_{CLK}=50 MHz , DF=10 KHz , F_{OUT}=100 KHz for logic (0) symbol or F_{OUT}=110 KHz for logic (1) symbol ,F_{DATA}=1 KHz.

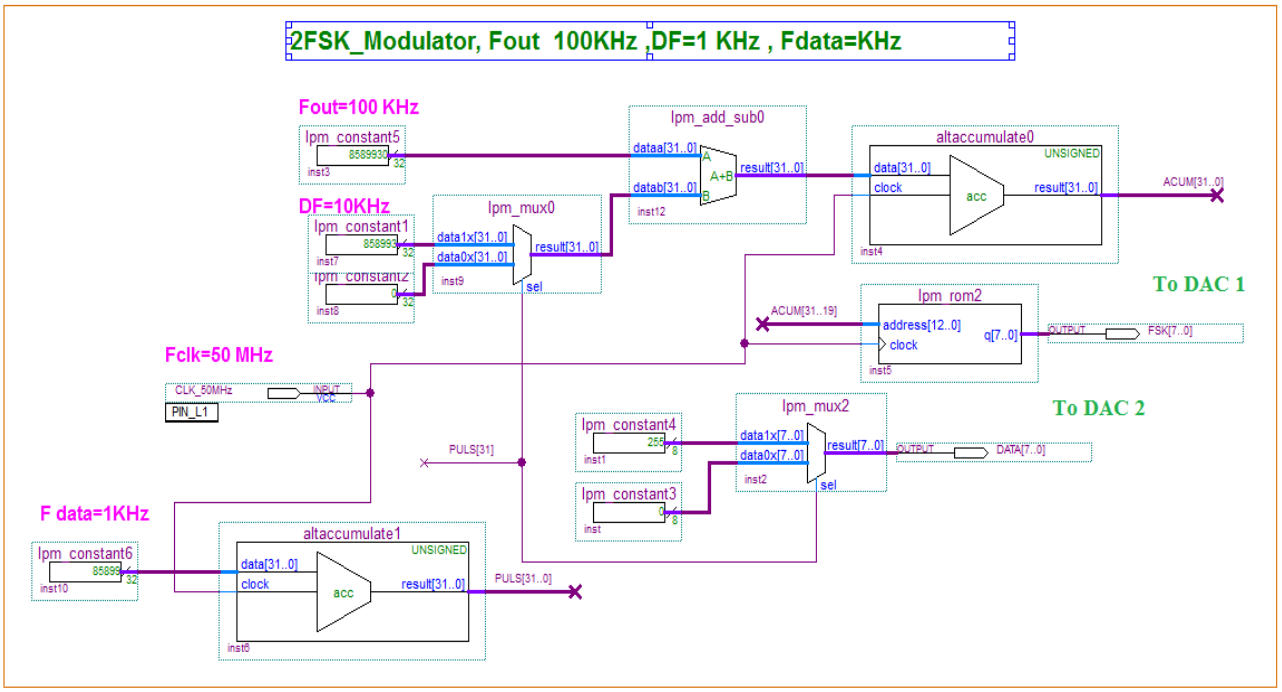

Figure (11) functional diagram of 2FSK modulator in Quartus II 9.1 design environment

XII. CONCLUSION AND EXPERIMENTAL RESULTS

The results of the practical design of a DDFS-2FSK modulator in time domain for (F_{data}=1KHz) and operating frequency (F_{OUT} = 100 KHz) and DF=10KHz is shown in figure (12).

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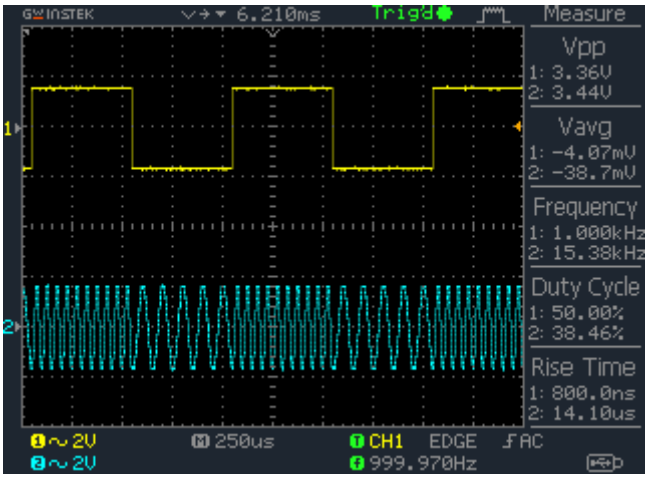

Figure (12) output signal of DDFS-2FSK modulator in time domain

-The results of the practical design of a digital FHSS in frequency domain for eight frequencies values and three users in time interval (T_1) is shown in figure (13).

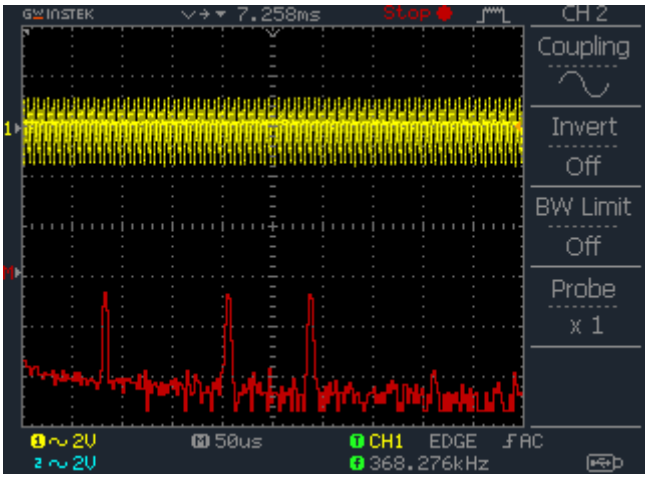

Figure (13) results in frequency domain of practical design of FHSS in time interval T_1 (F2,F5,F7).

-The results of the practical design of a digital FHSS in frequency domain for eight frequencies values and three users in time interval (T_2) is shown in figure (14).

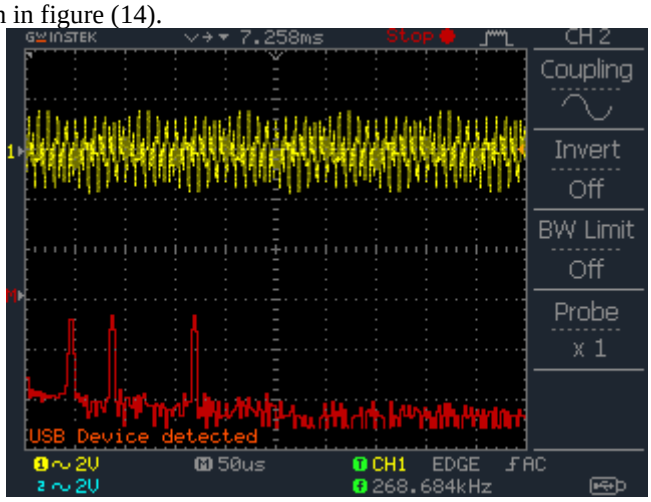

Figure (14) results in frequency domain of practical design of FHSS in time interval T_2 (F1,F2,F4).

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-The results of the practical design of a digital FHSS in frequency domain for eight frequencies values and three users in time interval (T_3) is shown in figure (15) and….etc.

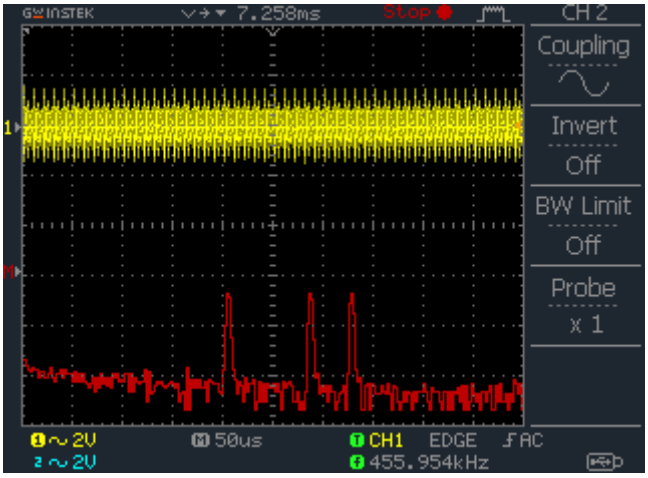

Figure (15) results in frequency domain of practical design of FHSS in time interval T_3 (F5,F7,F8).

-As the number of users increases, the capacity of the communications system increases and the bandwidth of the spread signal spectrum increases until it approaches noise.
-Developing the designed system so that the number of users is greater, and the number of frequencies is greater is possible by using a FPGA chip with greater material resources.

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BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university.

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