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ADVANCED REVERSIBLE LOGIC APPROACHES FOR MAGNITUDE COMPARATOR DESIGN AND ITS FPGA IMPLEMENTATION

Jes Evans Daniel[1], Dr.R.Manjith[2]

II year M.E VLSI Design, 'Dr.Sivanthi Aditanar College of Engineering, Tiruchendur[1]

Associate Professor/ECE Department, Dr.Sivanthi Aditanar College of Engineering, Tiruchendur[2]

Abstract: Reversible or information lossless gates have applications in nano-technology, digital signal processing (DSP) and in communication The power consumption is one of the biggest challenging issues for designing of VLSI circuits within the advanced technology. The reversible logic is one among the best approaches for low power application The main objective of this paper is to design and implementation of a magnitude comparator using reversible logic approaches. In this paper a 16-bit and 32-bit magnitude comparator are implemented with using reversible logic gates. The simulation of 16-bit and 32-bit magnitude comparator is carried out using Verilog HDL coding in Xilinx Software. Simulation results provide significant improvement in power consumption for 16-bit and 32-bit magnitude comparator using the proposed reversible logic gates method. Therefore, the proposed scheme can provide a significant improvement in comparator circuit in chips for future generation of VLSI blocks.

Keywords: Reversible, Verilog HDL, Xilinx, BJN gate, Power consumption.

I. INTRODUCTION

In advanced technology, the reversible logic is one among the simplest designing strategies for low power VLSI design. Since reversible logic is lossless, so this logic based circuit has no tendency to lose the information. Consequently, the power consumption is lower in reversible logic gate based circuit design compared to other combinational logic gate based CMOS logic styles. First a 16-bit Magnitude Comparator is constructed using Verilog code by giving 16 inputs for a and b in vector form. Then the given inputs are compared and according to that the output comes as a greater than b, a less than b or aeb depending on the input values given. Then the output waveform and Power consumption are taken using Xilinx software. After this process a 32-bit Magnitude Comparator is constructed by giving 32 input bits for a and b in vector form. Then the given inputs are compared and according to that the output comes as a greater than b, a less than b or aeb depending on the input values given. Then the output waveform and Power consumption are taken using Xilinx software. After this process a 16-bit magnitude comparator is constructed using reversible logic gates. By using Verilog code the output waveform is taken and the power consumption is also taken using Xilinx software. Then 32-bit magnitude comparator is constructed using reversible logic and the Output is taken and the power consumption is also calculated in Xilinx software. Finally all the result is compared.

II. REVERSIBLE LOGIC GATES

In today's life, the optimization of low power VLSI circuit is designed by the various techniques. The reversible logic based VLSI circuit is one of the best approaches in advanced technology. An optimized reversible logic circuit should have a minimum number of constant input, garbage output, reversible gate, and quantum cost. The constant input is represented by 0 or 1. The garbage outputs are those outputs which are not generating any useful function. The quantum cost is defined as the cost of the overall circuit in terms of primitive gate. In this section, the essential gates like NOT Gate, CNOT Gate, TR Gate, PG Gate, FG Gate, and BJN Gate are discussed below.

A.Not Gate

The NOT gate has single input and single output [4]. The output of the NOT gate is defined by $P = A^{-}$ where, A is the input of the NOT gate. It is a 1 × 1 reversible gate which has zero quantum cost. The block diagram of NOT gate is shown in Figure 1.

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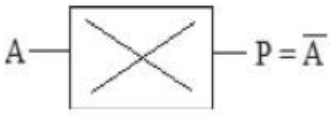

Fig 1. Block Diagram of Not gate

B.TR Gate

The TR gate is a 3 × 3 reversible gate whose quantum cost is 4. The inputs are represented by (A, B, C) and therefore the outputs are represented by (P, Q, and R). The outputs are defined by P = A, Q = (A ⊕ B), R = (AB ⊕ C). The block diagram of TR gate is shown in Figure 2.a

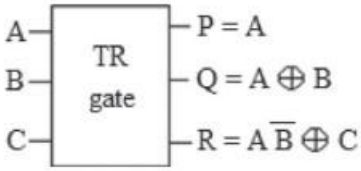

Fig 2. Block Diagram of TR Gate

C.Peres Gate

The Peres gate (PG) is a 3 × 3 reversible gate which has a quantum cost equal to 4. The inputs are represented by (A, B, C) and therefore the outputs are represented by (P, Q, and R). The outputs are defined by P = A, Q = (A ⊕ B), R = (AB ⊕ C). The block diagram of PG gate is shown in Figure 3.

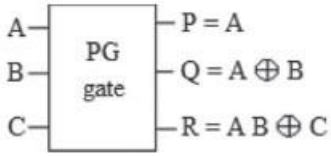

Fig 3. Block Diagram of PG gate

D.Feynman Gate

The Feynman gate (FG) is a 2 × 2 reversible CNOT gate which has two inputs (A, B) and two outputs (P, Q). The outputs are defined by P = A, Q = (A ⊕ B). The quantum cost of this gate is equal to 1. The block diagram of this gate is shown in Figure 4.

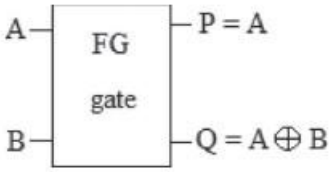

Fig 4. Block Diagram of FG gate

E.BJN Gate

The BJN gate is a 3 × 3 reversible gate. The inputs are represented by (A, B, C) and the outputs are represented by (P, Q, and R). The outputs are defined by P = A, Q = B and R = [(A + B) ⊕ C]. The quantum cost is equal to 5. The block diagram of BJN gate is shown in Figure 5.

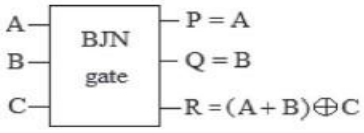

Fig 5. Block Diagram of BJN gate

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III. MAGNITUDE COMPARATOR

The magnitude comparator is a combinational logic circuit that compares two logic signals (A, B) according to their relative magnitude and gives three outputs which show that one signal is greater than, less than or equal to the other signal. The block diagram of a 4-bit comparator is shown in Figure 6.

The outputs of the 4-bit comparator are expressed by Equations (1)–(3).

$$A > B = A0B0' + (A0 \text{ XNOR } B0)[A1B1' + (A1 \text{ XNOR } B1) \times \{A2B2' + (A2 \text{ XNOR } B2)A3B\ 3'\}] \quad - (1)$$

$$A < B = A0' B0 + (A0 \text{ XNOR } B0)[A1' B1 + (A1 \text{ XNOR } B1) \times \{A2' B2 + (A2 \text{ XNOR } B2)A3' B3\}] \quad - (2)$$

$$A = B = (A0 \text{ XNOR } B0)(A1 \text{ XNOR } B1)(A2 \text{ XNOR } B2) \times (A3 \text{ XNOR } B3 \quad - (3)$$

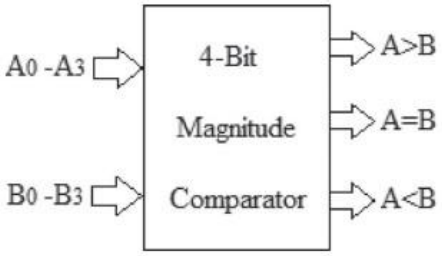

Fig 6. Block Diagram of 4-bit Magnitude Comparator

IV. DIFFERENT MAGNITUDE COMPARATOR DESIGN USING PROPOSED METHODS

The Magnitude Comparator is proposed by using reversible gates and decision blocks. By using reversible gates and logic the 16-bit and 32-bit Magnitude Comparator is proposed.

(i) 16-bit Reversible Magnitude Comparator

The 16-bit Reversible Magnitude Comparator is proposed by using 8 2-bit Magnitude Comparators, 7 decision blocks and 1 BJN gate. The Proposed Block diagram is shown in fig 7.

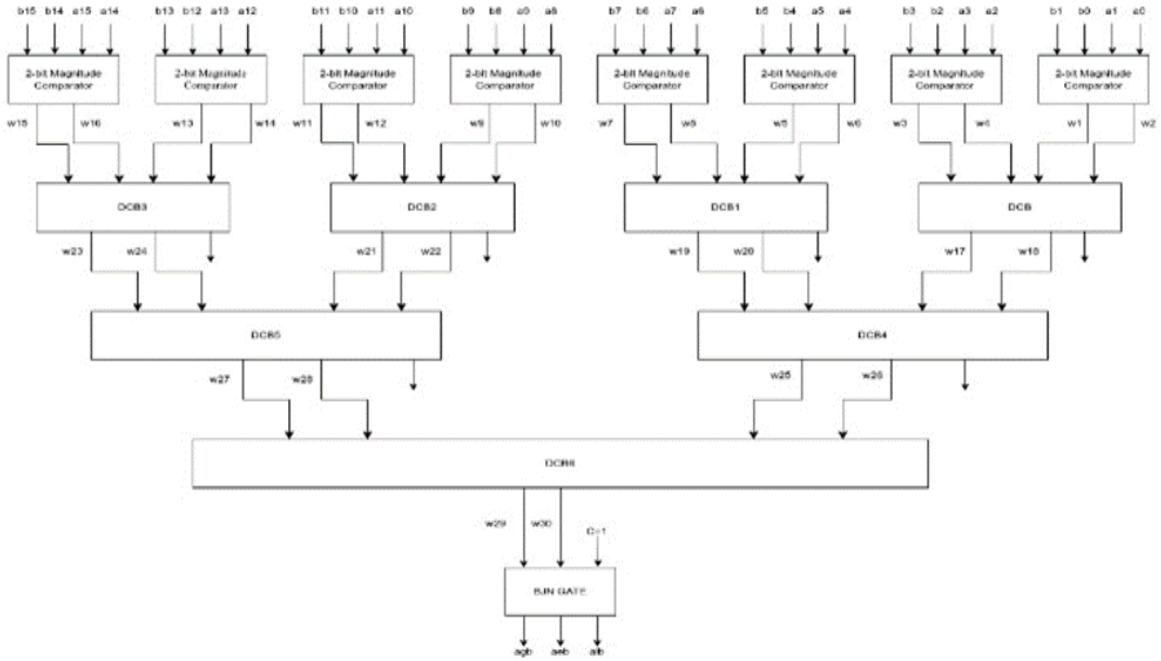

Fig 7. Block Diagram of 16-bit Reversible Magnitude Comparator

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These blocks are coded using Verilog HDL Code in Xilinx software and the output is taken. Hence Power consumption is also obtained using Xilinx software. The circuit diagram of decision block is shown in fig 8.

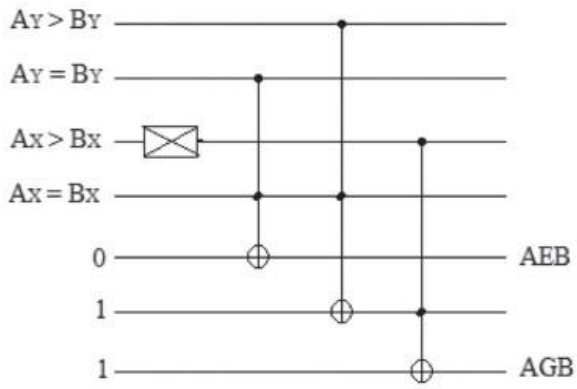

Fig 8.Circuit Diagram of Decision Block

(ii) 32-bit Reversible Magnitude Comparator

Like 16-bit Reversible Magnitude Comparator, a 32-bit Reversible Magnitude Comparator is proposed using 15 2-bit Magnitude Comparators, 14 decision blocks and 1 BJN

Gate. The Proposed block diagram is shown in fig 9.These block are coded using Verilog HDL code in Xilinx software and the output is obtained. Hence power consumption is also obtained using Xilinx software.

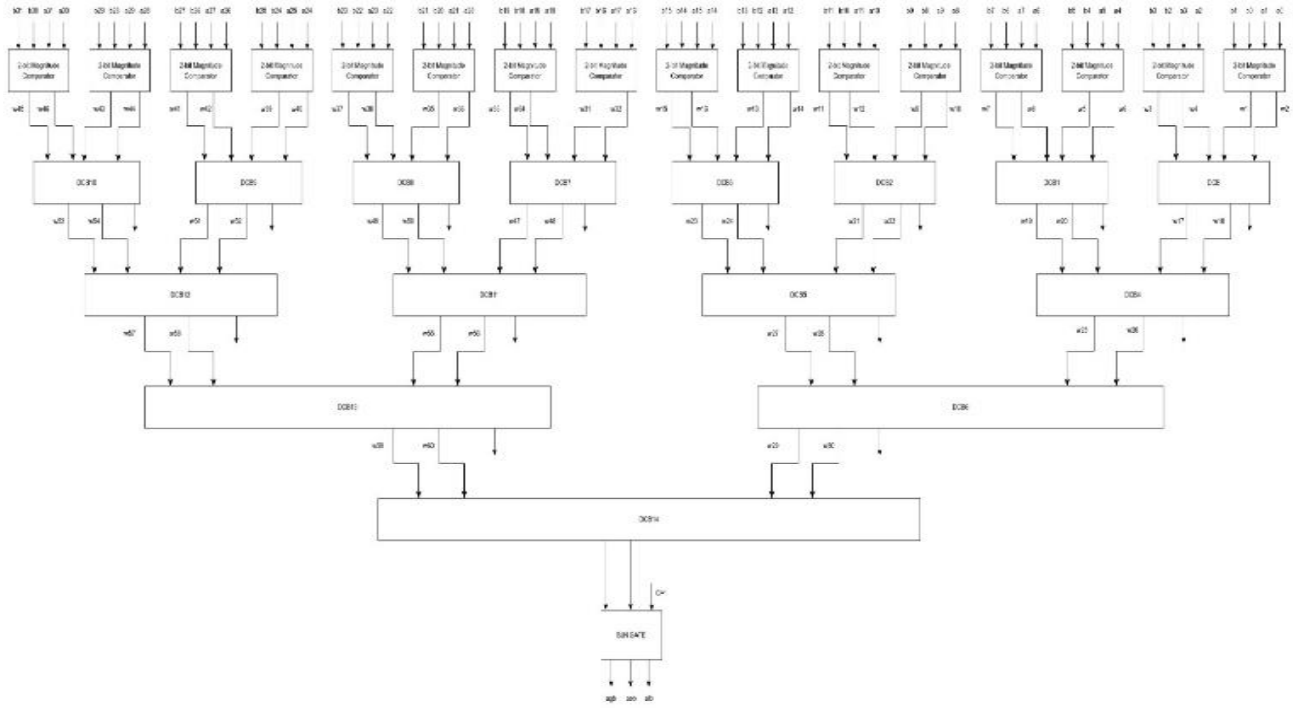

Fig.10. Block diagram of 32-bit Reversible Magnitude Comparator

The table for the power consumption and output waveform are shown in table 1 and fig 11.

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Table 1. Power consumption of 16-bit reversible magnitude comparator

REVERSIBLECOMPARATOR Project Status			
Project File:	ReversibleComparator.ise	**Current State:**	Placed and Routed
Module Name:	topmodule16bit	**• Errors:**	No Errors
Target Device:	xqv600e-6bg432	**• Warnings:**	35 Warnings
Product Version:	ISE 9.2i	**• Updated:**	Mon Jun 10 12:53:31 2024

REVERSIBLECOMPARATOR Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	10	13,824	1%	
Logic Distribution				
Number of occupied Slices	5	6,912	1%	
Number of Slices containing only related logic	5	5	100%	
Number of Slices containing unrelated logic	0	5	0%	
Total Number of 4 input LUTs	10	13,824	1%	
Number of bonded IOBs	35	316	11%	
Total equivalent gate count for design	84			
Additional JTAG gate count for IOBs	1,680			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints		

The above table shows the overview design summary of the 16-bit reversible magnitude comparator.

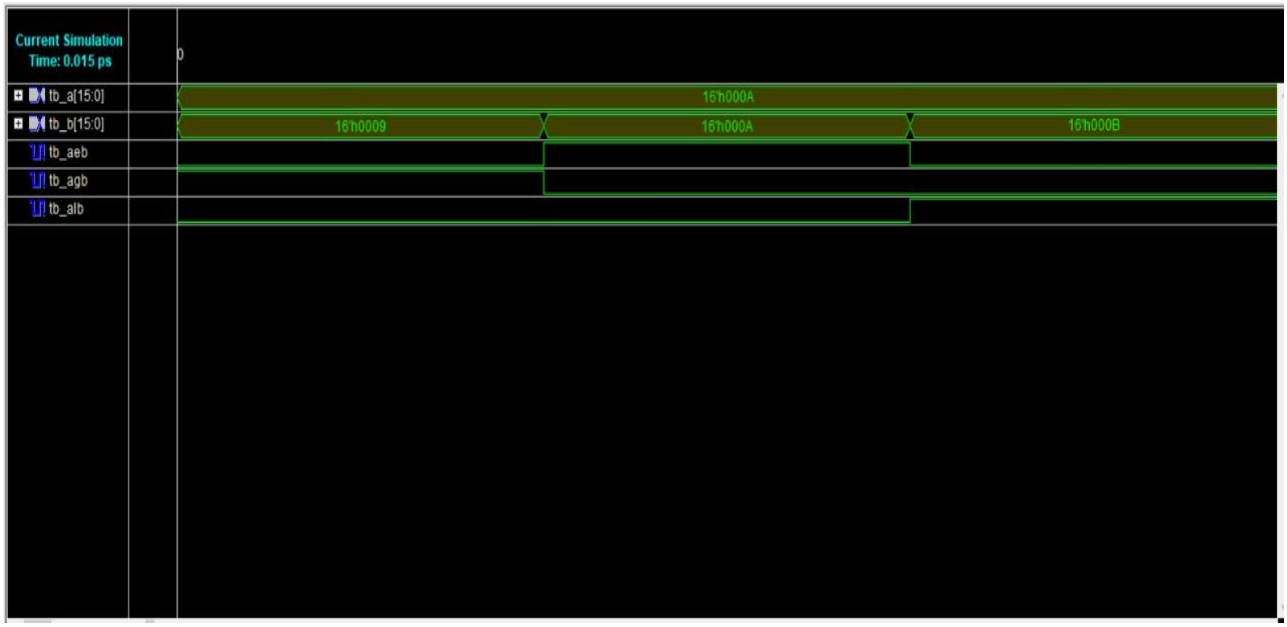

Fig 11.Output waveform of 16-bit reversible magnitude comparator

+

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```
--------------------------------------------------------------------
Release 9.2i - XPower SoftwareVersion:J.36
Copyright (c) 1995-2007 Xilinx, Inc.  All rights reserved.
Design:       E:\Daniel Project\ReversibleComparator\topmodule16bit.ncd
Preferences:  topmodule16bit.pcf
VCD File:     E:\Daniel Project\ReversibleComparator\tb_topmodule16bit.vcd
Part:         xqv600ebg432-6
Data version: PRODUCTION,v1.0,05-28-03

Power summary:                          I(mA)     P(mW)
--------------------------------------------------------------------
Total estimated power consumption:                   7
                                        ---
                        Vccint 1.80V:     0         0
                        Vcco33 3.30V:     2         7
                                        ---
                             Inputs:      0         0
                              Logic:      0         0
                            Outputs:
```

Fig 12. Power consumption of 16bit reversible magnitude comparator

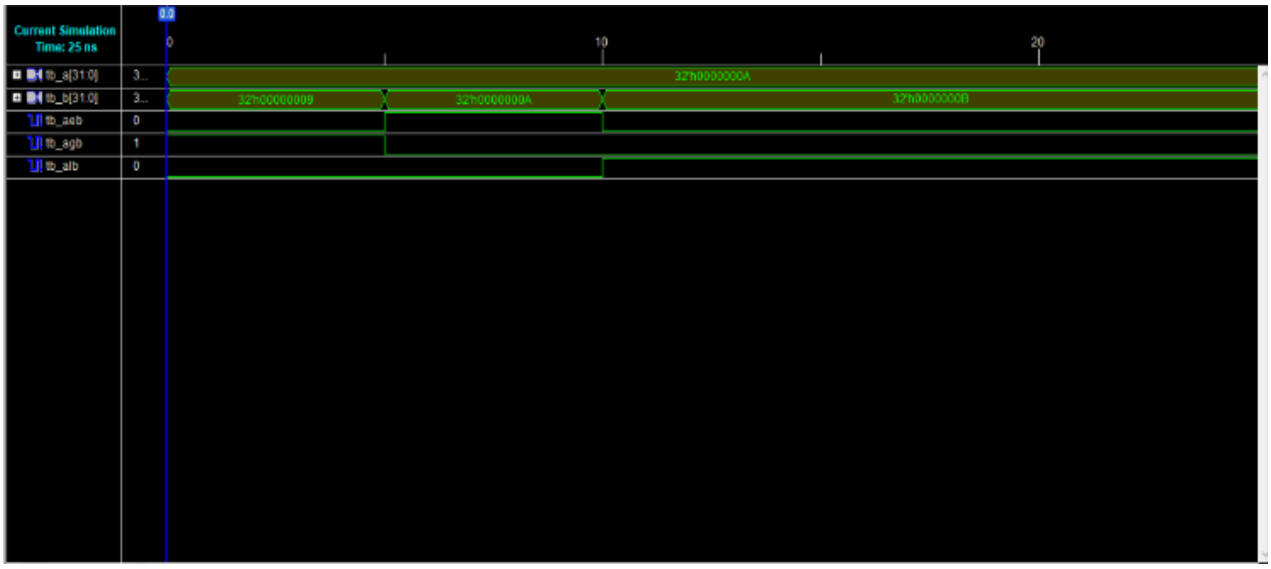

Fig 13. Output waveform of 32-bit reversible magnitude comparator

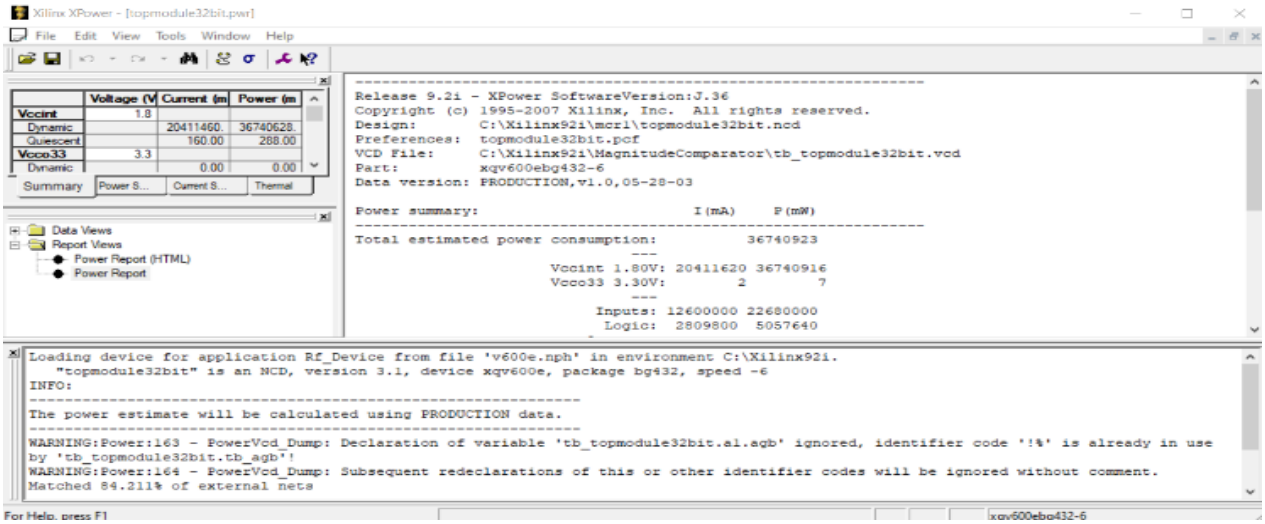

Fig 14. Power Consumption of 32-bit reversible magnitude comparator

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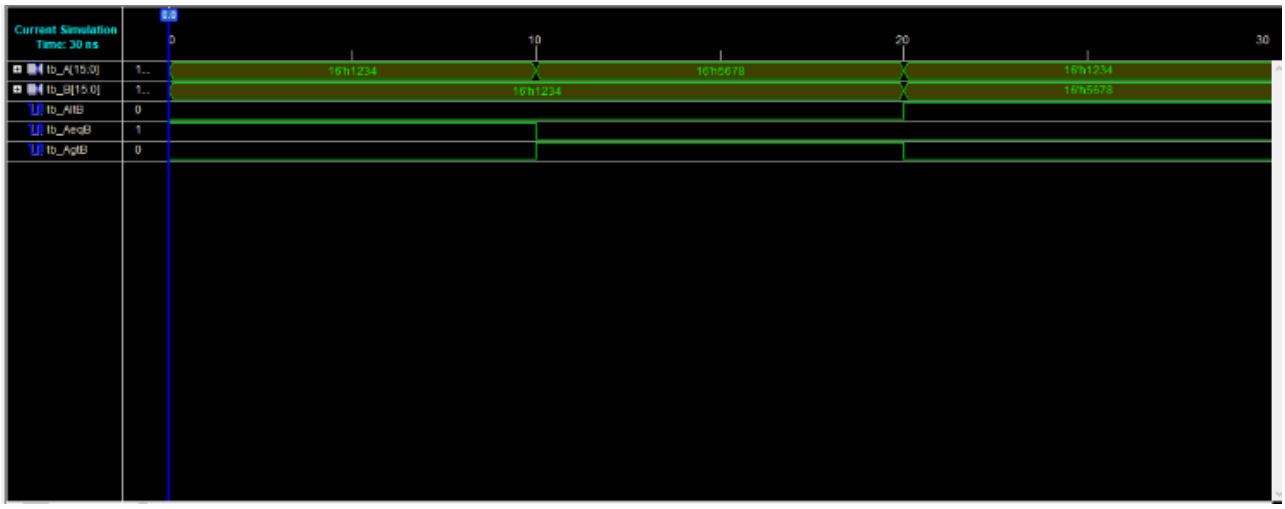

Fig 15.Output Waveform of 16-bit magnitude comparator

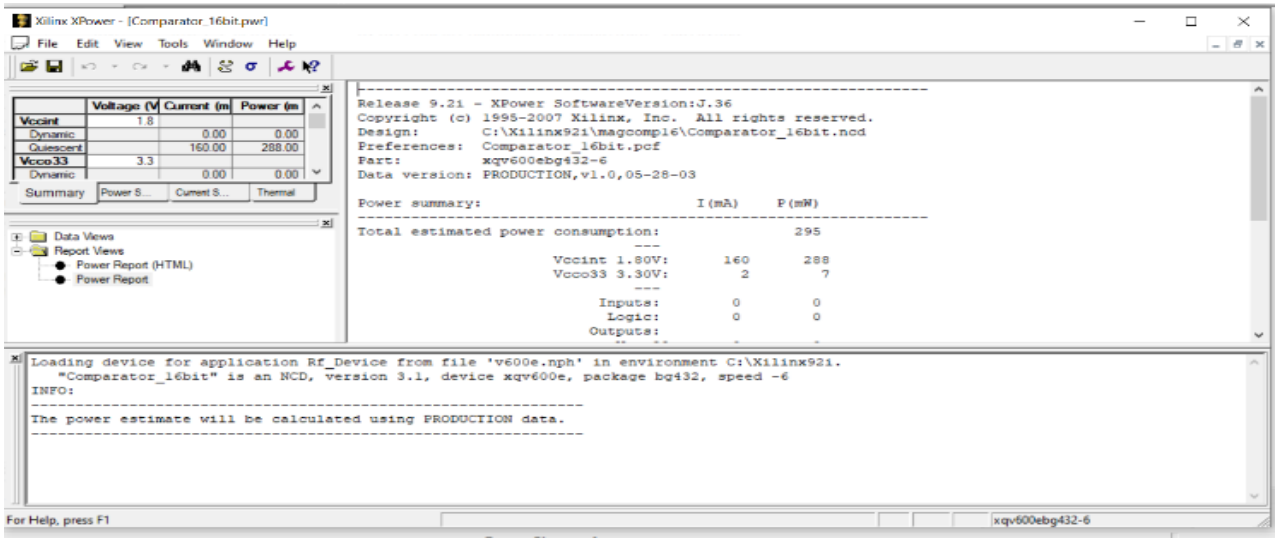

Fig 16.Power Consumption of 16-bit magnitude comparator

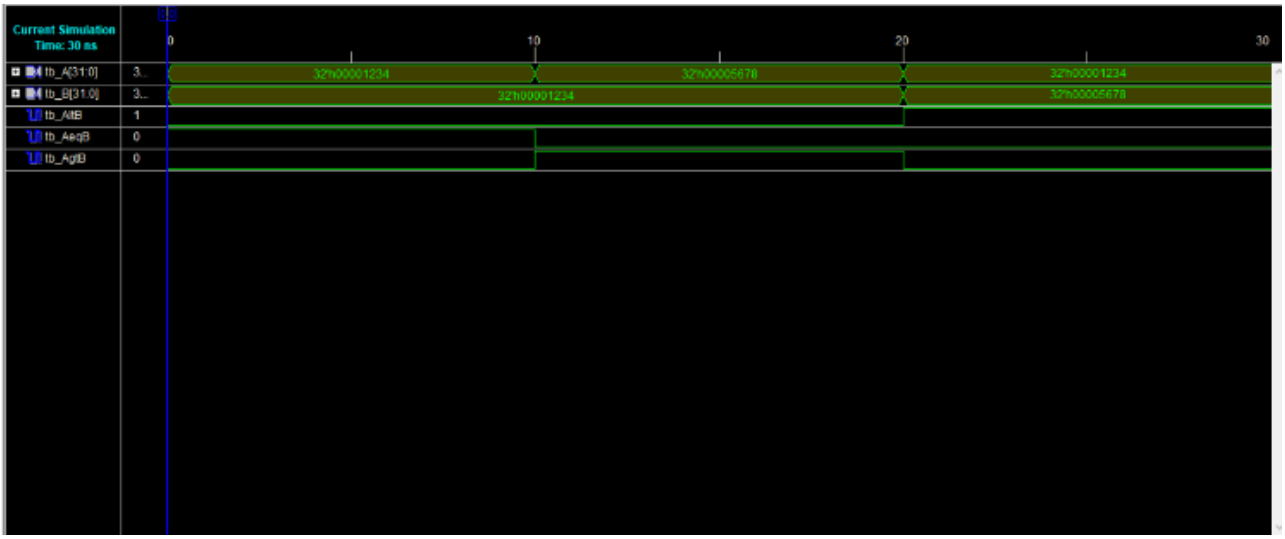

Fig 17.Output waveform of 32-bit magnitude comparator

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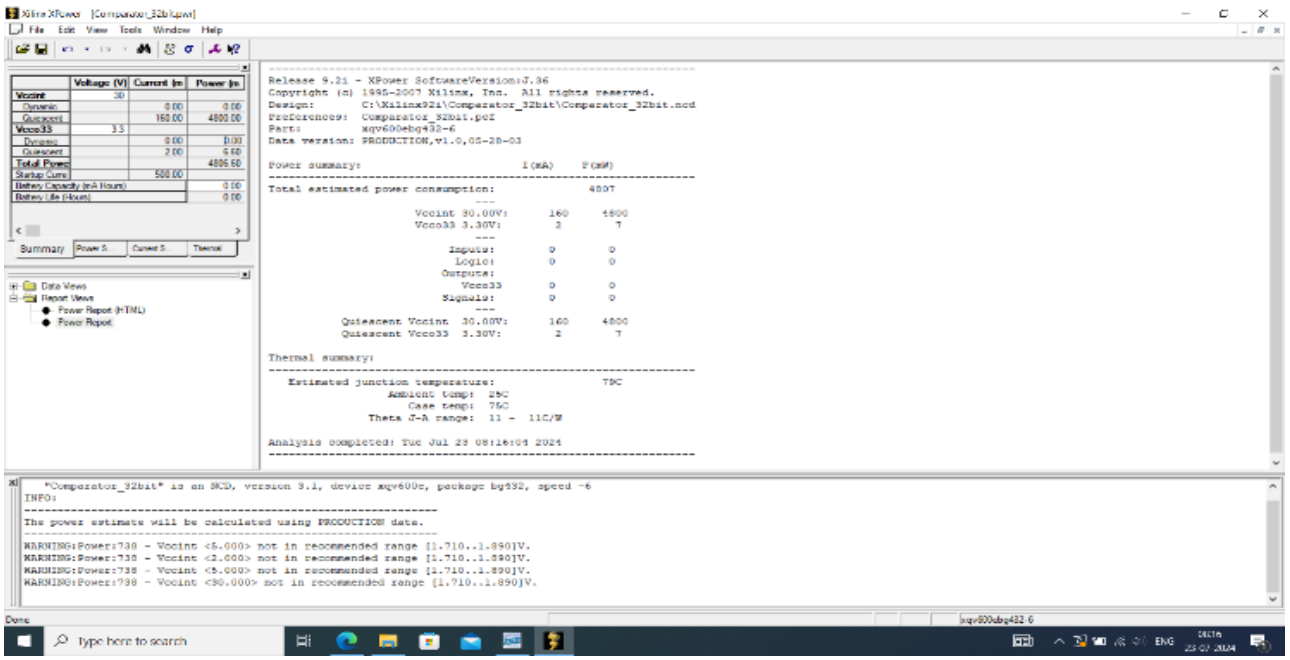

Fig 18.Power Consumption of 32-bit magnitude comparator

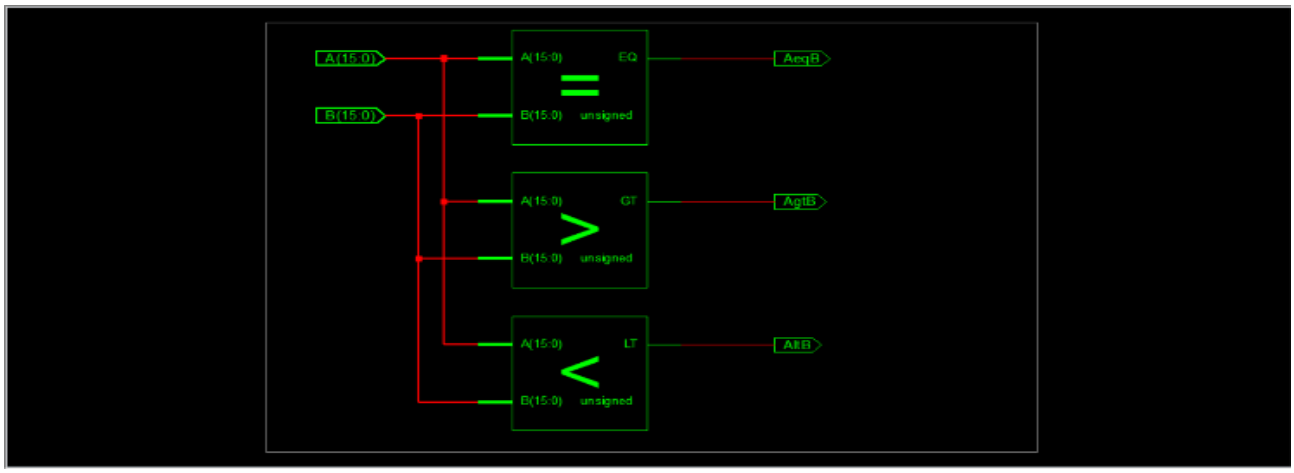

Fig 19.Structural diagram of 16-bit magnitude comparator

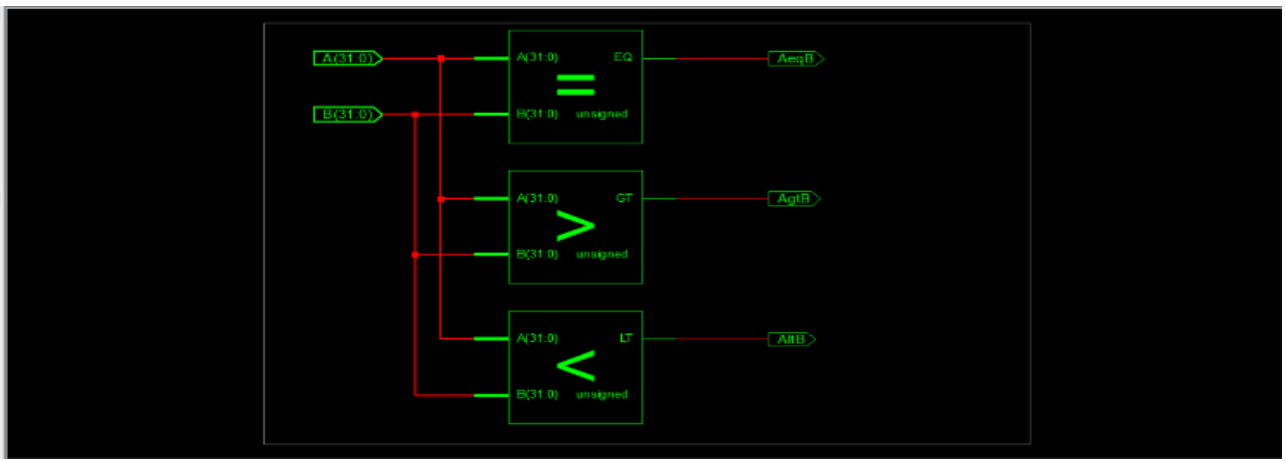

Fig 20.Structural diagram of 32-bit magnitude comparator

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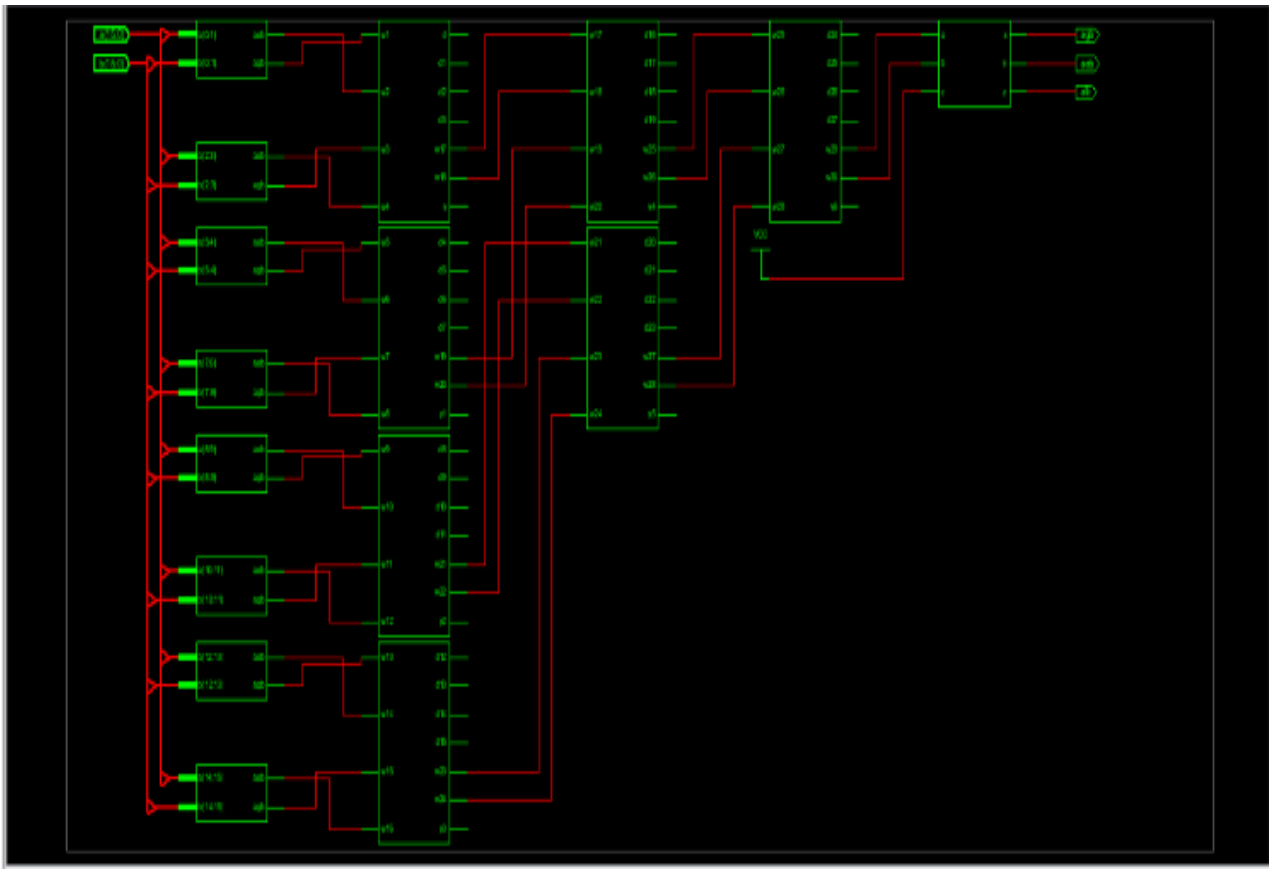

Fig 21.Structural diagram of 16-bit reversible magnitude comparator

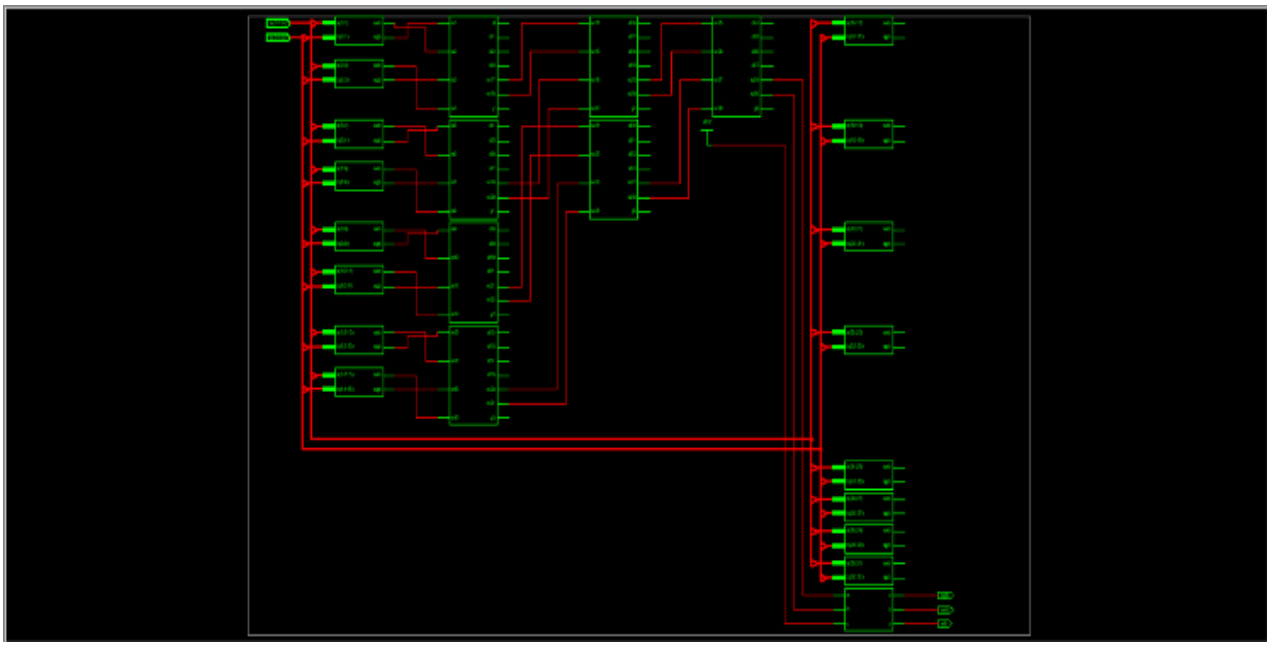

Fig 22.Structural diagram of 32-bit reversible magnitude comparator

Fig 12 shows the power consumption of 16-bit reversible magnitude comparator. Fig 13 shows the Output waveform of 32-bit reversible magnitude comparator. Fig 14 shows the Power Consumption of 32-bit reversible magnitude comparator. Fig 15 shows the Output waveform of 16-bit Magnitude Comparator. Fig 16 shows the Power consumption of 16-bit magnitude comparator. Fig 17 shows the Output waveform of 32-bit magnitude comparator. Fig

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18 shows the Power Consumption of 32-bit magnitude comparator. Fig 19 shows the Structural diagram of 16-bit magnitude comparator. Fig 20 shows the Structural diagram of 32-bit magnitude comparator. Fig 21 shows the structural diagram of 16-bit reversible magnitude comparator. Fig 22 shows the structural diagram of 32-bit reversible magnitude comparator.

Table 2.Comparision of Power Consumption of 16-bit and 32-bit Magnitude comparator with and without using reversible logic

Magnitude Comparator	Power Consumption	
	Without reversible logic	With reversible logic
16-bit	295mW	7mW
32-bit	4807mW	3674mW

V. CONCLUSION

Thus 16-bit and 32-bit magnitude comparators are proposed with reversible logic. The 16-bit and 32-bit magnitude comparator are proposed without using reversible logic.It is written in Verilog HDL coding in Xilinx software and the output waveforms and power consumptions are successfully obtained . The Power consumption of 16-bit magnitude comparator using reversible logic is 2.37%more efficient than normal 16-bit magnitude comparator. Similarly the power consumption of 32-bit magnitude comparator using reversible logic is 76.42% more efficient than the normal 32-bit magnitude comparator.

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