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Modelling and Simulation Analysis of III-V Type Material Double-Gate Tunnel Field Effect Transistor

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Abstract: This work presents a comprehensive analysis of Double-Gate Tunnel Field-Effect Transistors (DG-TFETs) employing III-V semiconductor materials, utilizing the Non-Equilibrium Green's Function (NEGF) formalism. TFETs, which operate based on quantum tunneling mechanisms, offer promising solutions for low-power electronic applications due to their potential for achieving steep subthreshold swings and high ON-state currents. The NEGF formalism, known for its robustness in modeling quantum transport phenomena, is applied to study the performance of DG-TFETs with III-V materials such as GaAs and InP, which are known for their high electron mobility and narrow bandgaps. Key performance metrics, including ON-state current (I_{ON}) and OFF-state current (I_{OFF}) are evaluated by utilizing different gate metal work functions. Our analysis demonstrates that electric field and drain current of III-V DG-TFETs exhibit significantly improved I_{ON} and reduced I_{OFF} through optimized band alignment. All simulation have been carried out using the SILVACO technology computer aided design (TCAD) tool.

Keywords: Double-Gate Tunnel Field Effect Transistor (DG-TFET), Non-Equilibrium Green's Function (NEGF), Work function, ON-State current, OFF-State current, Doping concentration.

I. INTRODUCTION

The evolution of Very Large Scale Integration (VLSI) technology has consistently aimed at creating smaller, more energy-efficient, and higher-performing electronic components. Within this dynamic landscape, Tunnel Field-Effect Transistors (TFETs) have emerged as a promising avenue for achieving breakthroughs in power efficiency and reduced leakage currents. This project delves into the intersection of TFETs and the VLSI era, exploring the potential of these novel transistors to reshape the landscape of integrated circuits.

As the VLSI era pushes the boundaries of semiconductor miniaturization and performance, alternative transistor designs are being investigated, with TFETs standing out. Unlike traditional transistors, TFETs operate based on quantum tunnelling, providing a unique method of current modulation that can address some of the power challenges faced by conventional designs.

The Parabolic approximation method is utilized to tackle the 2-D Poisson condition with appropriate device boundary conditions and logical articulations for surface potential and electric fields for Triple Material Quadruple Gate (TMQG) Tunnel Field Effect Transistor are determined [1]. By improving the gate engineering over the channel area, the device ON current is improved Surface Potential and electric field are obtained by solving the Poisson's equation and parabolic approximation method is used to build the precise structure constructed by the combination of tri–gate engineering and triple material gate TFET model is analysed [8].

Cavities in the gate oxide of the TFET are created to form dual-cavity (DC) HJ-STFET structure contain biomolecules of GaSb/GaAs type-III hetero-junction TFET on SELBOX substrate (HJ-STFET)-based dielectric modulated ultrasensitive label-free biosensor has been demonstrated [2]. High-performance pocket-DG-JLTFET is designed with bio sensing the cavity region [5]. This device structure is designed with the same type of doping in source and drain regions and channel as intrinsic forms a junction-less heavily doped TFET. High dielectric permittivity material along with vacuum based dual material junction-less transistor with surrounding gate (DUM-HIK-VAC-JLSG-MOSFET) are proposed [4]. An analytical model for 12nm germanium based triple - material surrounding - gate junction-less tunnel FET resembles to be the assuring device for low-power design of 6T SRAM [9].

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The Double Gate, Tri-Gate, and Hetero-junction TFET structures have been compared and suggested a systematic survey and overview of various device architectures for Hetero-junction TFET [6]. It examines and evaluates parameters such as the ION/ IOFF ratio, channel length (L), sub-threshold swing (SS), and the cut-off frequency of various interface architectures. A novel stack gate-oxide junction-less double-gate tunnel field effect transistor with low work-function live strip (LWLS-SGO-JL-TFET) has been investigated [7]. The benefits of including a stacked oxide layer of high-k dielectric and SiO2 has been studied by comparing the Ids-Vgs curves of TMGSO TFET with TMG Single Oxide TFET, it can be observed that there is an improvement in ION-IOFF ratio in TMGSO TFET [10]. Hetero-junction Tunnel Field Effect Transistor (TFET) with dual gate material is designed with narrow bandgap semiconductor material InGaAs (0.74 eV) at source region and wider energy bandgap InP (1.34 eV) at channel and drain regions [11]. The simulation results show significant improvement in ON current (10^{-5}A/μm) and reduced OFF current (10^{-12}A/μm). Hetero-junction structure that exhibits lesser band-gap between source and intrinsic region, which leads to the improvement in ON-current. The presence of HfO2 placed over a SiO2 acting as a stack causes a significant improvement in the performance of surface potential [14].

Triple material double gate Tunnel Field Effect Transistor (TM-DG TFET) with hetero-junction formed by germanium and silicon materials in the source-channel junction and hetero-dielectric gate stack is used with Silicon Dioxide (SiO2) and Hafnium Dioxide (HfO2) as dielectric materials [12]. The influence of trap carriers at the Si-SiO2 interface near the source channel junction is analysed and the drain current is computed using the analytical model and it is expanded for constructing the SiO2/HfO2 cylindrical gate tunnel FET [13]. A gate-all-around InAs–Si vertical tunnel field-effect transistor with a triple metal gate (VTG-TFET) obtained improved switching characteristics of the improved electrostatic control on the channel and the narrow bandgap source [3].The motivation behind incorporating TFETs into VLSI circuits lies in their inherent capability to operate at lower power levels. As the industry confronts escalating demands for energy-efficient electronics, TFETs present a compelling solution, leveraging quantum tunnelling phenomena to facilitate electron transport with reduced energy barriers. This works aims to provide a comprehensive understanding of the integration of TFETs in the VLSI landscape. From the theoretical foundations of TFET operation to the practical challenges and opportunities in the fabrication processes and exploration encompasses the diverse facets of this transformative synergy. To navigate the intricate details of material selection, hetero-junction engineering, and the potential scalability of TFETs seek to uncover insights that could drive the future trajectory of semiconductor technology.

II. DEVICE STRUCTURE AND SIMULATION SETUP

The 2D schematic view of Double Gate Tunnel Field Effect Transistor is shown in fig. 1. In this structure, the source and intrinsic are (P^+region), while, drain is (N^+). The detailed technical parameters used to simulate DG-TFET are given in Table 1. The source region of a TFET is typically heavily doped with impurities to create a high concentration of charge carriers. This is necessary to enhance the tunnelling current, which is the primary mechanism of current flow in TFET. When level variation due to fact that the tunnelling takes place between source and intrinsic channel region, which results increasing source doping level improves the ON-current and decrease the threshold value. Since, the barrier potential of the device in the drain junction is the critical parameter determining the OFF-current, the impact of the source doping variation on leakage current is minimal. When decreasing source-channel junction barrier leads to electric field high.

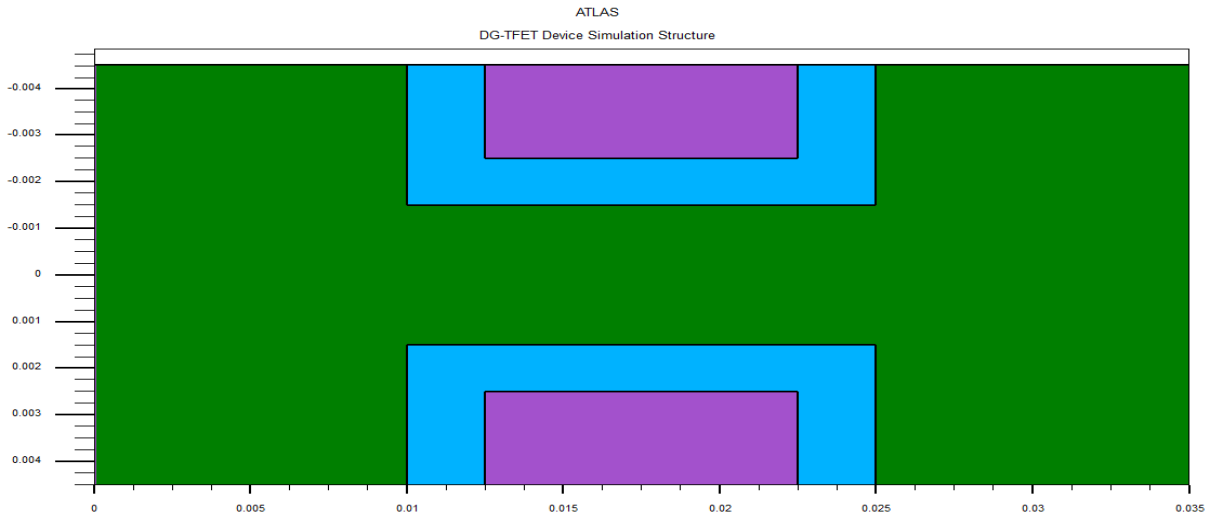

Fig. 1. 2D Schematic view of DG-TFET

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Table 1 DG-TFET design parameter for simulation

S.No	PARAMETER	VALUE (nm)
1.	Channel length	15
2.	Gate length	15
3.	Source length	10
4.	Drain length	10
5.	Silicon body thickness	10
6.	Gate oxide thickness	2
7.	Buried oxide thickness	1

The drain region is typically doped with the same type of impurities as the channel but with a different concentration. The primary role of the drain doping is to collect the charge carriers that have tunnelled through the channel from the source. It also helps in defining the electric field distribution within the device, which influence the overall performance of the TFET. Properly designed drain doping ensures efficient collection of carriers and minimizes unwanted leakage currents. Electrical parameters are less sensitive to the drain doping fluctuations reason, the effective junction for the band to band tunnelling (source-channel). When decreasing the drain doping level ON-state current improves and threshold value decreases. When drain doping level increases ON-state current decreases and threshold value decreases.

The body thickness is an important parameter that can significantly affect the device's performance. Electrostatic control is related to body thickness. A thinner body improves the gate's electrostatic control over the channel, reducing short-channel effect and enhancing sub-threshold swing. It helps in maintaining an abrupt off-state, which is important for low leakage currents. A thinner gate oxide improves the gate control over the channel, reducing short-channel effects and enhancing sub-threshold swing. This results in better control of the channel potential and minimizes leakage current. A thicker gate oxide reduces gate capacitance and can lead to weaker electrostatic control, potentially increasing OFF-state leakage and deteriorating sub-threshold swing. The channel length in a Tunnel Field-Effect Transistor (TFET) significantly influences the device's performance, including its electrostatic control, sub-threshold swing, leakage currents and overall switching characteristics. When channel length increases results in low ON-state current and leakage current and also high threshold voltage. To justify this behaviour, carrier transport experience two mechanisms of scattering and transmission. Total transmission of the transistor may be

$$T_{tot} = \frac{T_{BTBT} T_{Scat}}{T_{BTBT} + T_{Scat} - T_{BTBT} T_{Scat}} \quad (1)$$

$$T_{Scat} = \frac{L_{mfp}}{L_{mfp} + L_G} \quad (2)$$

Where, T_{tot} is a total transmission of transistor.
T_{Scat} is a transmission related to scattering in channel.
T_{BTBT} is a band-to-band tunnelling transmission of channel.
L_{mfp} is a scattering mean free path (nm).
L_G is a channel length of the transistor.

Maximum value of tunnelling probability is one. For this value, assuming T_{Scat} is small, Denominator of equation 1 become close to one making T_{tot} and hence, current is propagation to T_{Scat}. When T_{Scat} is proportional to $1/L_G$, Current becomes inversely proportional to channel length.

III. RESULTS AND DISCUSSION

The modelling of the double gate tunnel field effect transistor is carried out by assigning a length of 15nm. The doping concentration of Source is $1x10^{18}$ cm^{-3}, Channel $5x10^{17}$ cm^{-3} and Drain $1x10^{19}$ cm^{-3}. By employing different doping materials, a homostructure results. In this work, to increase the transmission of electron from source to intrinsic region GaAs and InP semiconductor materials are used as a doping materials. To verify the accuracy of performance of the device with different gate metal work function, two dimensional device simulation has been performed by using SILVACO TCAD tool. The models available in TCAD tool to simulate band-to-band tunneling are Kane's Band-to-Band model, Hurkx's Band-to-Band model, Schenk's Band-to-Band model, the Dynamic Non-Local Band-to-Band model, Auger Recombination model (AR), Shockley-Read-Hall (SRH), Non-Equilibrium Green's Function model, SRH Generation-Recombination model (GR). In our work the Non-Equilibrium Green's Function model is used to evaluate the transmission of electron rate to improve ON-state current.

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Fig. 2 Indicates the effect of the Electric field of GaAs based DG-TFET using gate work function (Cobalt=5.0eV) for channel length 15nm and Fig. 3 indicates the effect of the gate-source voltage on the electron mobility over the channel of GaAs based DG-TFET using gate work function (Cobalt=5.0eV). Fig. 4 shows I-V characteristic of GaAs based DG-TFET using work function (Cobalt=5.0eV) by applying Vgs=0.4V and doping concentration of Source ($1x10^{18}$ cm^{-3}), Channel ($5x10^{17}$ cm^{-3}),and Drain ($1x10^{19}$ cm^{-3}).The x-axis which plot gate voltage (linear scale) and y-axis which plot drain current (log scale). Which results $I_{ON}=10^{-3}$ A/µm, $I_{OFF}=10^{-19}$ A/µm and the ratio of $I_{ON}/I_{OFF} = 10^{16}$ is obtained.

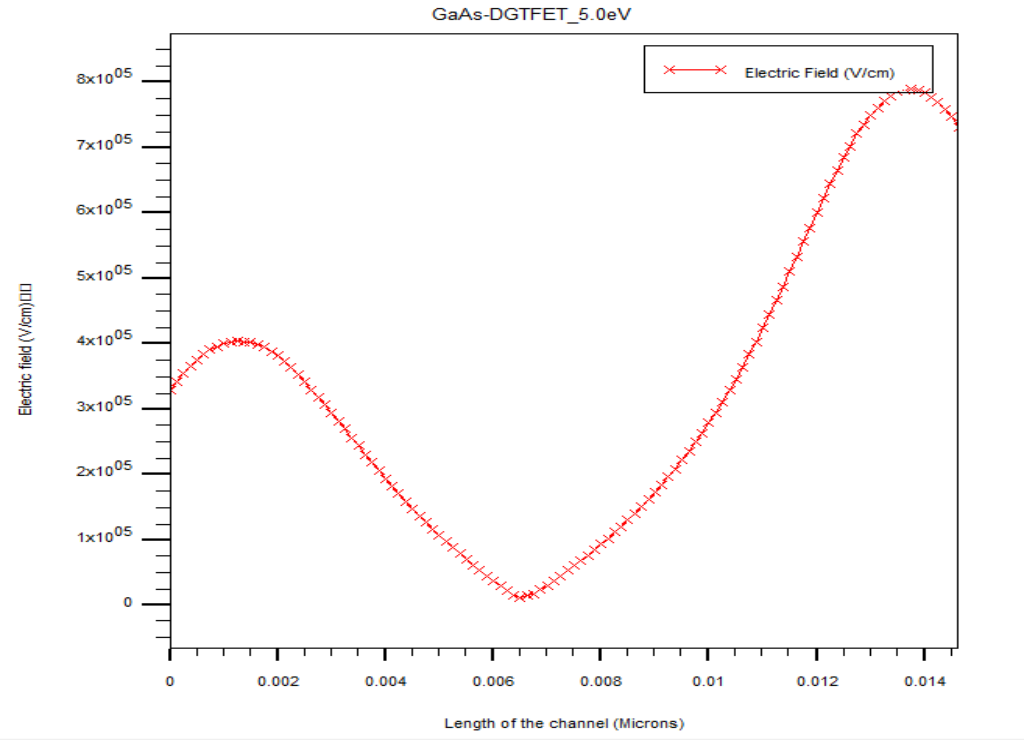

Fig. 2 The effect of lateral electric field of GaAs based DG-TFET using gate work function (Cobalt=5.0eV) for channel length 15nm.

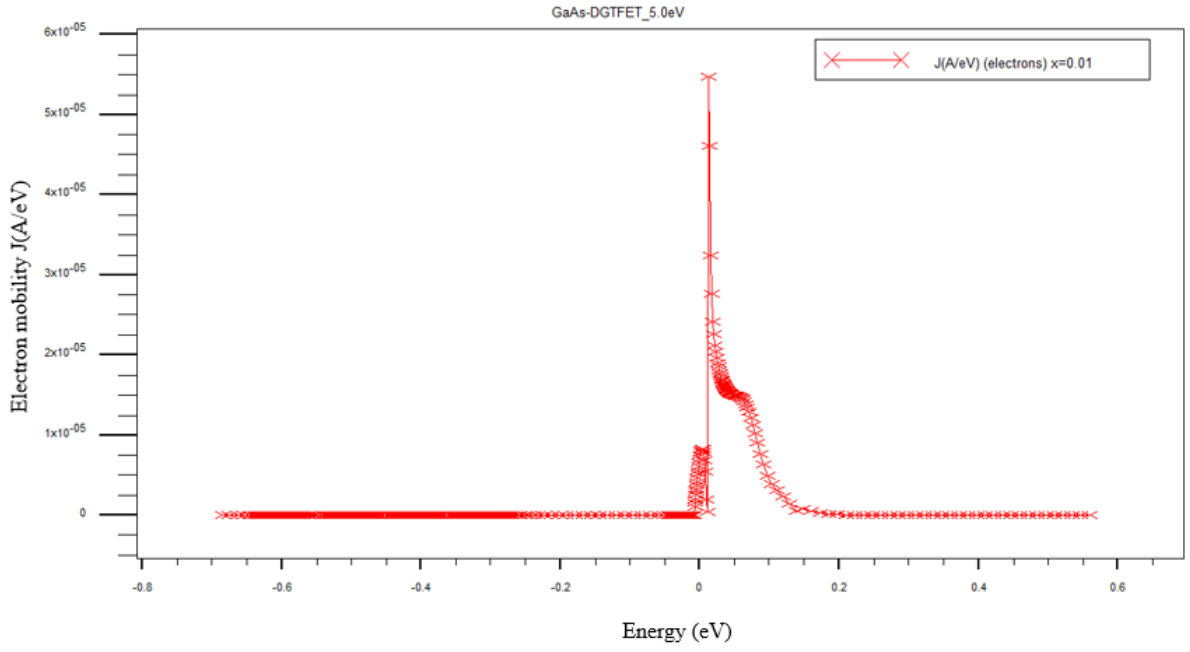

Fig. 3 The effect of electron mobility of GaAs based DG-TFET using gate work function (Cobalt=5.0eV).

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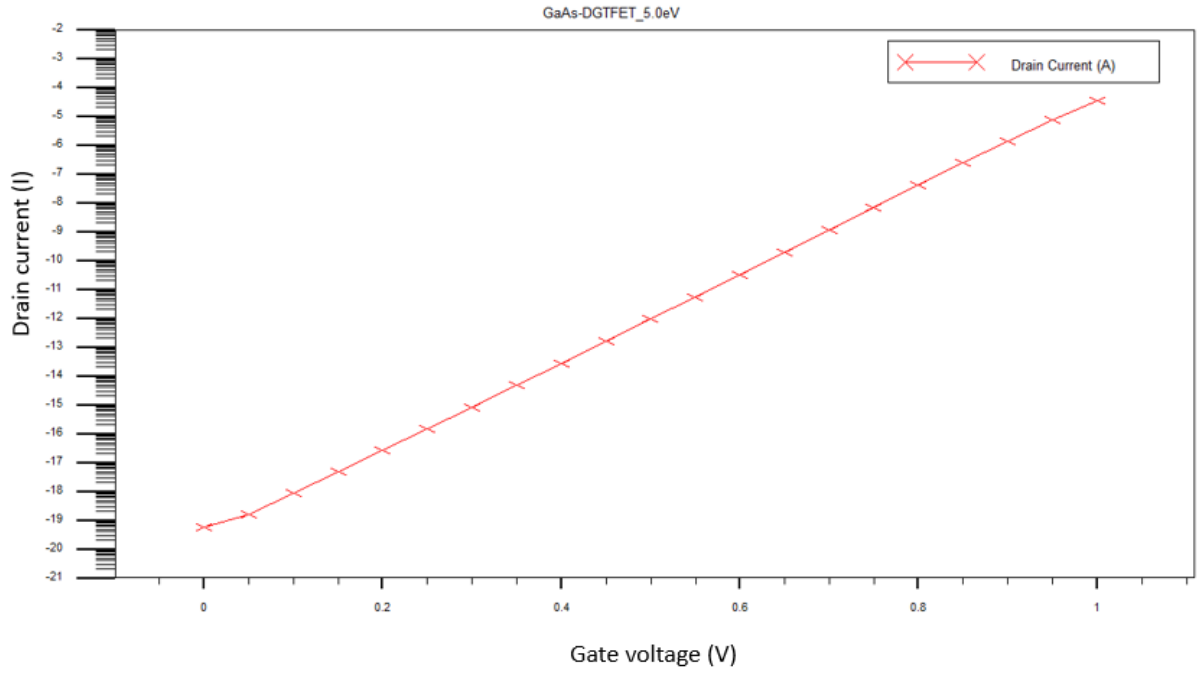

Fig. 4 The transfer characteristic of the drain current (Id) versus the gate voltage (Vgs) of GaAs based DG-TFET using gate work function (Cobalt=5.0eV).

Fig. 5 Indicates the effect of the Electric field of GaAs based DG-TFET using gate work function (Copper=4.7eV) for channel length 15nm and Fig. 6 indicates the effect of the gate-source voltage on the electron mobility over the channel of GaAs based DG-TFET using gate work function (Copper=4.7eV). Fig. 7 shows I-V characteristic of GaAs based DG-TFET using work function (Copper=4.7eV) by applying Vgs=0.4V and doping concentration of Source ($1x10^{18}$ cm^{-3}), Channel ($5x10^{17}$ cm^{-3}), and Drain ($1x10^{19}$ cm^{-3}).The x-axis which plot gate voltage (linear scale) and y-axis which plot drain current (log scale).Which results $I_{ON}=10^{-3}$ A/µm, $I_{OFF}=10^{-15}$ A/µm and the ratio of I_{ON} / I_{OFF} = 10^{12} is obtained.

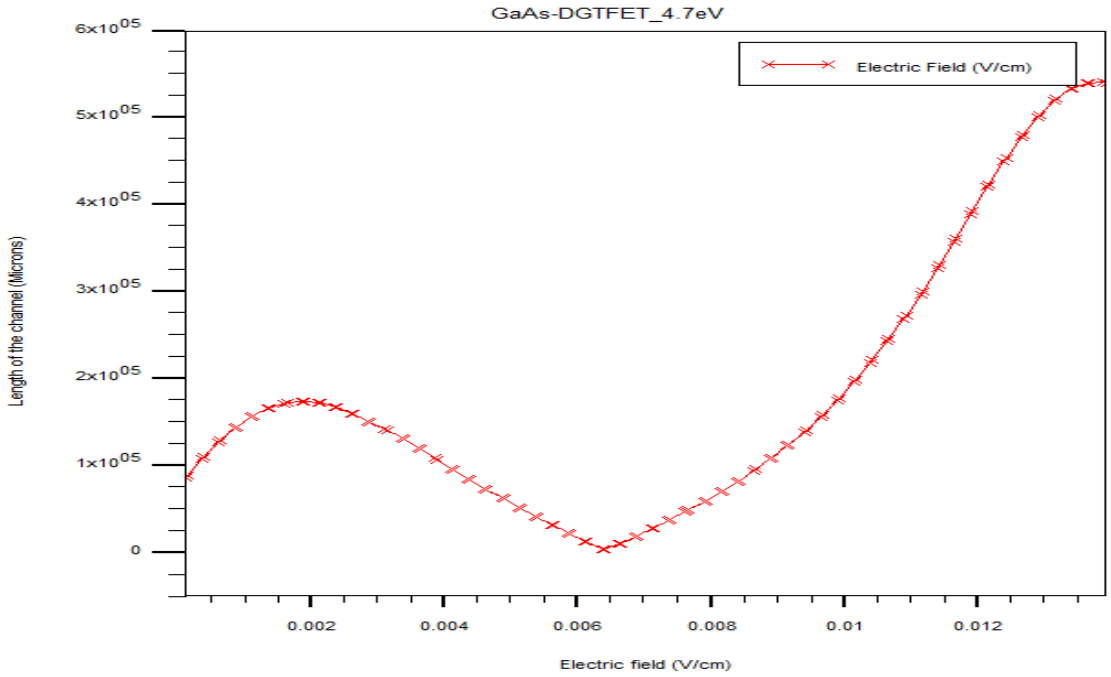

Fig. 5 The effect of lateral electric field of GaAs based DG-TFET using gate work function (Copper=4.7eV) for channel length 15nm.

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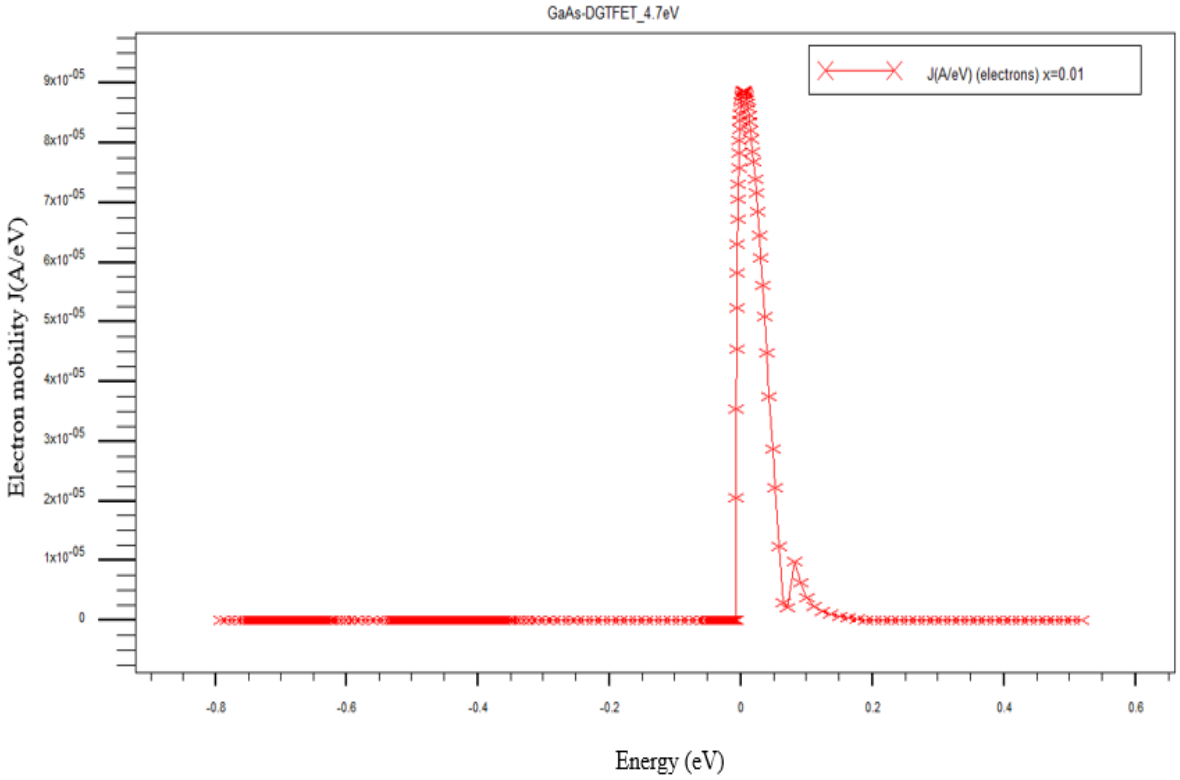

Fig. 6 The effect of electron mobility of GaAs based DG-TFET using gate work function (Copper=4.7eV).

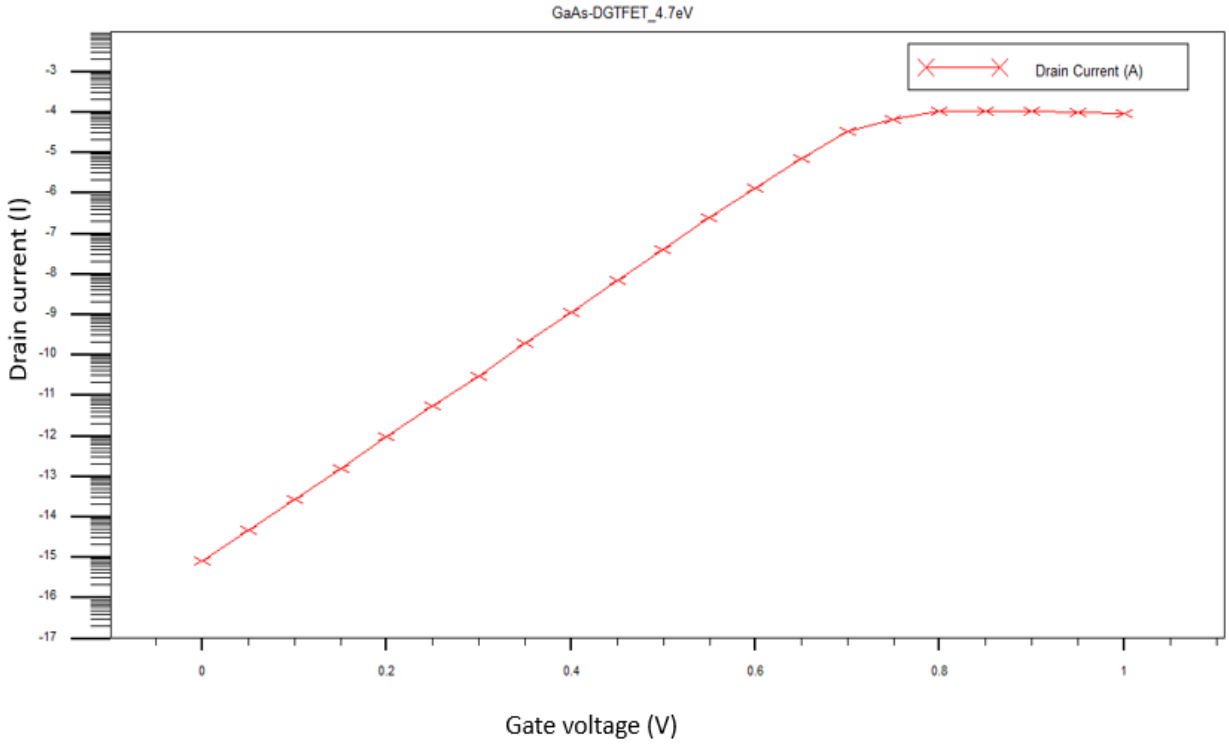

Fig. 7 The transfer characteristic of the drain current (Id) versus the gate voltage (Vgs) of GaAs based DG-TFET using gate work function (Copper=4.7eV).

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Fig. 8 Indicates the effect of the Electric field of GaAs based DG-TFET using gate work function (Gold=5.1eV) for channel length 15nm and Fig. 9 indicates the effect of the gate-source voltage on the electron mobility over the channel of GaAs based DG-TFET using gate work function (Gold=5.1eV). Fig. 10 shows I-V characteristic of GaAs based DG-TFET using work function (Gold=5.1eV) by applying Vgs=0.4V and doping concentration of Source ($1x10^{18}$ cm^{-3}), Channel ($5x10^{17}$ cm^{-3}),and Drain ($1x10^{19}$ cm^{-3}).The x-axis which plot gate voltage (linear scale) and y-axis which plot drain current (log scale). Which results I_{ON} =10^{-5} A/µm, I_{OFF} =10^{-19} A/µm and the ratio of I_{ON}/I_{OFF} = 10^{14} is obtained.

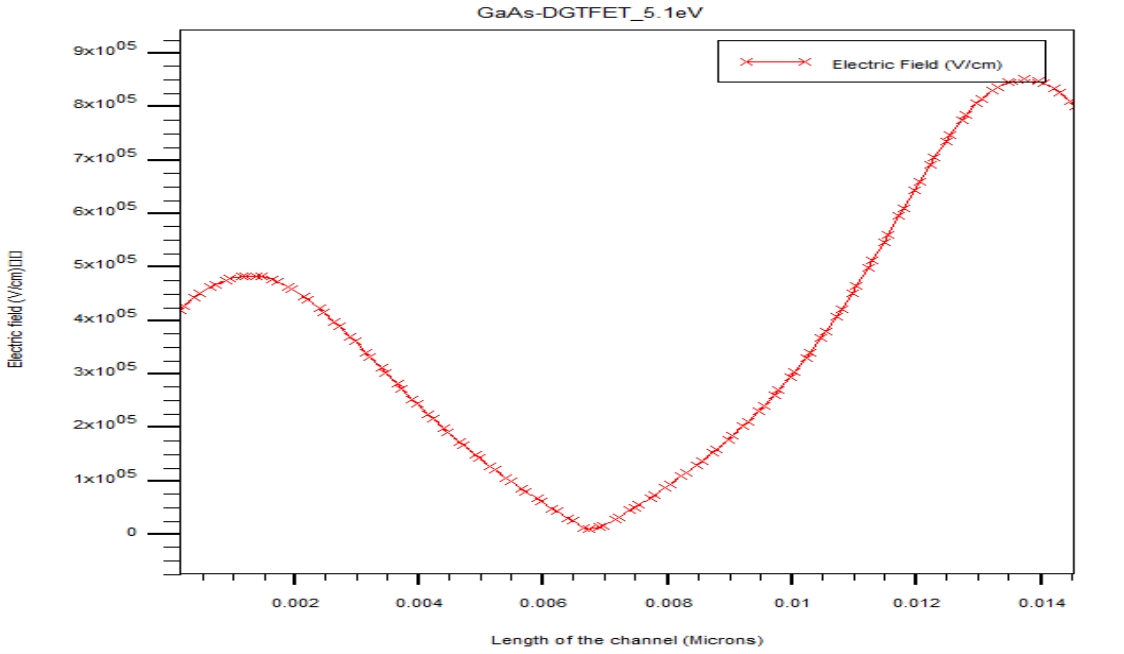

Fig. 8 The effect of lateral electric field of GaAs based DG-TFET using gate work function (Gold=5.1eV) for channel length 15nm.

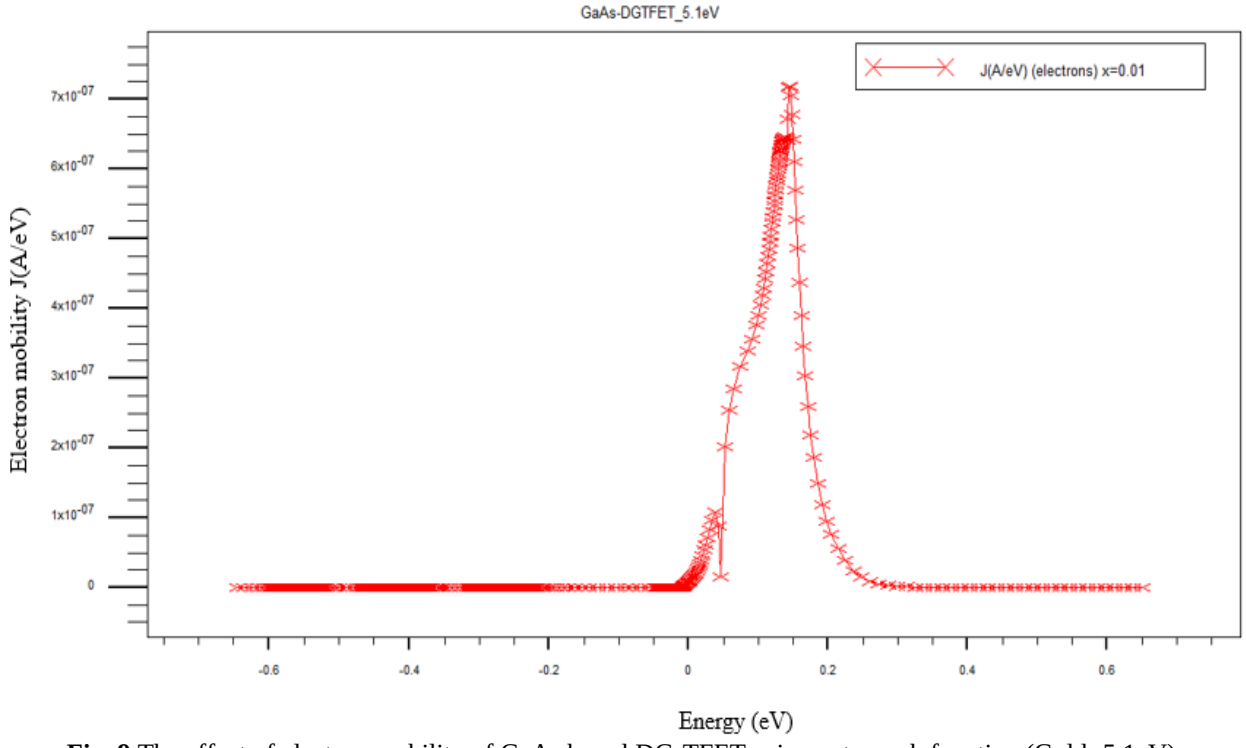

Fig. 9 The effect of electron mobility of GaAs based DG-TFET using gate work function (Gold=5.1eV).

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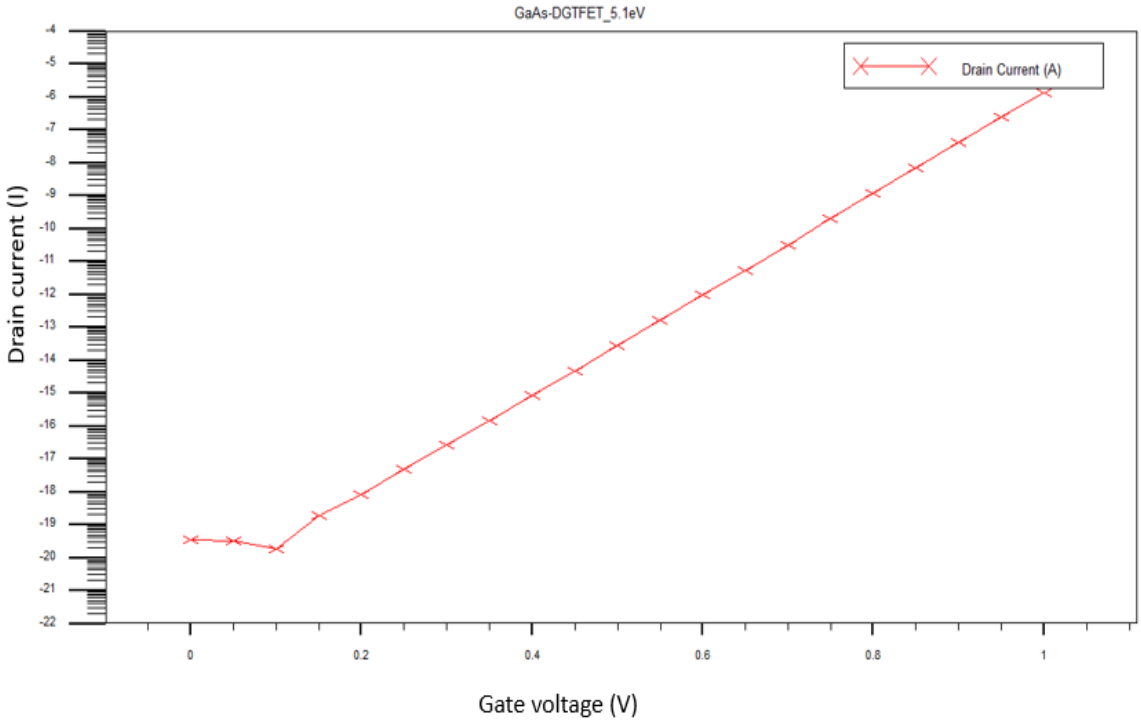

Fig. 10 The transfer characteristic of the drain current (Id) versus the gate voltage (Vgs) of GaAs based DG-TFET using gate work function (Gold=5.1eV).

Fig. 11 Indicates the effect of the Electric field of InP based DG-TFET using gate work function (Cobalt=5.0eV) for channel length 15nm and Fig. 12 indicates the effect of the gate-source voltage on the electron mobility over the channel of InP based DG-TFET using gate work function (Cobalt=5.0eV). Fig. 13 shows I-V characteristic of InP based DG-TFET using work function (Cobalt=5.0eV) by applying Vgs=0.4V and doping concentration of Source ($1x10^{18}$ cm^{-3}), Channel ($5x10^{17}$ cm^{-3}),and Drain ($1x10^{19}$ cm^{-3}).The x-axis which plot gate voltage (linear scale) and y-axis which plot drain current (log scale). Which results I_{ON} =10^{-3} A/µm, I_{OFF} =10^{-14} A/µm and the ratio of I_{ON}/I_{OFF} = 10^{11} is obtained.

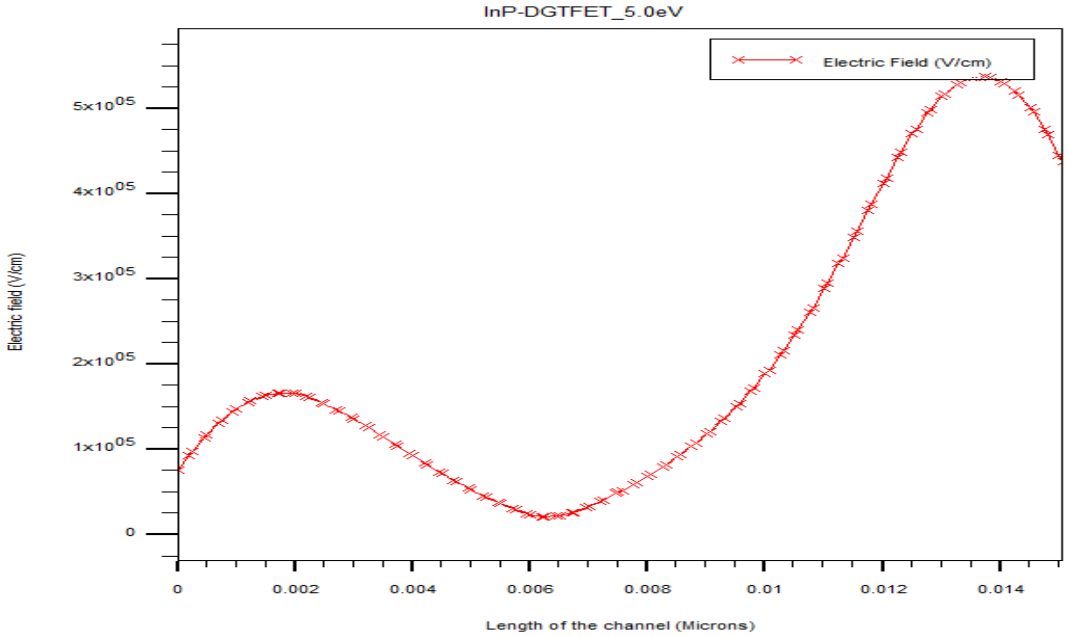

Fig. 11 The effect of lateral electric field of InP based DG-TFET using gate work function (Cobalt=5.0eV) for channel length 15nm.

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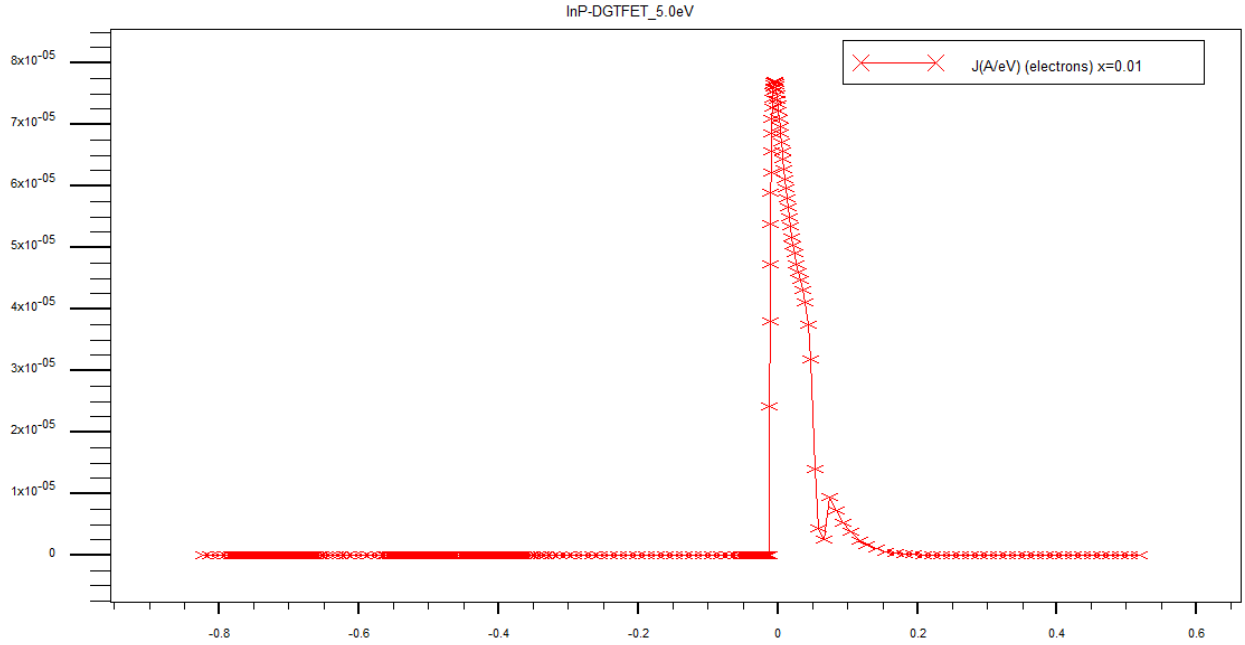

Fig. 12 The effect of electron mobility of InP based DG-TFET using gate work function (Cobalt=5.0eV).

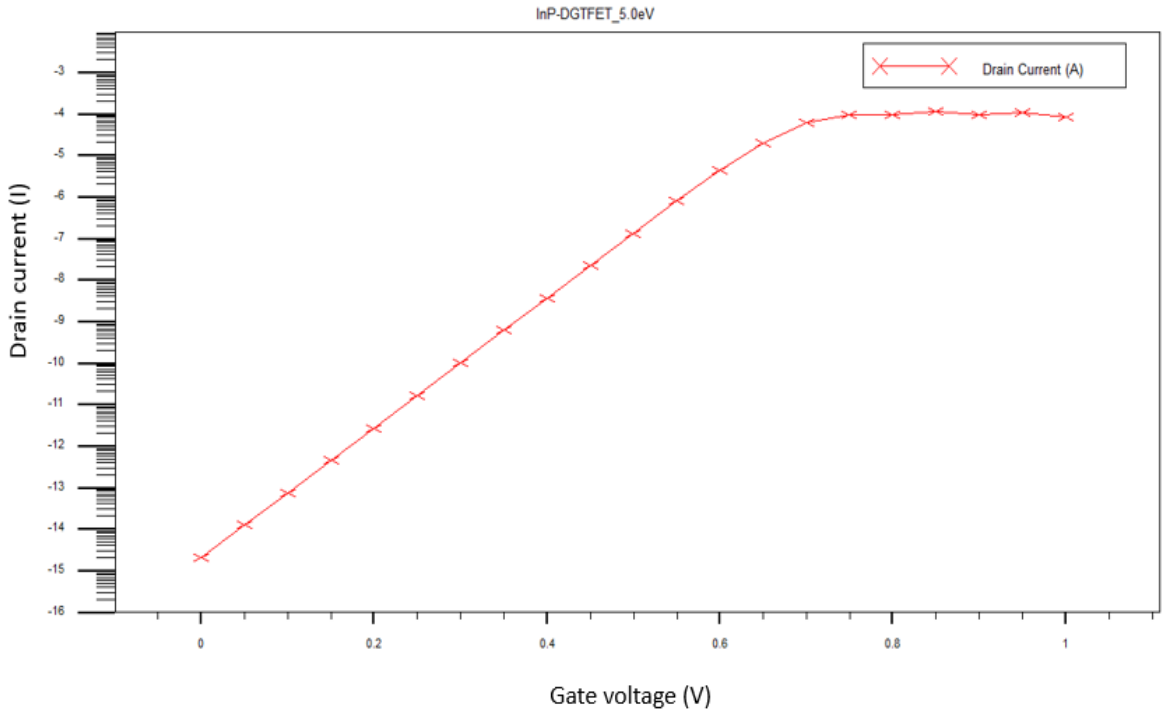

Fig. 13 The transfer characteristic of the drain current (Id) versus the gate voltage (Vgs) of InP based DG-TFET using gate work function (Cobalt=5.0eV).

Fig. 14 Indicates the effect of the Electric field of InP based DG-TFET using gate work function (Copper=4.7eV) for channel length 15nm and Fig. 15 indicates the effect of the gate-source voltage on the electron mobility over the channel of InP based DG-TFET using gate work function (Copper=4.7eV). Fig. 16 shows I-V characteristic of InP based DG-TFET using work function (Copper=4.7eV) by applying Vgs=0.4V and doping concentration of Source ($1x10^{18}$ cm^{-3}), Channel ($5x10^{17}$ cm^{-3}),and Drain ($1x10^{19}$ cm^{-3}).The x-axis which plot gate voltage (linear scale) and y-axis which plot drain current (log scale). Which results I_{ON} =10^{-3} A/µm, I_{OFF} =10^{-9} A/µm and the ratio of I_{ON}/I_{OFF} = 10^{6} is obtained.

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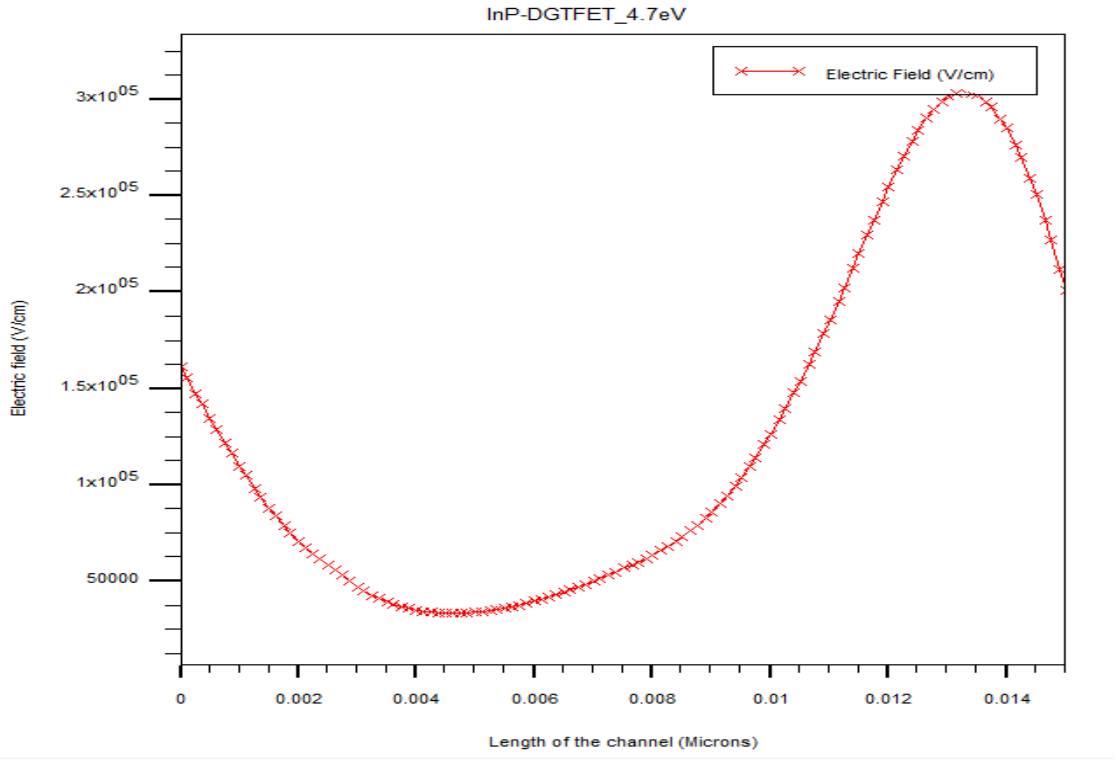

Fig. 14 The effect of lateral electric field of InP based DG-TFET using gate work function (Copper=4.7eV) for channel length 15nm.

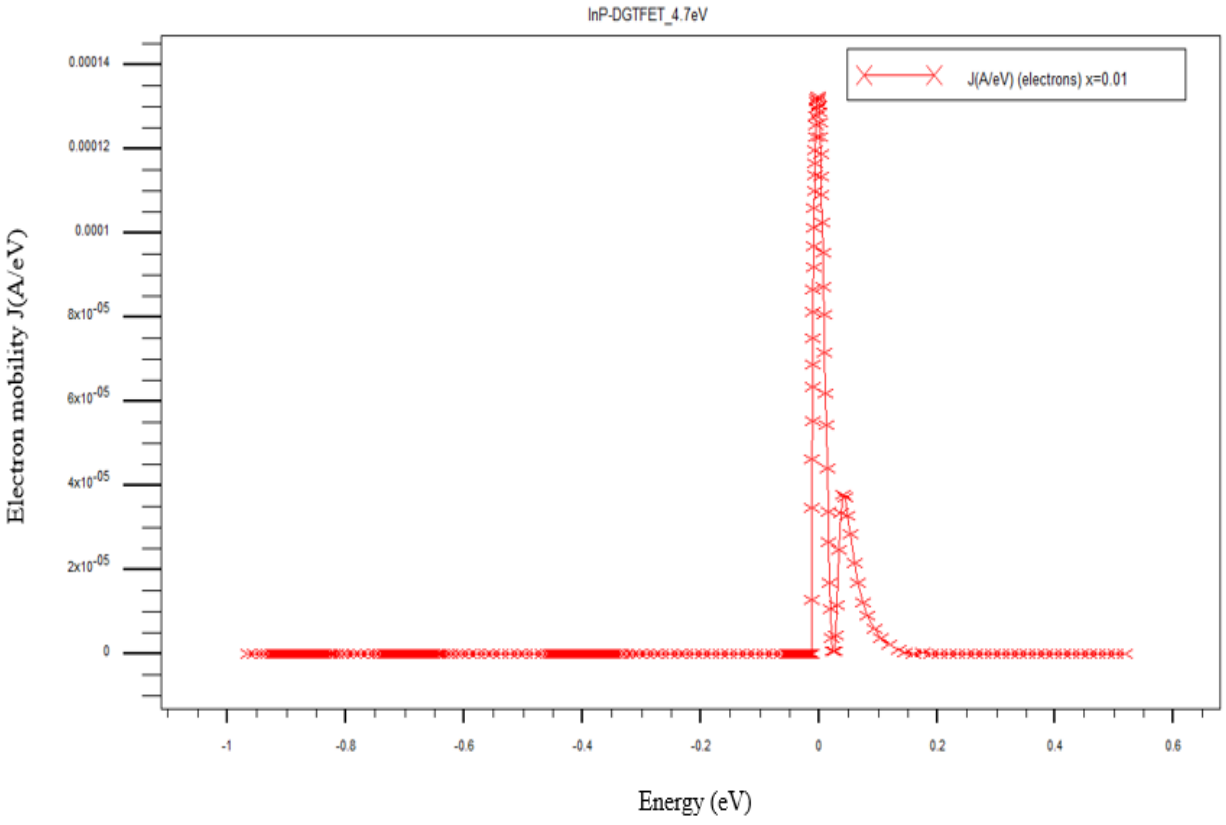

Fig. 15 The effect of electron mobility of InP based DG-TFET using gate work function (Copper=4.7eV).

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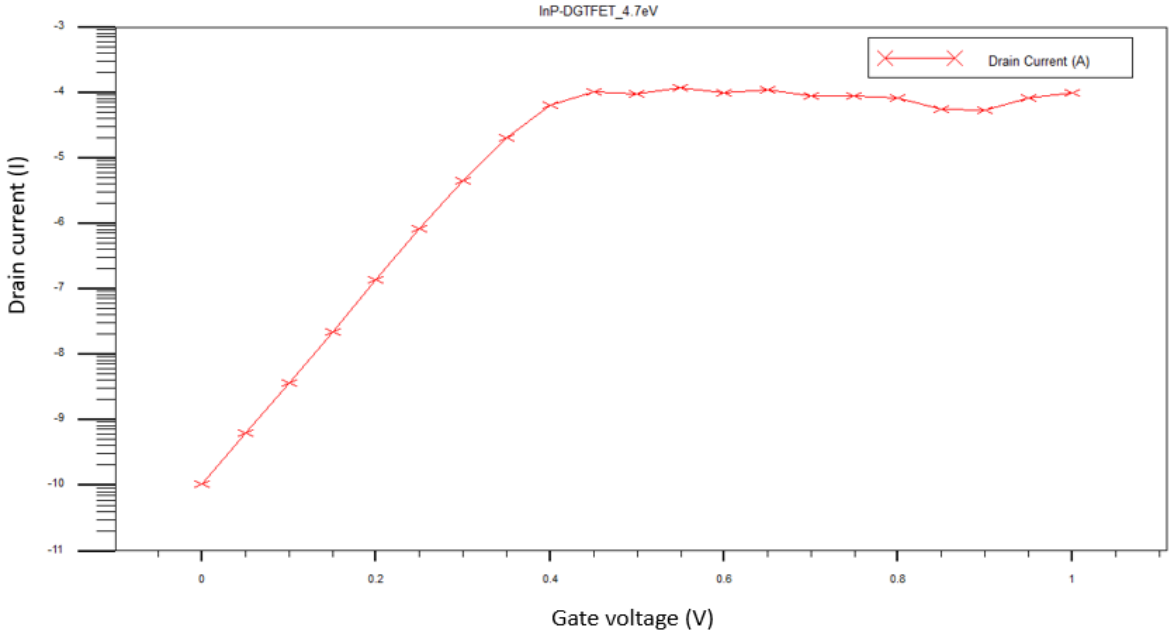

Fig. 16 The transfer characteristic of the drain current (Id) versus the gate voltage (Vgs) of InP based DG-TFET using gate work function (Copper=4.7eV).

Fig. 17 Indicates the effect of the Electric field of InP based DG-TFET using gate work function (Gold=5.1eV) for channel length 15nm and Fig. 18 indicates the effect of the gate-source voltage on the electron mobility over the channel of InP based DG-TFET using gate work function (Gold=5.1eV). Fig. 19 shows I-V characteristic of InP based DG-TFET using work function (Gold=5.1eV) by applying Vgs=0.4V and doping concentration of Source ($1x10^{18}$ cm^{-3}), Channel ($5x10^{17}$ cm^{-3}),and Drain ($1x10^{19}$ cm^{-3}).The x-axis which plot gate voltage (linear scale) and y-axis which plot drain current (log scale). Which results I_{ON} =10^{-5} A/µm, I_{OFF} =10^{-11} A/µm and the ratio of I_{ON}/I_{OFF} = 10^{6} is obtained.

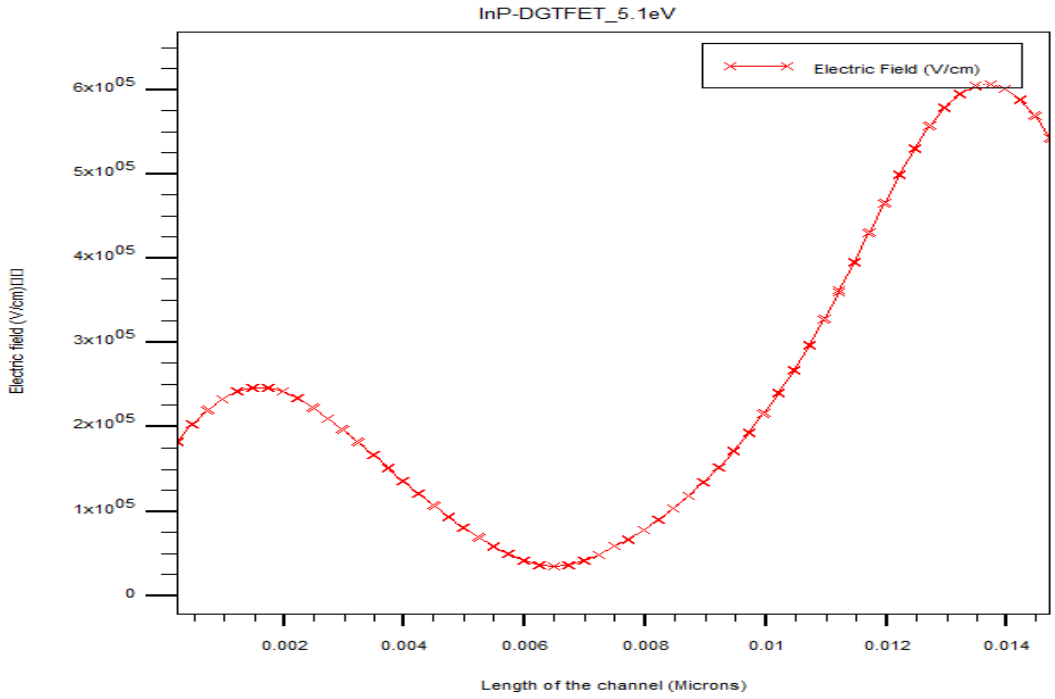

Fig. 17 The effect of lateral electric field of InP based DG-TFET using gate work function (Gold=5.1eV) for channel length 15nm.

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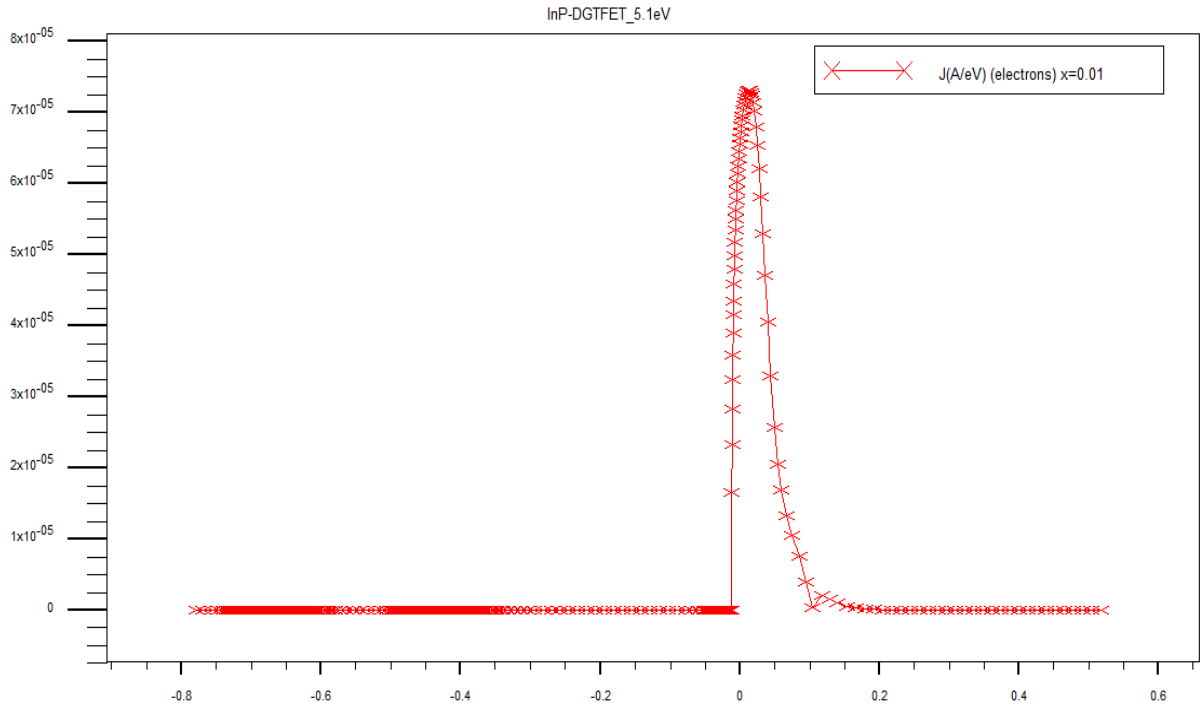

Fig. 18 The effect of electron mobility of InP based DG-TFET using gate work function (Gold=5.1eV).

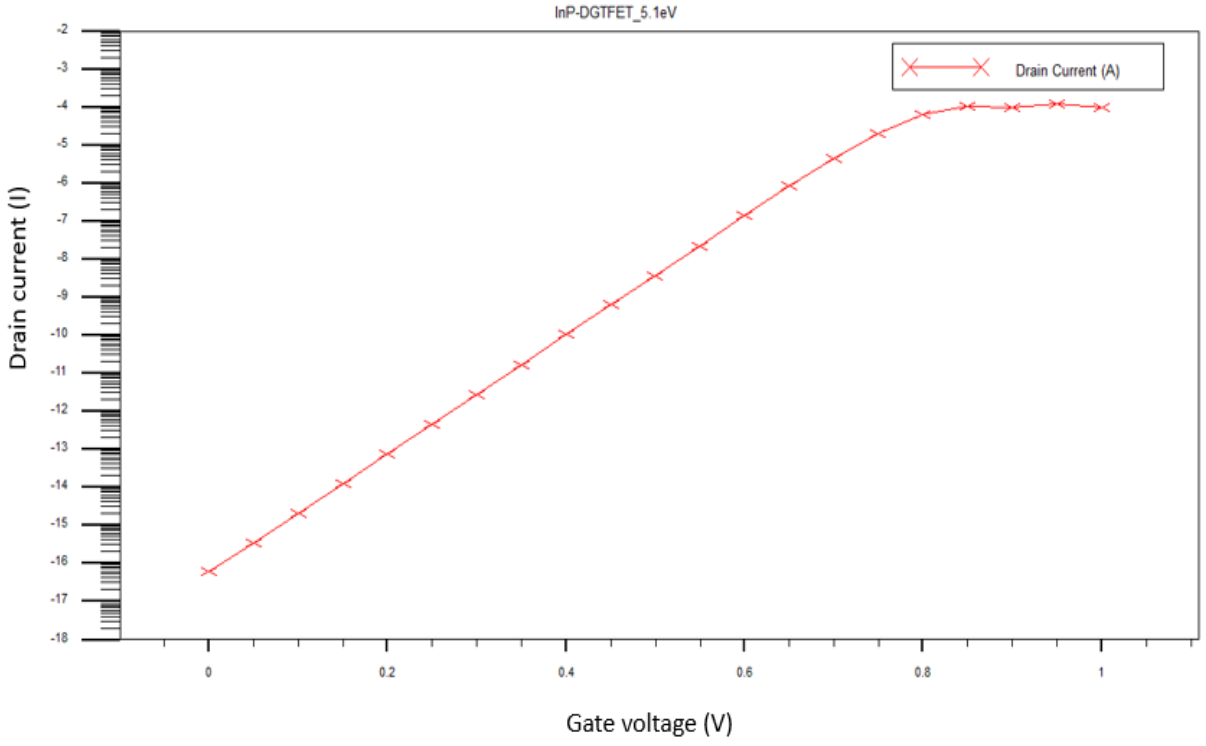

Fig. 19 The transfer characteristic of the drain current (Id) versus the gate voltage (Vgs) of InP based DG-TFET using gate work function (Gold=5.1eV).

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Table 2 Comparison table of GaAs and InP semiconductor material based DG-TFET I-V characteristics using Non-Equilibrium Green's Function Model.

S.No	METAL (Work Function)	GaAs Material			InP Material		
		I_{OFF} A/μm	I_{ON} A/μm	I_{ON} / I_{OFF} Ratio	I_{OFF} A/μm	I_{ON} A/μm	I_{ON} / I_{OFF} Ratio
1.	Cobalt (5.0eV)	10^{-19}	10^{-3}	10^{16}	10^{-14}	10^{-3}	10^{11}
2.	Copper (4.7eV)	10^{-15}	10^{-3}	10^{12}	10^{-9}	10^{-3}	10^{6}
3.	Gold (5.1eV)	10^{-19}	10^{-5}	10^{14}	10^{-16}	10^{-3}	10^{13}

From the comparison of GaAs and InP semiconductor material based DG-TFET I-V Characteristics using Non-Equilibrium Green's Function Model, using following work functions of Cobalt=5.0eV, Copper=4.7eV, Gold=5.1eV by applying V1=0.4,V2=0.0, Vstep=0.05,Vfinal=1.0 and doping concentration of Source is $1x10^{18}$ cm^{-3}, Channel $5x10^{17}$ cm^{-3} and Drain $1x10^{19}$ cm^{-3}. The above results shows gate metal work function (5.0eV) and gate metal work function (4.7eV) for both GaAs and InP ON-state current is high (10^{-3}), but very low leakage current for GaAs than leakage current to InP. Also, gate work function (5.1eV) shows high ON-state current for InP (10^{-3}) than ON-state current of GaAs (10^{-3}).

IV. CONCLUSION

The Double gate Tunnel FET characteristics of Drain current versus Gate voltage in variation with doping concentration of Source is $1x10^{18}$ cm^{-3}, Channel $5x10^{17}$ cm^{-3} and Drain $1x10^{19}$ cm^{-3} from the respective ON-state current and OFF-state current is analysed by comparing the GaAs and InP based semiconductor material using different gate metal work function to calculate ON and OFF current ratio to achieve the improved ON current and their electric field in the SILVACO TCAD simulation tool. Which results $I_{ON}/I_{OFF} = 10^{16}$ for GaAs and $I_{ON}/I_{OFF} = 10^{11}$ for InP using work function 5.0eV, $I_{ON}/I_{OFF} = 10^{12}$ for GaAs and $I_{ON}/I_{OFF} = 10^{6}$ for InP using work function 4.7eV, $I_{ON}/I_{OFF} = 10^{14}$ for GaAs and $I_{ON}/I_{OFF} = 10^{13}$ for InP using work function 5.1eV. When increasing value of gate metal work function range the device leakage current is minimizing and have a better ON-state current. From the above achieved results comparing GaAs with InP semiconductor material, GaAs has the better I_{ON} and I_{OFF} ratio. GaAs has improved ON current and low leakage current which improvise the performance of the device. In future the device structure can be modify and develop to find the threshold voltage, sub-threshold voltage, ON-state and OFF-state current ratio for the proposed device. The device structure can be developed and integrated into wearable electronics where long battery life and energy efficient can be lead to significant reduction in power consumption, making them ideal for battery-operated devices and IOT applications. Gallium and Indium-based TFET can be employed in RF circuits for wireless communication, offering advantages in terms of power efficiency and frequency response.

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