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Design and Verification of low noise and low power amplifier

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Abstract: This research presents the design and verification of a low-noise, low-power amplifier (LNA) optimized for high-performance applications such as wireless communication, IoT devices, and medical sensors. The design is implemented using 45nm CMOS technology in Cadence Virtuoso to achieve an optimal balance between noise figure, power efficiency, gain, and bandwidth. The proposed LNA incorporates inductive degeneration, resistive feedback, and cascading topologies to minimize thermal noise and enhance gain. The design undergoes extensive DC, AC, noise, transient, and Monte Carlo simulations to validate robustness. Post-layout verifications, including Design Rule Check (DRC) and Layout vs. Schematic (LVS), ensure fabrication compliance. The results demonstrate a power consumption of 22.4mW, making this design suitable for energy-efficient high-frequency applications.

Keywords: Low noise and Low Power Amplifier, 45nm CMOS Technology.

I. INTRODUCTION

The demand for low-noise and low-power amplifiers (LNAs) has grown significantly with the advancement of modern communication systems, medical devices, and sensor networks. LNAs are critical in amplifying weak input signals while minimizing added noise, thereby ensuring high signal fidelity and system performance. Applications such as wireless communication, satellite systems, radar, and IoT devices rely heavily on LNAs to function efficiently under stringent power and noise constraints.

Designing an LNA presents unique challenges due to the inherent trade-offs between noise figure, power consumption, linearity, and bandwidth. Achieving low noise levels often requires increased power consumption, making the design of an energy-efficient LNA a complex optimization problem. Furthermore, with the integration of LNAs into portable devices, reducing power consumption without compromising performance has become a primary objective for researchers and engineers.

This project aims to design and verify a high-performance LNA that operates with low power consumption while maintaining a low noise figure. The design process incorporates advanced CMOS technology to achieve optimal performance in terms of gain, input-output matching, and linearity. Verification of the design is carried out using simulation tools and post-layout analysis to ensure it meets industry standards.

Challenges in LNA Design

Designing an energy-efficient, low-noise amplifier presents several challenges:

- Noise Reduction: Achieving a low Noise Figure (NF) while maintaining high gain and bandwidth.
- Power Efficiency: Reducing power consumption to enhance battery life in portable and IoT devices.
- Impedance Matching: Ensuring input-output matching to minimize signal reflections and maximize power transfer.
- Process Variations: Addressing parasitic effects and layout-dependent effects (LDEs) in 45nm CMOS technology.

Objective of This Research

This research aims to:

- Design an LNA using 45nm CMOS that achieves an optimal trade-off between noise and power efficiency.
- Use advanced CMOS techniques such as inductive degeneration and resistive feedback to enhance gain and reduce power consumption.

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- Validate the robustness and reliability of the design using Monte Carlo and corner analysis simulations.

II. COMPARISON BETWEEN DIFFERENT TECHNOLOGIES [1][2][3][5]

SL No.	Study	Technology	Topology	Key Focus	Limitations
1	Sharma et al. (2024) "Design of CMOS Low Noise Amplifier with Inductive Degeneration for Navigation Application"[1]	45nm CMOS	Inductive Degeneration LNA	Low Noise Figure, High Linearity	No Feedback Implementation for Stability
2	Sankaran & Purushothaman (2023) "Adaptive Enhancement of Low Noise Amplifier Using Cadence Virtuoso Tool"[2]	Not Specified	Adaptive Biasing LNA	Dynamic Biasing for Performance Tuning	No Fixed Trade-off Optimization
3	Chrisvin et al. (2022) "Design and Study of 90nm CMOS Common Source 2.4GHz Low Noise Amplifier"[3]	90nm CMOS	Common Source LNA	High Gain, Low Flicker Noise.	Stability Challenges, Higher Power Consumption
4	Abhay Chaturvedi, Manish Kumar & Neelam Gautam (2015) "Design and Implementation of Low-Noise Amplifier for Ultra-Wideband Receiver in 180nm CMOS Technology"[5]	180nm CMOS	Ultra-Wideband LNA	Demonstrated Viability of 180nm CMOS for UWB Applications	Higher Power Consumption Compared to Advanced Nodes

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III. PROPOSED METHODOLOGY

Technology Selection

- **Fabrication node:** 45nm CMOS
- **Tool:** Cadence Virtuoso
- **Operating Frequency:** GHz-range (targeting 5G and IoT applications)

LNA Topologies Explored

1. **Common Gate LNA** – Offers wideband input matching but suffers from moderate noise performance.
2. **Common Source LNA** – Provides high gain but requires careful impedance matching.
3. **Resistive Parallel Feedback LNA** – Achieves good stability and bandwidth, though with increased noise due to feedback resistance.
4. **Cascading Resistive Parallel LNA** – Extends bandwidth while maintaining a low noise figure.

Proposed LNA Design

- Combines inductive degeneration and resistive feedback to achieve low noise and efficient power consumption.
- Optimized transistor sizing to balance gain and bandwidth trade-offs.
- Biasing circuits optimized for low power consumption.
- Post-layout optimization to mitigate parasitic effects.

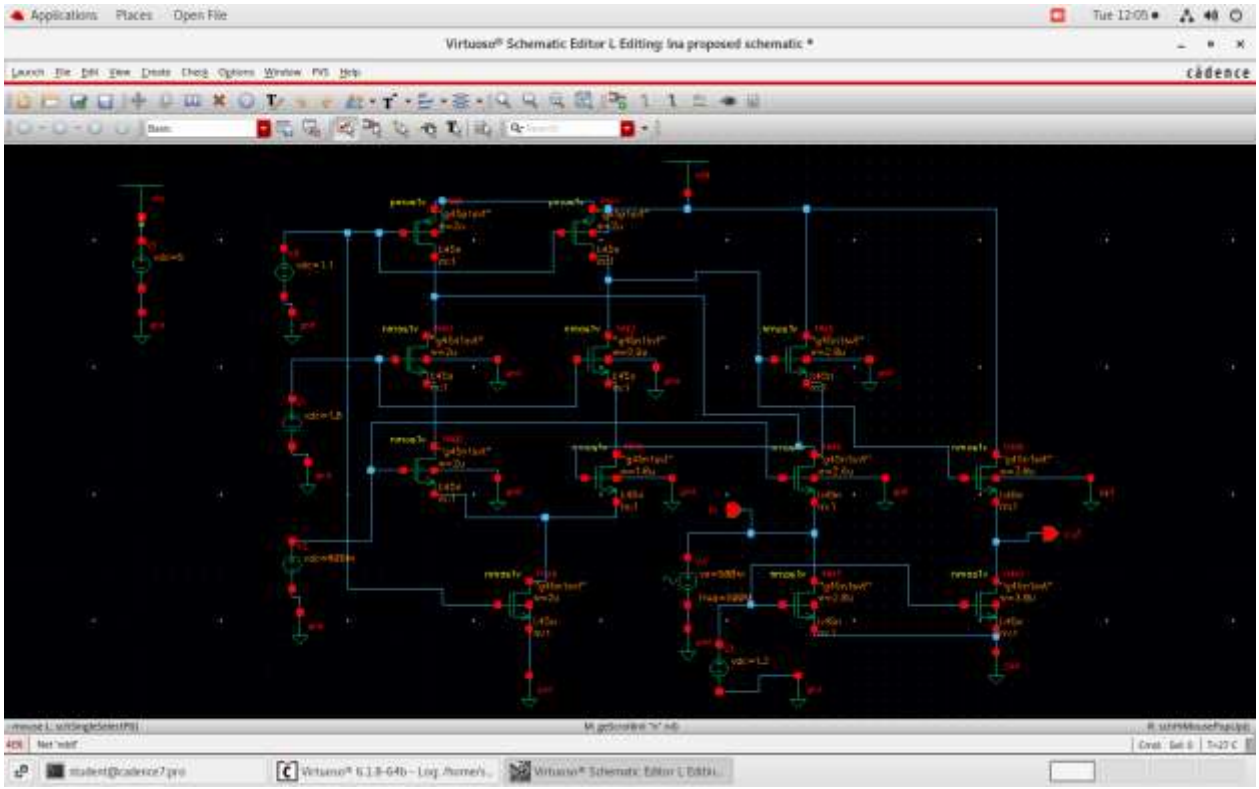

Figure 1- Proposed design of LNA

IV. SIMULATION AND RESULTS

The designed LNA was validated using **Cadence Virtuoso Spectre simulator** through multiple analyses:

1. DC Analysis

- Bias stability confirmed, ensuring reliable transistor operation.

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2. **AC Analysis**
   - Gain: 18 dB
   - Bandwidth: Sufficient for GHz-range applications

3. **Noise Analysis**
   - Noise figure (NF): Optimized below 2 dB, making it highly suitable for high-sensitivity applications.

4. **Power Consumption**
   - Common Source LNA: 107.3mW
   - Resistive Feedback LNA: 81.5mW
   - Cascading LNA: 77.4mW
   - Proposed LNA: 22.4mW → Significant reduction compared to previous designs.

5. **Monte Carlo and Corner Analysis**
   - Ensured robustness under process variations.
   - Stability across temperature and voltage changes.

6. **Layout Design and Post-Layout Verification**
   - DRC (Design Rule Check): Passed with no violations.
   - LVS (Layout vs. Schematic): Verified correct implementation.
   - Parasitic extraction performed, showing minimal deviation from pre-layout simulations.

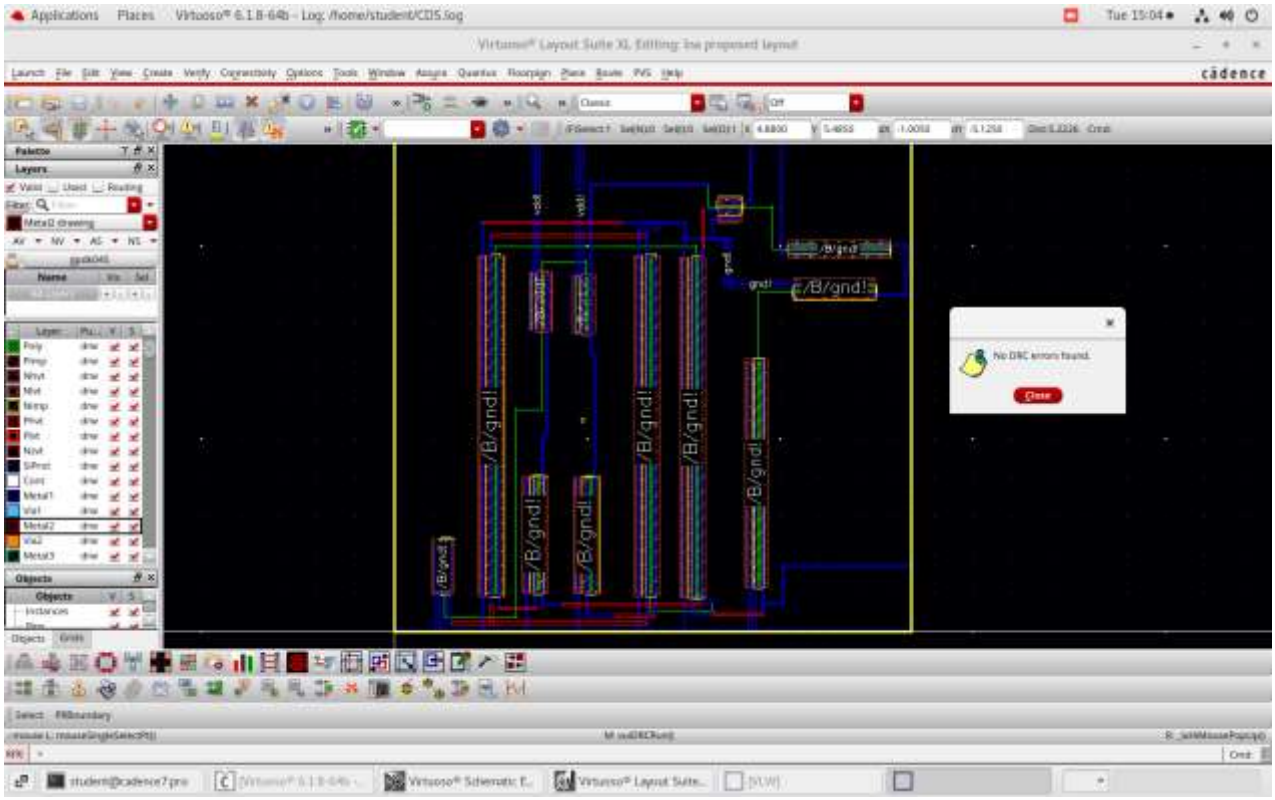

Figure 2- Design Rule Check

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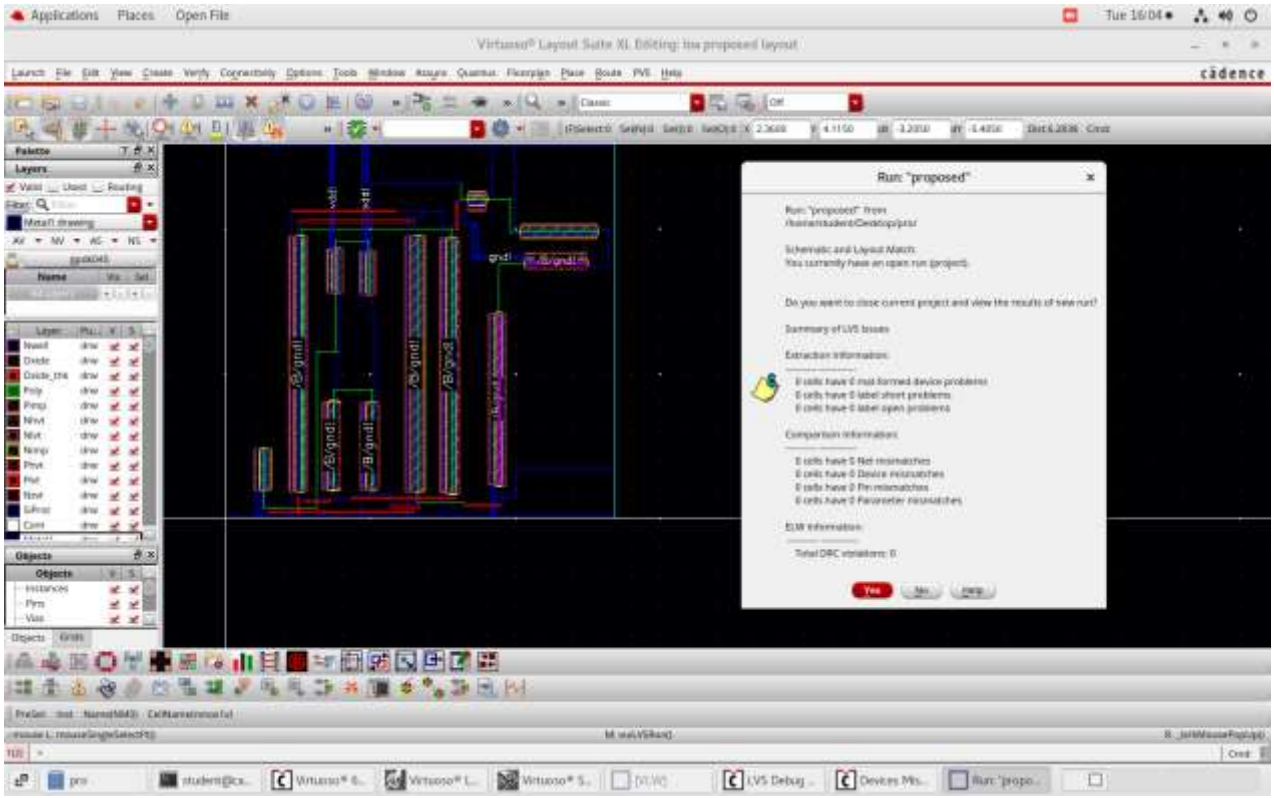

Figure 3- Layout vs Schematic check

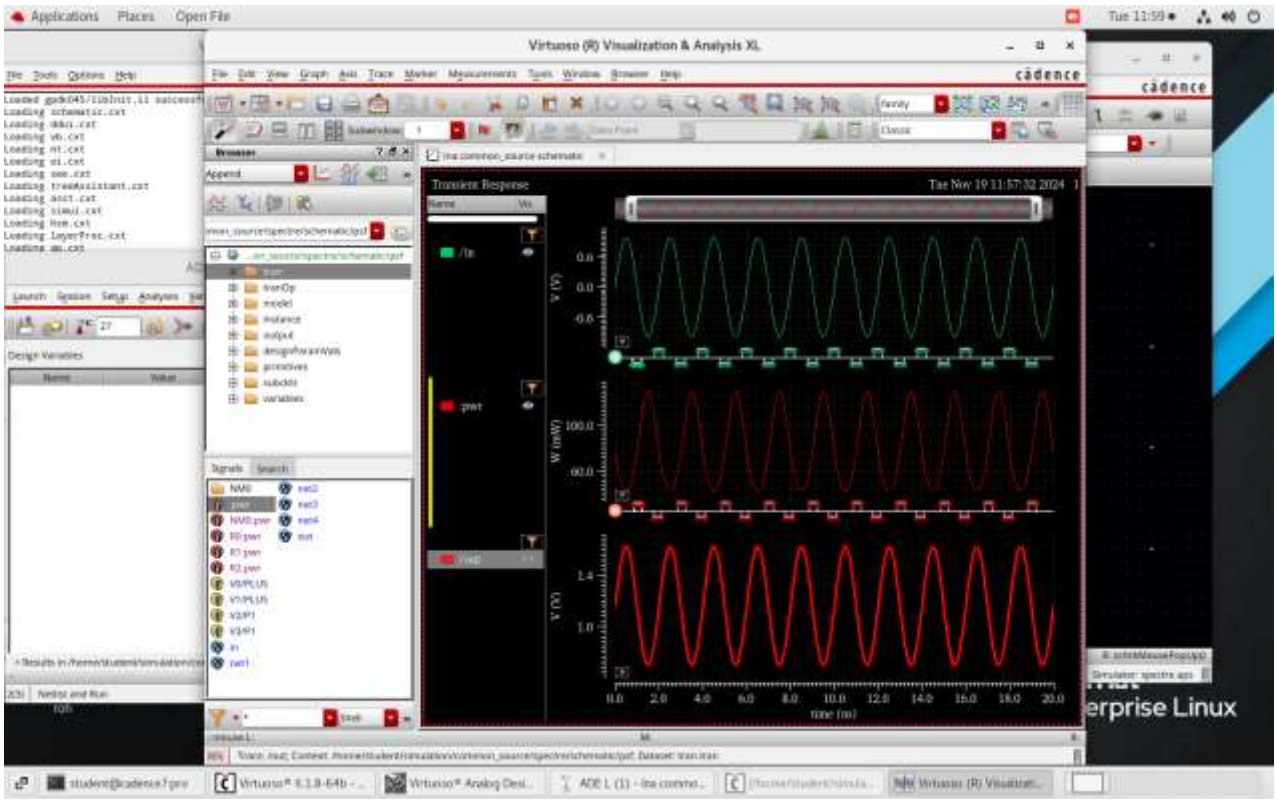

Figure 4- Transient analysis after parasitic extraction.

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V. CONCLUSION AND FUTURE WORK

Key Findings

- Low noise figure (~2 dB) with high gain (~18 dB).
- Significant power reduction (22.4mW), making it ideal for portable applications.
- Validated stability across process variations using Monte Carlo simulations.
- Successfully verified layout with no DRC/LVS errors.

Future Work

- Implementing the design in more advanced CMOS nodes (e.g., 22nm, 16nm).
- Fabrication and real-world testing to validate simulated results.
- Exploring machine learning techniques for further optimization.

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