Efficient CRC – BCH Unified Encoder for Global Positioning System

Hemnath T[1], Kiruthik P[2], Manimalan V[3], Jayapal N[4]

B.E, ECE, Kongunadu College of Engineering and Technology, Trichy, India[1]

B.E, ECE, Kongunadu College of Engineering and Technology, Trichy, India[2]

B.E, ECE, Kongunadu College of Engineering and Technology, Trichy, India[3]

Assistant Professor, ECE, Kongunadu College of Engineering and Technology, Trichy, India[4]

Abstract: GPS uses ECCs to see if an error occurs when the data sent from the satellite reaches the user. Each message structure uses ECCs such as Hamming Code, CRC, BCH Code, and LDPC Code. If the satellite contains all of the encoders, it has a negative impact to the area and power consumption. Therefore, in this paper, we propose a CRC-BCH unified encoder for GPS, which is efficient in terms of space and power consumption. Since both the CRC and BCH encoders use shift registers, the design was made using this part. To replace the existing encoder, the CRC-BCH encoder must have the same output. To validate this, we used individual CRC and BCH encoders and confirmed that the generated output was identical to the output of the proposed encoder. The proposed CRC-BCH unified encoder was synthesized at an operating frequency of 400 MHz using the CMOS 28nm process. The synthesis results showed that it used 16.67% less area and consumed 19.68% less power than the existing encoder. Therefore, the proposed CRC-BCH unified encoder offers advantages in terms of satellite weight and energy efficiency.

Keywords: GPS, ECC, CRC, BCH, Encoder.

I. INTRODUCTION

The Global Navigation Satellite System (GNSS) is a service that provides information on the position, velocity, and time (PVT) of receivers using signals transmitted by satellites in Earth's orbit. Currently, various countries provide GNSS, including Russia's GLONASS, China's Bei Dou, and Europe's Galileo. Among them, the most notable GNSS is the Global Positioning System (GPS). GPS is a GNSS provided by the United States and has been available to the public since the 1980s. It is still widely used by many people today. When GPS satellites transmit signals in orbit, the signals may be exposed to various environments. This environment provides the user with the possibility of containing errors different from the data transmitted by the satellite when received [1] .Therefore, GPS uses an Error Correction Code (ECC) that can check whether there is an error in the received signal. The ECCs used in GPS are Hamming Code, Cyclic redundancy Check (CRC), Bose-Chaudhuri- Hocquenghem (BCH) Code, and Low-Density Parity Check (LDPC) Code. They depend on what message structure GPS uses, including Hamming Code in Legacy Navigation (LNAV) message structure, CRC in Civil Navigation (CNAV) message structure, and CRC, BCH Code, and LDPC in CNAV-2 message structure [2-3]. Therefore, there should be a circuit inside the GPS satellite that can encode these four ECCs. However, having many circuits can increase weight and power consumption of the satellite. If the shared part of each encoder is considered and integrated into one encoder, area and power consumption can be reduced. Therefore, this paper proposes a power and area efficient CRC-BCH unified encoder that combines the two encoder circuits into one. The encoders of the two ECCs were integrated using shift registers. In addition, comparisons are made in terms of area and power used compared to when existing CRC and BCH encoders are used separately.

II. METHODOLOGY

A. Dataset

The dataset used for this study comprises GPS signal data containing encoded message blocks. These messages follow standard GPS communication protocols, including NAV, CNAV, and CNAV-2 formats. To ensure robustness, the dataset includes various error patterns and noise conditions, simulating real-world interference such as atmospheric noise, multipath effects, and hardware-induced distortions. The dataset is collected from publicly available GPS signal repositories and synthesized error scenarios to evaluate the encoding performance under different conditions.

B. Preprocessing

Preprocessing is crucial to standardizing and preparing the GPS messages for encoding. First, raw GPS messages are converted into binary sequences, ensuring compatibility with the CRC-BCH encoding framework. Next, controlled bit errors are introduced to test the efficiency of the encoding process in mitigating errors. The binary sequences are then normalized to maintain consistency in message length and format. Additionally, bit alignment techniques are employed to ensure proper message framing, preventing misalignment issues during CRC and BCH encoding. This step helps in reducing unnecessary overhead while optimizing computational performance. CRC is an ECC using the properties of cyclic codes [4]. There are two main advantages of the CRC. One is that encoders can be designed relatively easily using shift registers using the nature of cyclical codes. The second is that it is robust not only to random errors but also to burst errors, which occur continuously. The encoding process is as follows: starting with a shift register initialized to a value of 0, an 8-bit message is fed from the most significant bit (MSB). After the entire 8-bit input is registered, 51 shifts are executed, resulting in 51 outputs from the 7 b register. The initial 8 bits of the output remain identical to the original values. Thereafter, 43 bits calculated by the shift register are output. These 43 bits that came out at the end become parity bits.

III. SYSTEM MODEL

A. Data Formatting

The first step in preprocessing is converting raw GPS messages into a structured binary format GPS messages , such as NAV, CNAV, and CNAV-2, are typically transmitted in structured bit sequences. These messages contain essential information like satellite ephemeris, clock corrections, and system time. To standardize the data, each message is extracted, segmented, and converted into a binary representation that aligns with the requirements of the CRC and BCH encoding modules. This conversion ensures that all messages maintain uniformity in structure, facilitating smooth encoding . To compare the performance with the existing encoders, synthesis was carried out using the CMOS 28nm process. Experimental results confirmed that the proposed structure offers advantages in terms of area and power consumption compared to the traditional design.

B. Error pattern simulation

To evaluate the robustness of the encoding process, error patterns are artificially introduced into the binary sequences. These errors simulate real-world disturbances such as thermal noise, multipath interference, and ionospheric distortions. Different error types, including random bit flips, burst errors, and synchronization errors, are applied to test how well the CRC-BCH unified encoder detects and corrects them. By introducing controlled errors, the system's ability to handle various levels of signal degradation can be thoroughly analyzed . After the entire 8-bit input is registered, 51 shifts are executed, resulting in 51 outputs from the 7 b register. The initial 8 bits of the output remain identical to the original values. Thereafter, 43 bits calculated by the shift register are output. These 43 bits that came out at the end become parity bits. Due to its cyclic property, the BCH code can also be encoded using a shift register. The BCH code used in CNAV-2 is BCH (51, 8), meaning that an 8-bit message is encoded into 51 encoded symbols.

IV. PROPOSED SYSTEM

A. Overview

CRC is an ECC using the properties of cyclic codes. There are two main advantages of the CRC. One is that encoders can be designed relatively easily using shift registers using the nature of cyclical codes. The second is that it is robust not only to random errors but also to burst errors, which occur continuously.
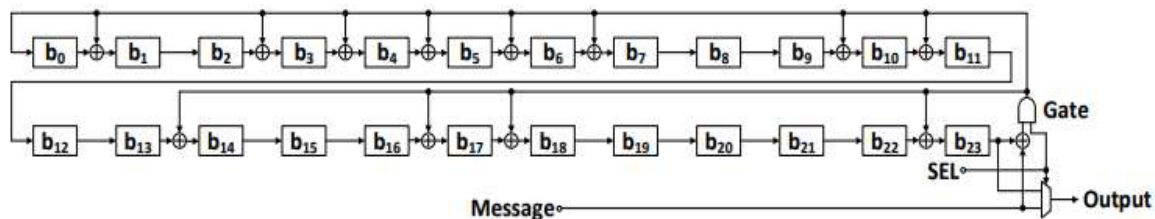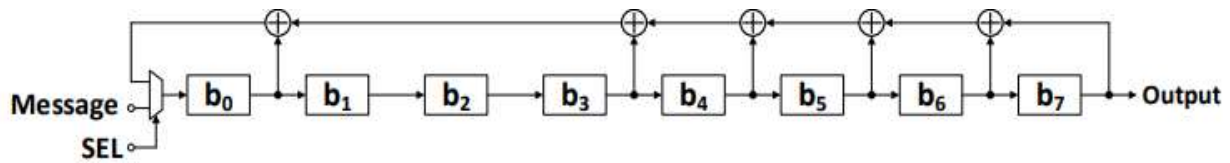

Fig. 1. Conventional CRC-24Q encoder
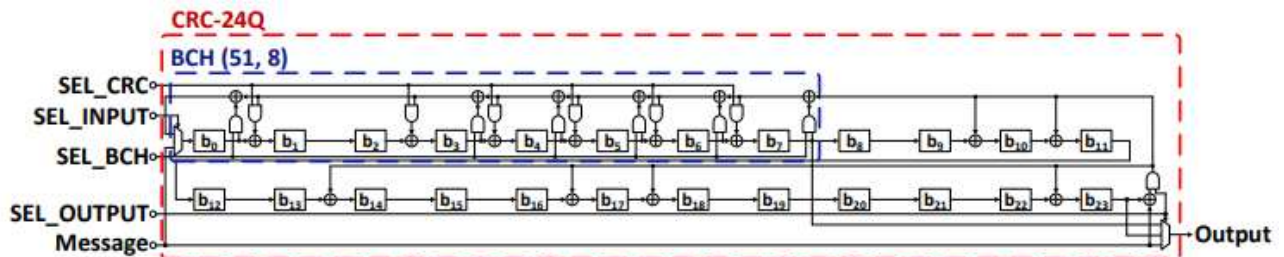
Fig. 2. Conventional BCH (51, 8) encoder

Fig. 3. Proposed CRC-BCH unified encoder

Using these generator polynomials, 24 parity bits can be generated regardless of the length of the input message. This specific generator polynomial-based CRC is referred to as CRC-24Q [2]. The process of CRC encoding can be represented. The process of obtaining the remainder through polynomial division can be implemented using a shift register. The encoding circuit for CRC-24Q is shown in figure 1. Based on a total of 24 shift registers initialized to a value of 0, each tap's position is determined by the coefficients of $g(X)$. When the message to be encoded enters from the input message, it performs an XOR operation with the output of b_{23}, and this result becomes the feedback value. While the input message is being fed into the register, the output is directly from the input message. After the entire input message is registered, the gate output is set to zero, ensuring the feedback remains zero, and the remaining values in the register are output bit by bit. These remaining values in the register correspond to the coefficients of the remainder in the mathematical formulation and serve as the parity bits. BCH code is also a type of cyclic code. However, unlike the CRC, it is constituted of polynomials based on the extended Galois field $GF(2)^m$ [4]. Due to its cyclic property, the BCH code can also be encoded using a shift register. The BCH code used in CNAV-2 is BCH (51, 8), meaning that an 8-bit message is encoded into 51 encoded symbols.

B. Normalization

Normalization ensures that all GPS messages have a consistent structure and length before undergoing encoding. Some GPS messages vary in size due to different data contents and transmission protocols. To standardize the input, padding techniques are applied to shorter messages, while longer messages are segmented into fixed-length blocks. This step is crucial for maintaining synchronization across all encoding operations and optimizing computational efficiency. To ensure robustness, the dataset includes various error patterns and noise conditions, simulating real-world interference such as atmospheric noise, multipath effects, and hardware-induced distortions. Additionally, normalization prevents excessive overhead in encoding by maintaining a balance between data integrity and processing speed.

C. Noise reduction

To improve image clarity and reduce unwanted artifacts that might affect model training, Gaussian filters were applied. These filters help smooth the images by reducing high-frequency noise, which is especially important when working with medical images that may have subtle variations in texture and details. However, given the differences in the generator polynomial and directions of tap between BCH and CRC, AND gates were utilized to control and set the appropriate tap directions for each condition. To relay the BCH output, the output section of the 7 b register was connected to the CRC output section. with a multiplexer introduced to select which value is outputted. The choice between encoding CRC or BCH is determined using SEL_CRC and SEL_BCH.

V. RESULTS AND DISCUSSION

To replace the existing encoder with the proposed CRC-BCH unified encoder, the output generated by each encoder must match the output from the CRCBCH encoder. Therefore, we first implemented conventional CRC-24Q and BCH (51, 8) encoders to check the output. Based on the respective encoders of CRC-24Q and BCH (51, 8) implemented, it was confirmed whether the output of the proposed CRCBCH unified encoder was the same. As a result of simulation to check whether the circuit is operating normally, it was confirmed that the correct output was produced according to each set mode as shown in Figure 4. Subsequently, CMOS 28nm was used in the synthesis process, and the operating

frequency was set to 400 MHz . In order to compare the area of the conventional and proposed structures, an equivalent gate count obtained by dividing the total area by the size of the two-input NAND gate was used, and the power consumption of the two structures was confirmed using the synthesis results. Based on the results presented in Table 1, the proposed structure reduced the area by 16.67% and the total power consumption by 19.68%, confirming that the proposed CRC-BCH unified provides advantages in terms of area and power consumption over the existing design. The proposed unified encoder integrates CRC for error detection and BCH for forward error correction, ensuring both reliability and efficiency in GPS message transmission.

The architecture consists of multiple key components. The input layer receives raw binary GPS messages, which are first processed through the CRC encoding module to append error detection bits. These CRC bits help in identifying transmission errors before applying BCH encoding. The BCH encoding module then introduces redundancy, allowing for error correction in noisy environments. The framework is designed to optimize computational complexity by integrating CRC and BCH encoding in a streamlined process. The final output layer produces encoded messages that are robust against errors and ready for transmission. To enhance the performance of the encoding process, an optimized hybrid algorithm combining lookup-table-based and polynomial-based encoding is implemented. This ensures efficient computation while maintaining accuracy. However, given the differences in the generator polynomial and directions of tap between BCH and CRC, AND gates were utilized to control and set the appropriate tap directions for each condition. To relay the BCH output, the output section of the 7 b register was connected to the CRC output section. with a multiplexer introduced to select which value is outputted.
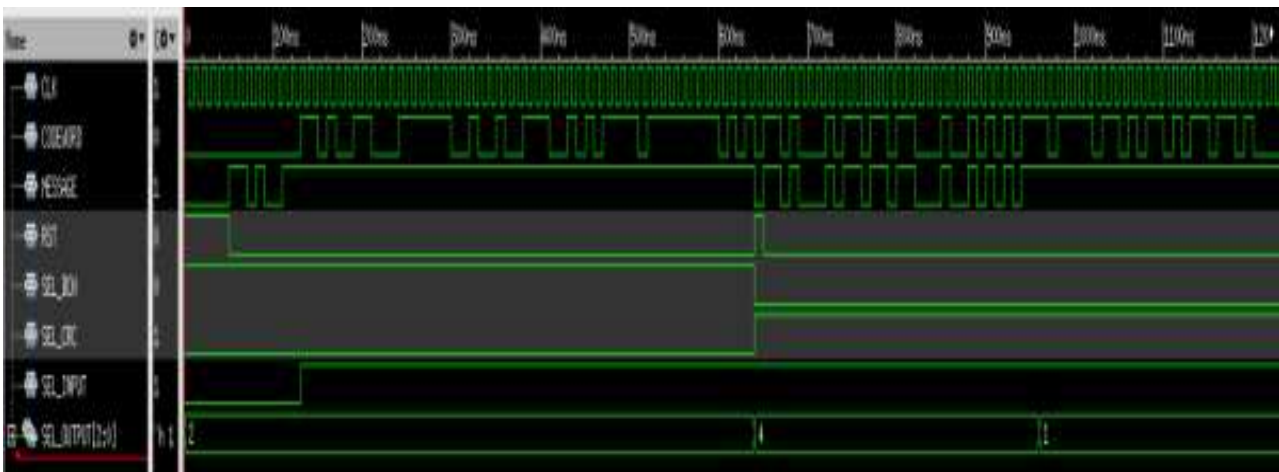

Fig. 4. Simulation result

To replace the existing encoder with the proposed CRC-BCH unified encoder, the output generated by each encoder must match the output from the CRCBCH encoder. Therefore, we first implemented conventional CRC-24Q and BCH (51, 8) encoders to check the output. Based on the respective encoders of CRC-24Q and BCH (51, 8) implemented, it was confirmed whether the output of the proposed CRCBCH unified encoder was the same. As a result of simulation to check whether the circuit is operating normally, it was confirmed that the correct output was produced according to each set mode as shown in Figure 4. Subsequently, CMOS 28nm was used in the synthesis process, and the operating frequency was set to 400 MHz . In order to compare the area of the conventional and proposed structures, an equivalent gate count obtained by dividing the total area by the size of the two-input NAND gate was used, and the power consumption of the two structures was confirmed using the synthesis results. Based on the results presented in Table 1, the proposed structure reduced the area by 16.67% and the total power consumption by 19.68%, confirming that the proposed CRC-BCH unified provides advantages in terms of area and power consumption over the existing design. To replace the existing encoder with the proposed CRC-BCH unified encoder, the output generated by each encoder must match the output from the CRCBCH encoder. Therefore, we first implemented conventional CRC-24Q and BCH (51, 8) encoders to check the output. Based on the respective encoders of CRC-24Q and BCH (51, 8) implemented, it was confirmed whether the output of the proposed CRCBCH unified encoder was the same.

As a result of simulation to check whether the circuit is operating normally, it was confirmed that the correct output was produced according to each set mode as shown in Figure 4. Subsequently, CMOS 28nm was used in the synthesis process, and the operating frequency was set to 400 MHz . In order to compare the area of the conventional and proposed structures, an equivalent gate count obtained by dividing the total area by the size of the two-input NAND gate was used, and the power consumption of the two structures was confirmed using the synthesis results. Based on the results

presented in Table 1, the proposed structure reduced the area by 16.67% and the total power consumption by 19.68%, confirming that the proposed CRC-BCH unified provides advantages in terms of area and power consumption over the existing design. The proposed unified encoder integrates CRC for error detection and BCH for forward error correction, ensuring both reliability and efficiency in GPS message transmission. The architecture consists of multiple key components. The input layer receives raw binary GPS messages, which are first processed through the CRC encoding module to append error detection bits. These CRC bits help in identifying transmission errors before applying BCH encoding. The BCH encoding module then introduces redundancy, allowing for error correction in noisy environments. The framework is designed to optimize computational complexity by integrating CRC and BCH encoding in a streamlined process. The final output layer produces encoded messages that are robust against errors and ready for transmission. Experimental results confirmed that the proposed structure offers advantages in terms of area and power consumption compared to the traditional design. Therefore, we believe that satellites using the proposed CRC-BCH unified encoder would have superior weight efficiency compared to current satellites.

VI. CONCLUSION

In this paper, we proposed a CRC-BCH unified encoder for GPS to reduce power consumption and area. Taking advantage of the fact that both CRC and BCH encoders use shift registers, we integrated the BCH encoder into the CRC encoder structure, which requires more registers. Additionally, we added a circuit to select between CRC and BCH encoding based on the desired encoding method. To compare the performance with the existing encoders, synthesis was carried out using the CMOS 28nm process. Experimental results confirmed that the proposed structure offers advantages in terms of area and power consumption compared to the traditional design. Therefore, we believe that satellites using the proposed CRC-BCH unified encoder would have superior weight efficiency compared to current satellites.

REFERENCES

[1]. L. Heng, G. X. Gao, T. Walter, and P. Enge, "Statistical characterization of GPS signal-in-space errors," in Proc. ION ITM, San Diego, CA, USA, Jan. 2011, pp. 312–319.

[2]. S. Lin and D. J. Costello, Error Control Coding: Fundamentals and Applications, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2004.

[3]. J. Zhang, C. Shao and Y. Hou, "Optimal quantification method for LDPC code decoding of GPS L1C signal", Science of Surveying and Mapping, vol. 44, no. 1, pp. 32-35, 2019.

[4]. K. Ghorbani, N. Orouji and M. R. Mosavi, "Navigation message authentication based on one-way Hash chain to mitigate spoofing attacks for GPS L1", Wireless Personal Communications, vol. 113, no. 6, pp. 1743-1754, 2020.

[5]. C. Wang, L. Zhang, C. Zheng et al., "Research on phase optimal matching strategy of GPS L1C signal coverage code", Proc. of the 6th China Satellite Navigation Academic Annual Conference, pp. 1-5, 2015.

[6]. Q. Li, "Study on the method and performance of fast frame synchronization of GPS L1C navigation message", Proc. of China Satellite Navigation Academic Annual Conference, pp. 1-5, 2015.

[7]. T. South and Y. Kou, "Implementation and performance analysis of soft decision decoding for CNAV-2 messages", Journal of Time and Frequency, vol. 38, no. 2, pp. 112-113, 2015.

[8]. Z. Deng, J. Li, C. Li et al., "Characteristic analysis and fast adaptive synchronization algorithm of GPS CNAV-2 navigation message synchronization code", Proc. of China Satellite Navigation Conference, pp. 32-38, 2014

[9]. G. Xie, Principle of Global Navigation Satellite System, Beijing: Publishing House of Electronics Industry, pp.143-158, 2013.

[10]. X. Fang, H. Peng and L. Wu, "A quick frame synchronization method for navigation message based on ephemeris matching", Modern Radar, vol. 43, no. 4, pp. 34-38, 2021.