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Energy Efficient GNRFET Operational Amplifier for Pneumatic applications in Aeronautical Engineering

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Abstract: In this research paper, energy efficient GNRFET operational amplifier for Pneumatic applications is designed and simulated at 45nm technology node. DC voltage gain, average power, unity gain bandwidth and output resistance have been computed using HSPICE. Recent work on GNRFET circuit simulations has shown that GNRFETs may have potential in low power applications. It has better DC Gain, low output resistance and extremely less average power as compared ot its CMOS counterpart. Further, the simulation studies have revealed that the performance of the proposed low voltage folded cascode Op Amp can be improved optimized for particle application. The proposed circuit is useful for Aeronautical Engineering, biomedical and other low power applications. In the proposed circuit, the DC Gain is 24.8% higher, Output Resistance is 26.92% lower as compared to Bulk Operational amplifier.

Index terms: GNR, GNRFET, Op Amp, Simulation, DC Gain, Power Consumption, Output Resistance, Bandwidth, Phase Margin.

I. CMOS AND GNRFET

The conventional Op Amps techniques at short channel length is going to out of reach in near future. The appropriate topology is suggested which has a perfect balance between complexity and performance. Scaling of CMOS to the nano ranges has many limitations and leads to increase the leakage currents, power dissipation, and short-channel effects [1-2]. Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces less risk to the thinner oxides, which results from device scaling. However, the reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing. Scaling down the threshold voltage of the MOS reduces the performance to approximately extent but there is increase in the static power dissipation [3-4].

The graphene nano-ribbon field effect transistor (GNRFET) is an emerging technology that received much attention in recent years. There are two different kinds of GNRFETs: metal-oxide-semiconductor (MOS)-type GNRFETs (MOS-GNRFETs) and Schottky-barrier (SB)-type GNRFETs (SB-GNRFETs) [5-6]. The SB-type device forms Schottky barriers at its junctions using a graphene channel and metallic contacts. Impurities of either the donor or acceptor types are purposefully injected into the reservoirs while using MOS-type. When donors are used for doping, an n-type GNRFET is formed, in which electron conduction is the primary driver of current flow. Figure 1 is a schematic of a four-ribbon GNRFET. Each ribbon represents armchair chirality. The number of ribbons (n_{Rib}) have equal width (W_{Ch}) and spacing ($2*W_{SP}$). The width of a GNR (W_{Ch}) is typically specified by the number of dimer lines (N) in its lattice structure[7-8].

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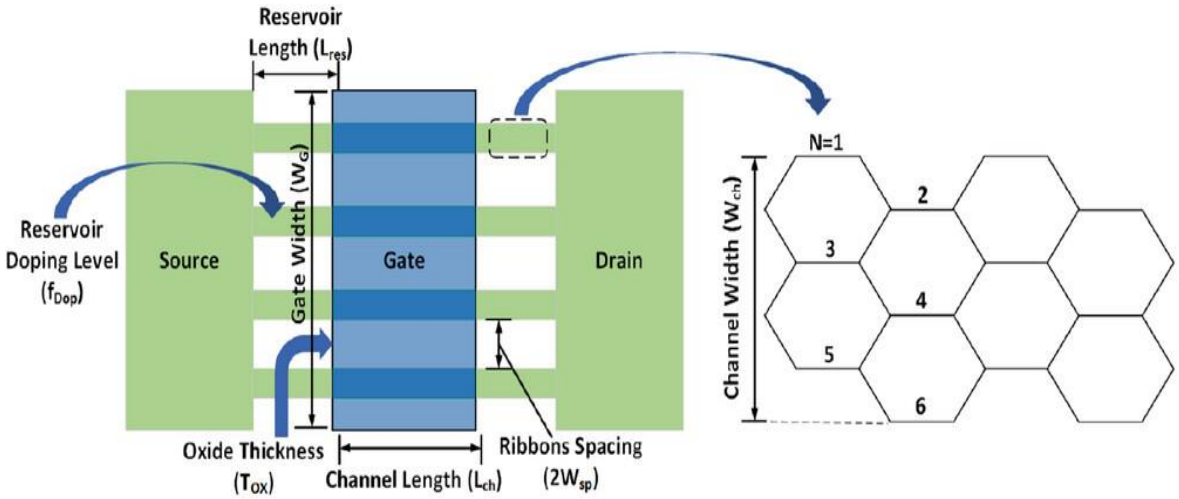

Figure 1. The 4-ribbon MOS-type GNRFET's structural design with ribbons sharing a common source and drain, and armchair-type GNR's lattice structure with dimer lines (*N*) = 6.

$$\text{Gate width}(W_{\text{gate}}) = n_{\text{Rib}} \times (W_{\text{Ch}} + 2W_{\text{SP}}) \quad (1)$$

The right shows an example of an (N) = 6 GNR. A single metal gate is positioned on top of the parallel ribbons. The gate of this four-ribbon GNRFET measures in equation 1.

$$\text{Channnel width}(W_{\text{Ch}}) = (N-1)\sqrt{3} \times d_{cc}/2 \quad (2)$$

Equation (2) establishes a relationship between the width of a GNR (W_{Ch}), the number of dimer lines in GNR (N), and the bond spacing between carbon atoms dcc [5].

II. PROPOSED GNRFET BASED FOLDED CASCODE OP AMP DESIGN

The Figure 2 shows the schematic of a folded-folded cascode op-amp using a class AB output buffer. In the frequency response of the op-amp, the load of the op-amp is a 1 pF capacitor. Folded cascode Operational Amplifier is designed at different voltages. The widths of MOSFETs are chosen to be identical for a reasonable comparison. We simulated the proposed circuit using HSPICE which can be used in VLSI systems such as microprocessors, DSP architectures and nano-micro systems.

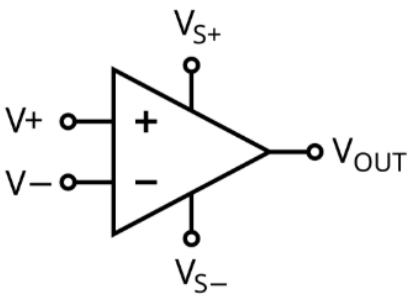

Figure 2. Symbol of Operational Amplifier

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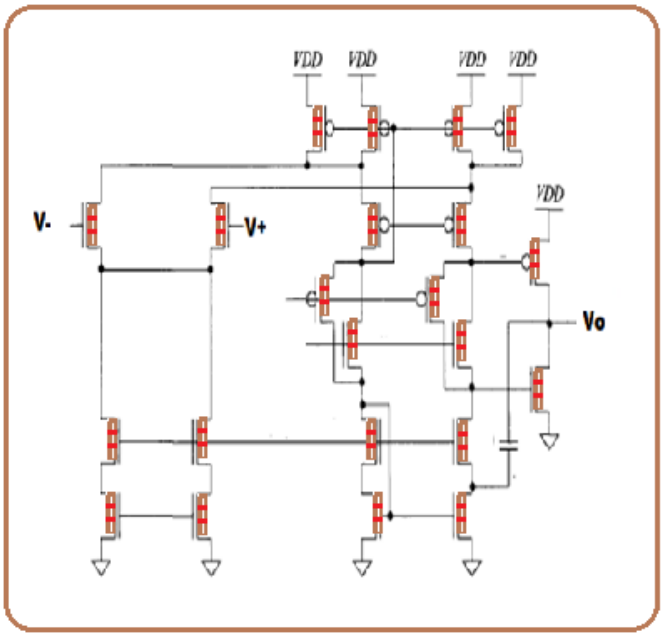

Figure 3. PROPOSED GNRFET BASED FOLDED CASCODE OP AMP DESIGN

III. SIMULATIONS OF PROPOSED FOLDED CASCODE OP AMP DESIGN

The proposed circuit is simulated using hspice software at 45nm technology nodes. It is observed that the proposed circuit is having higher gain, low output resistance and higher phase margin as compared to CMOS Circuit due to unique properties of GNRFET technology like 1-D Transport, high Transconductance and large drive current.

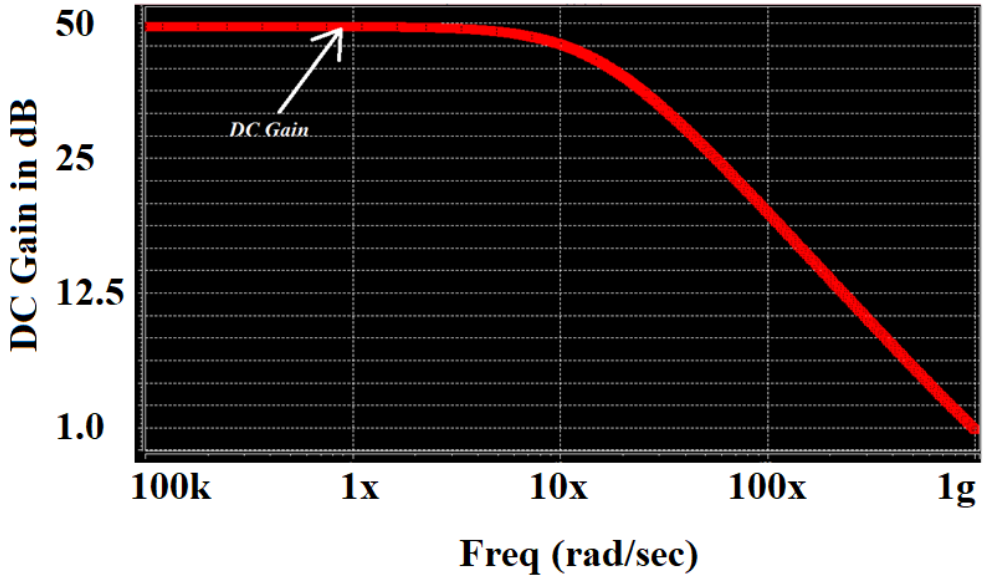

Figure 4: Frequency response of GNRFET based folded cascode op amp design

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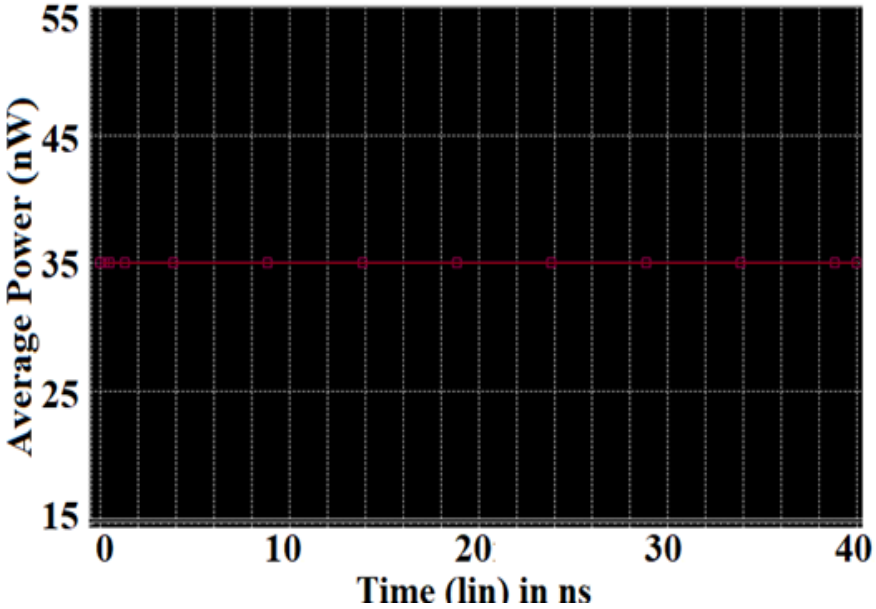

Figure 5: Average Power of GNRFET based folded cascode op amp design

TABLE 1. The design parameters of the MOS-GNRFET device.

Parameters	Descriptions	Values
L_{Ch}	Channel length	32 nm
n_{Rib}	Number of GNRs	6
N	Number of dimer lines in the GNR	9
W_{SP}	Spacing between the edges of two adjacent GNRs	4.35 nm
T_{OX}	Thickness of the top gate dielectric material (planer gate)	0.95 nm
T_{OX2}	Oxide layer between the channel and substrate/bottom gate	20 nm
d_{op}	Doping fraction of the source and drain reservoirs	0.001
P_r	Device's edge roughness percentage	0
Temp	Room temperature	300 K
W_{Ch}	Channel width	32 nm

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Table 2: Comparative analysis of Folded Cascode CMOS and GNRFET based Op Amp Design with C_L = 1 pf, at V_{DD}=1.0 V.

S. NO.	PARAMETERS	CMOS BASED FOLDED CASCODE AMPLIFIER AT 1V[2]	Proposed GNRFET BASED FOLDED CASCODE AMPLIFIER AT 1V
1	DC GAIN	37.6 dB	50 dB
2	Unity Gain Freq	951 MHz	936MHz
3	Output Resistance	23.1 Ohms	18.2 Ohms
4	Average Power	1.24mW	35 nW
5	Phase Margin	79.2^0	87.7^0
	Slew Rate	8.57E+8	2.2E+9

IV. CONCLUSION

In this research paper, simulation of GNRFET based low voltage folded cascode Op Amp at 45 nm is carried out. The performance parameters shows that the proposed low voltage Cascode Op Amp is better for applications in VLSI design specially in Aeronautical Engineering, biomedical and other low power applications. In the proposed circuit, the DC Gain is 24.8% higher, Output Resistance is 26.92% lower as compared to Bulk Operational amplifier.

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