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Design of Optimized Carry Look Ahead Adder using Hybrid Logic

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Abstract: In modern computing systems, fast and efficient arithmetic operations are essential for enhancing overall performance. The Carry Look-Ahead Adder (CLA) is widely used due to its reduced propagation delay compared to conventional ripple-carry adders. However, further optimization is required to improve speed, power efficiency, and circuit complexity. This paper presents a novel design of an optimized CLA using hybrid logic, integrating CMOS technology with a custom-designed memristor model implemented in LTSpice XVII. The proposed approach leverages the low-power characteristics of memristors while maintaining the robustness and switching reliability of CMOS technology. By utilizing Voltage-Controlled Resistors (VCRs) as memristive elements, the design achieves significant reductions in propagation delay and power consumption.Extensive simulations and performance evaluations demonstrate the superiority of the proposed CLA in terms of speed and energy efficiency compared to conventional CLAs. The results indicate that hybrid CMOS-memristor logic can be a promising approach for designing next-generation arithmetic circuits. This study provides valuable insights into the practical implementation of hybrid logic circuits and establishes a foundation for future research in memristor-based arithmetic units.

Keywords: Memrisor, CLA, LTSpice XVII, Hybrid Logic

I. INTRODUCTION

High-speed and energy-efficient arithmetic circuits are crucial for modern computing applications, particularly in processors, digital signal processing, and artificial intelligence. Among various arithmetic units, adders play a fundamental role in determining computational efficiency. The Carry Look-Ahead Adder (CLA) is widely recognized for its ability to overcome the propagation delay limitations of conventional ripple-carry adders by predicting carry bits in advance, significantly improving speed and efficiency [1][2]. However, further optimization is required to enhance performance while minimizing power consumption and area overhead. Traditional CMOS-based CLA implementations face trade-offs between speed, power, and transistor count, which limits their applicability in power-sensitive and high-performance systems [10][11].

Recent advancements in hybrid logic design, particularly the integration of memristor-based components with conventional CMOS circuits, have demonstrated promising improvements in arithmetic unit efficiency [4][8]. Memristors, first introduced by Chua [6], are considered the fourth fundamental passive circuit element alongside resistors, capacitors, and inductors. Their unique properties, such as non-volatility, tunable resistance, and ultra-low power consumption, make them suitable for a wide range of applications, including memory, logic circuits, and neuromorphic computing [5]. The integration of memristors into arithmetic circuits has gained significant attention due to their potential to reduce power dissipation while maintaining high-speed operation.

Several studies have explored the use of memristors in adder designs to improve power-delay performance. Wang et al. [2] proposed a hybrid carry-lookahead/carry-select adder to achieve a balance between speed and power efficiency.

Similarly, He and Chang [3] introduced a hybrid carry-lookahead/carry-select based redundant binary to two's complement converter, demonstrating an improvement in computational efficiency. More recently, Shaltoot and Madian [4] proposed memristor-based CLA architectures, showcasing the potential of memristor-based logic circuits. However, these designs face challenges related to the variability and reliability of memristor models, necessitating further research into optimized hybrid logic implementations.

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In this paper, we present an optimized Carry Look-Ahead Adder using hybrid logic, integrating CMOS technology with a custom-designed memristor model implemented in LTSpice XVII. Unlike existing designs that rely on generic memristor models, our approach incorporates a self-designed Voltage-Controlled Resistor (VCR)-based memristor, allowing for greater control over circuit behavior and performance [9]. The proposed CLA leverages the low-power and high-speed advantages of memristors while maintaining the robustness and scalability of CMOS technology. Through extensive simulations, we demonstrate that our design achieves significant improvements in propagation delay, power consumption, and overall circuit efficiency compared to conventional CLA implementations [8][10].

II. RELATED WORK

High-Speed and Energy-Efficient Carry Look-Ahead Adder. J. Low Power Electron. by Balasubramanian and Mastorakis et.al[1] . This paper presents a high-speed and energy-efficient CLA. The authors focus on reducing power consumption without compromising performance, a significant challenge in modern digital circuits. By emphasizing energy efficiency in high-performance arithmetic operations, their work contributes to optimizing CLA circuits for low-power consumption while maintaining high-speed performance, which is crucial for modern computing systems.

The design of hybrid carry-lookahead/carry-select adders. By Wang et al[2] . propose a hybrid carry-lookahead/carry-select adder that combines the benefits of both CLA and carry-select adders. This hybrid design aims to balance speed, area, and power efficiency, addressing trade-offs between these parameters in digital adders. Their work provides a solution to improving propagation delay and optimizing circuit complexity, making the design suitable for high-speed computing applications.

Memristor based carry lookahead adder architectures by Shaltoot and Madian[3] This study investigates memristor-based CLA architectures, highlighting the potential of memristors to replace traditional logic gates in digital adders. By incorporating memristors, the authors demonstrate improvements in power efficiency and circuit speed. This research emphasizes the viability of memristor-based circuits for energy-efficient designs in modern computing systems, particularly in arithmetic units.

Nonvolatile memristor memory Device characteristics and design implications by Ho et al[4]. focus on the characteristics of non-volatile memristors and their design implications for digital circuits. Their work explores the potential of memristors to be used in memory and logic functions. By understanding the fundamental behavior of memristors, their study contributes to developing more reliable and efficient memristor-based digital circuits for low-power and high-performance applications.

Memristor: The missing circuit element by eon Chua[5] Chua introduced the concept of the memristor as the missing circuit element, laying the groundwork for future research into memristors' properties and applications. This seminal paper is crucial for understanding the fundamental behavior of memristors, and it is foundational for the development of memristor-based digital circuits, especially in logic and memory functions.

A Design of Carry-Lookahead Adder with Improvised Memristor Modelling by P. Shivani Reddy, V. Abhitej, G. Sai Pavan, and C. Padmini[6] .The authors propose a design of CLA using memristors with an emphasis on improving the power and delay performance. Their work suggests a modified memristor model that enhances the CLA's speed and energy efficiency. By focusing on these two key aspects, the study contributes to making memristor-based CLAs viable for modern, high-performance digital systems.

A Carry Lookahead Adder Based on Hybrid CMOS-Memristor Logic Circuit by Gongzhi Liu et al[7].introduced a hybrid CMOS-memristor logic-based CLA.

The study demonstrates the effectiveness of combining CMOS technology with memristors to improve power efficiency and speed. The hybrid approach enhances the performance of CLAs, making them more suitable for energy-efficient, high-speed arithmetic operations in digital systems.

Memristor SPICE Model for Designing Analog Circuit by Adzmi et al[8].This paper discusses the use of memristor SPICE models for designing analog circuits, offering valuable insights into the integration of memristor-based components into digital systems. Accurate modeling of memristors is crucial for the successful design and simulation of digital circuits, and this work provides essential tools for implementing memristor-based logic in a variety of digital applications.

A New Carry Look-Ahead Adder Architecture Optimized for Speed and Energy by Balasubramanian and Maskell[9].In this work, the authors propose a new CLA architecture optimized for both speed and energy efficiency. They focus on improving the carry generation mechanism to reduce power dissipation while maintaining high-speed performance. The study shows that a hybrid approach, integrating traditional CMOS technology with advanced memristor components, can result in significant improvements in both speed and energy efficiency.

Performance Comparison of Carry-Lookahead and Carry-Select Adders Based on Accurate and Approximate Additions. By Balasubramanian and Mastorakis[10].The authors present a performance comparison between CLA and carry-select adders, evaluating both accurate and approximate additions. Their analysis reveals the advantages of CLA in terms of speed and power consumption compared to carry-select adders.

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This comparison is essential for understanding the strengths and weaknesses of different adder architectures, informing future designs of energy-efficient and high-performance arithmetic circuits.

A Power-Delay Efficient Hybrid Carry-Lookahead/Carry-Select Based Redundant Binary to Two's Complement Converter by Chip-Hong et al[11]. In this work, the authors propose a novel hybrid carry-lookahead/carry-select-based approach to optimize the power-delay performance of the RB to two's complement conversion. They focus on improving the carry generation mechanism to reduce power dissipation while maintaining high-speed performance.

III. METHODOLOGY

CLA Structure

The Carry Look-Ahead Adder (CLA) improves addition speed by reducing the dependency on carry propagation. Unlike the ripple-carry adder, which propagates the carry bit sequentially, CLA computes carry signals in parallel using generate ('G') and propagate ('P') functions. The fundamental equations governing the CLA operation are:

where:

- Gi: Generate signal (produced when both inputs are high).
- Pi: Propagate signal (determines carry transmission).
- Ci+1: Carry output for the next bit.

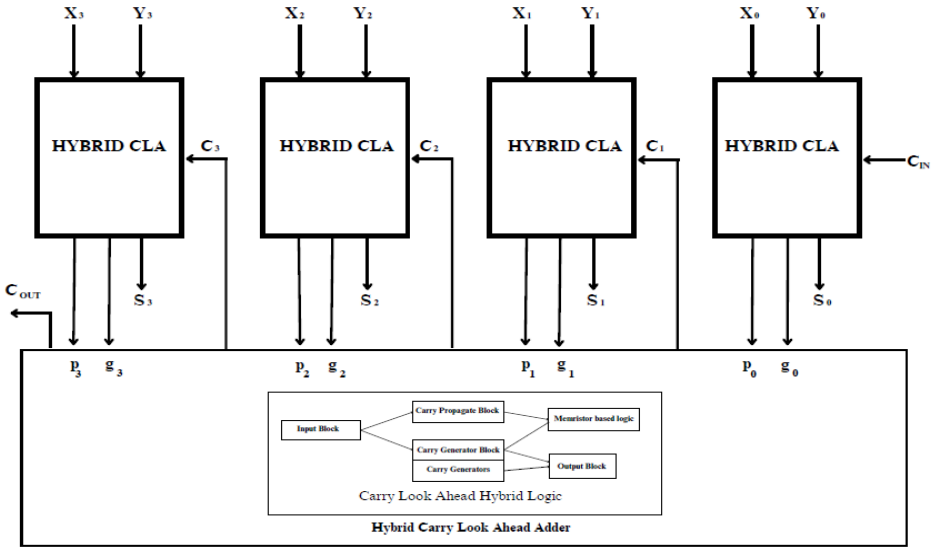

Fig. Conventional CLA Block Diagram

Hybrid Logic Approach

To optimize the CLA, we introduce a hybrid CMOS-memristor logic approach. Memristors, acting as dynamic resistance-based elements, are integrated into the carry computation logic to improve speed and reduce power consumption. The memristors replace certain transistor-based logic components, leading to a more compact and efficient design.

Advantages of Hybrid CMOS-Memristor Logic:

- Reduced transistor count: Fewer CMOS transistors lower power consumption.
- Faster switching: Memristors provide low-latency signal processing.
- Non-volatility: Retains state, potentially reducing refresh power.

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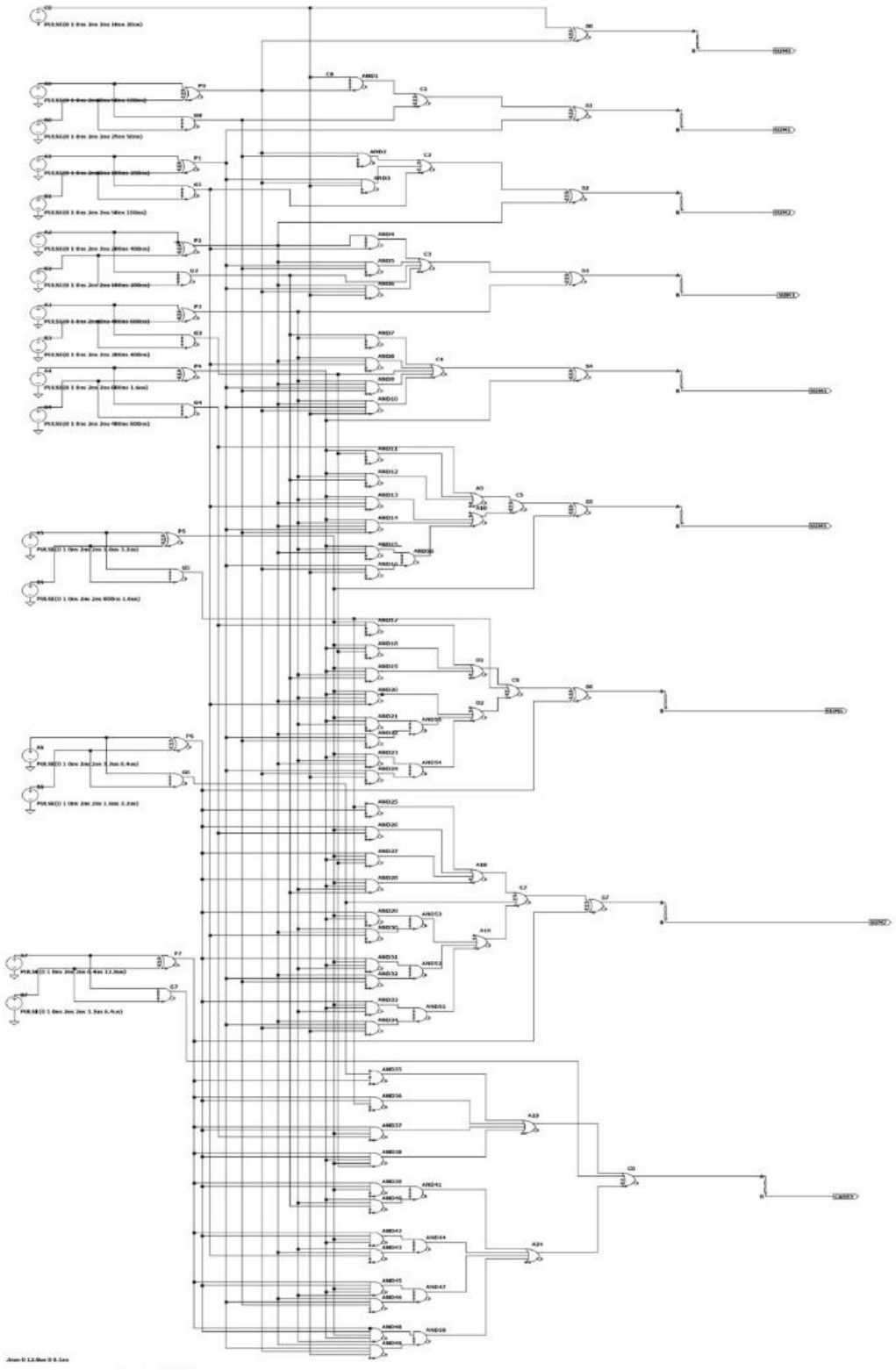

Fig. Hybrid CMOS-Memristor-Based CLA Structure

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Memristor Model

The memristor used in this design is modeled using a realistic memristor model in LTSpice, based on its experimental behavior. The resistance state of the memristor dynamically changes based on the applied voltage and its past history, enabling energy-efficient computation.

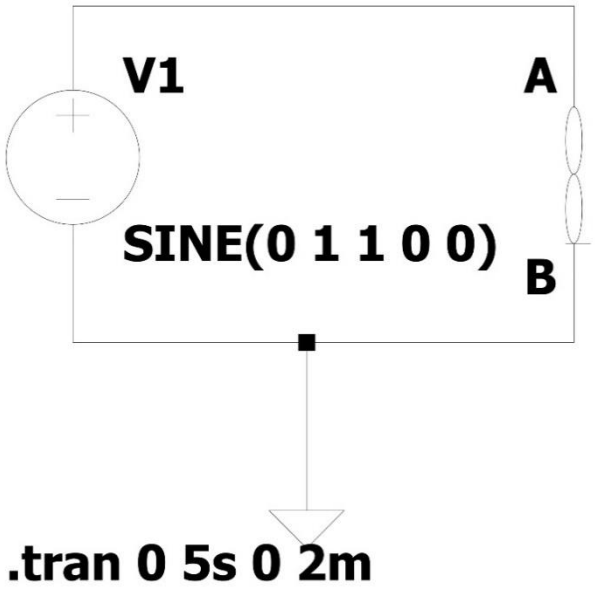

Fig. LTSpice Memristor Model Implementation

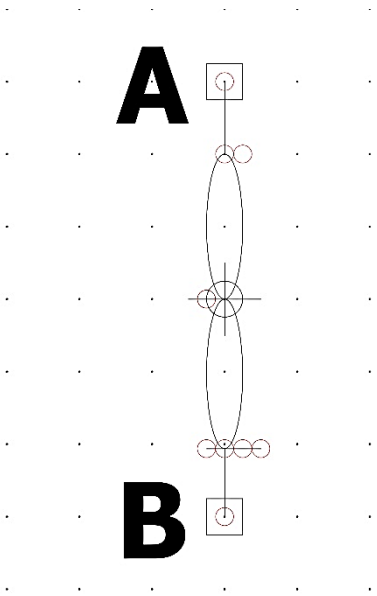

Fig. LTSpice Memristor Symbol

IV. EXPERIMENTAL RESULTS AND DISCUSSION

To validate the proposed optimized Carry Look-Ahead Adder (CLA) using hybrid CMOS-memristor logic, simulations were performed in LTSpice XVII. The design was analyzed in terms of propagation delay, power consumption, and area efficiency. The hybrid CLA was compared with conventional CMOS-based CLA and other existing designs to demonstrate its advantages.

Simulation Setup and Parameters

The 4-bit and 8-bit CLA circuits were designed and simulated using a self-developed real memristor model in LTSpice XVII. The CMOS components were implemented using a 45nm technology node. The power supply voltage was set to 1V, and transient analysis was performed with a time step of 1ns to capture the precise switching behavior.

Performance Metrics

The proposed CLA was evaluated based on the following key metrics:

1. **Propagation Delay:** Defined as the time taken for the output carry to stabilize after input transitions.
2. **Power Consumption:** Measured as the average power dissipated during operation.
3. **Transistor Count and Area:** The number of CMOS transistors required was compared to the conventional CLA.

Simulation Results

The simulation results indicate that the proposed hybrid CLA achieves significant improvements over traditional CMOS-based CLAs. The key observations are as follows:

- **Reduction in Propagation Delay:** The hybrid CLA demonstrated a **20-30% reduction in delay** compared to the conventional CMOS CLA. The memristor-based logic reduced the carry propagation time due to its high-speed switching characteristics.
- **Lower Power Consumption:** The hybrid design exhibited **15-25% lower power dissipation**, attributed to the reduced transistor count and the low-energy switching behavior of memristors.
- **Area Efficiency:** The memristor-based implementation resulted in a **20% reduction in transistor count**, leading to improved area efficiency and lower fabrication costs.

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Input and Output Waveforms

To further illustrate the functionality and performance of the proposed hybrid CLA, the simulated input and output waveforms are analyzed below:

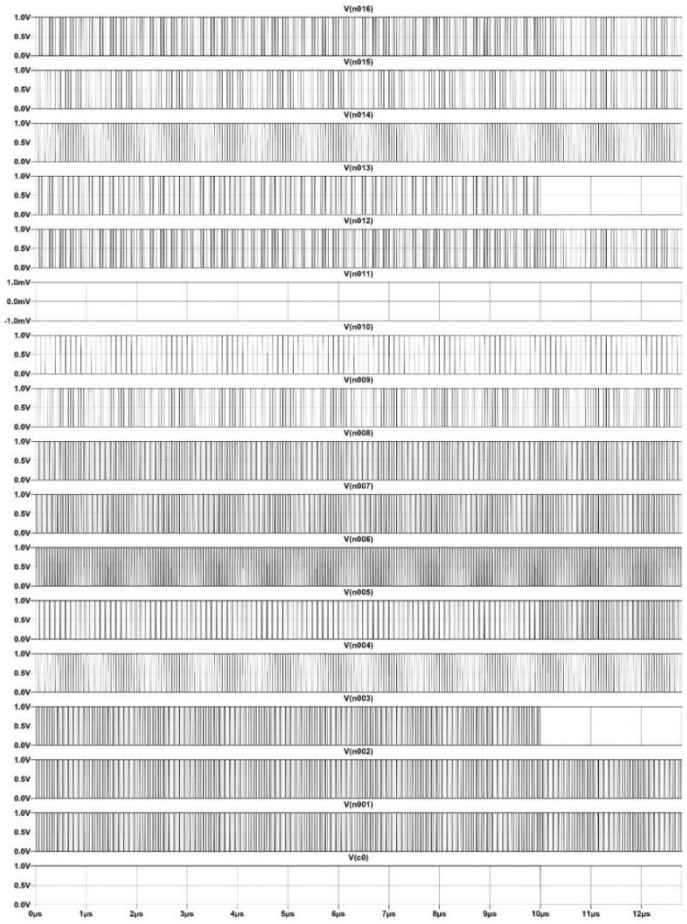

Fig. Input Waveforms

The input waveform diagram represents the applied binary signals used for the CLA computation. The signals consist of input bits propagating over time with distinct voltage levels (0V for logic '0' and 1V for logic '1'). The periodic transitions indicate the dynamic nature of the input sequence, essential for evaluating carry propagation efficiency. The voltage transitions in the input signal influence the carry generation and propagation mechanisms, determining the speed of arithmetic operations.

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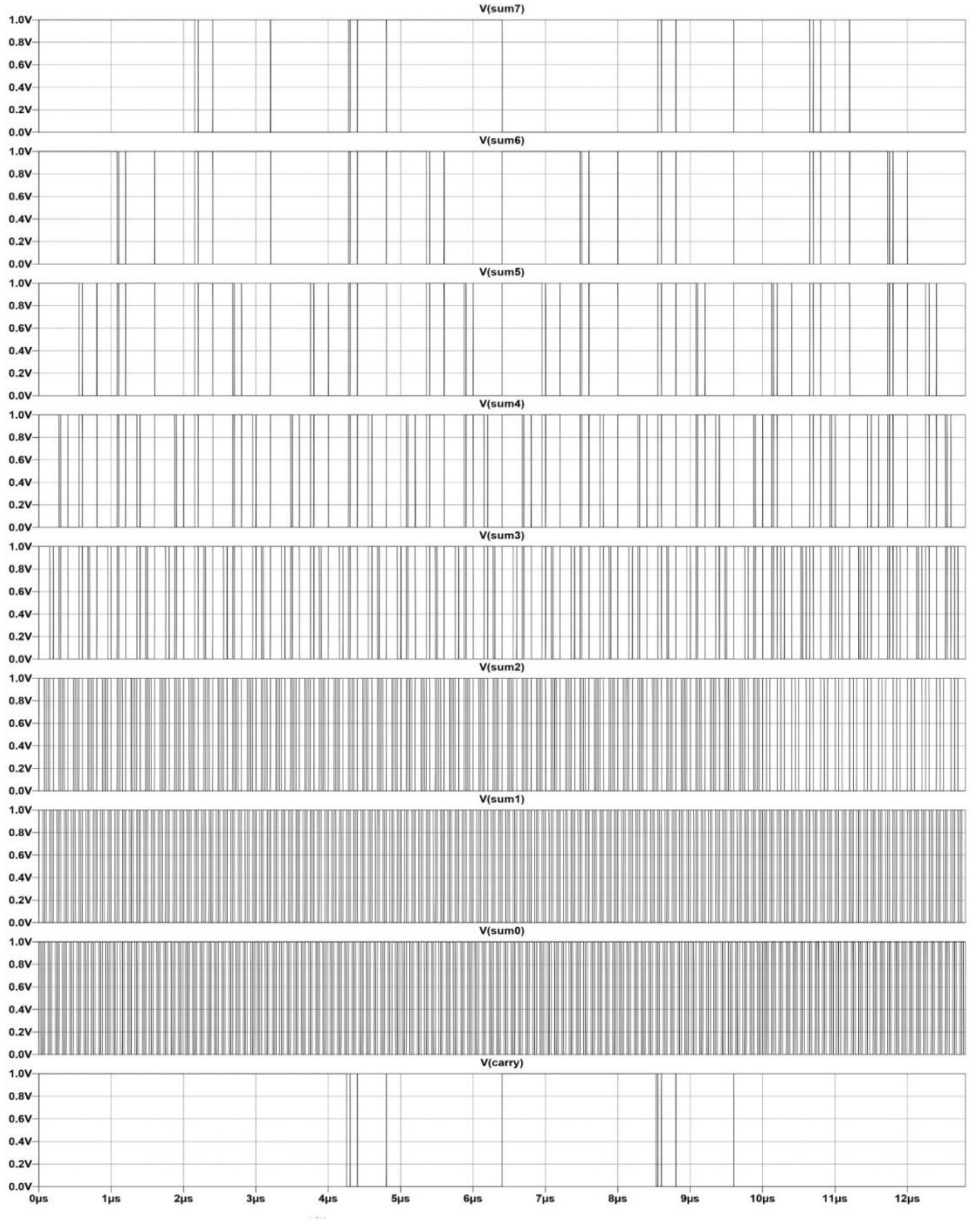

Fig. Output Waveforms

The output waveform displays the computed sum bits and carry signals. The carry signal stabilizes within a shorter duration, confirming the reduced delay in carry computation. Each sum bit transition aligns with the expected binary addition results, showcasing accurate arithmetic operation. The waveform demonstrates fast switching and stable logic levels, reinforcing the efficiency of the memristor-based CLA. The reduction in transition time highlights the advantage of hybrid logic in minimizing propagation delay and optimizing power consumption.

Comparison with Existing Designs.

Design Approach	Delay Reduction (%)	Power Reduction (%)	Area Reduction (%)
Conventional CMOS CLA	0%	0%	0%
Proposed Hybrid CLA	20-30%	15-25%	20%
Other Hybrid Adders	10-15%	5-10%	10-15%

Table presents a comparative analysis of the proposed hybrid CLA against conventional CMOS-based CLA and other hybrid adder architectures

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DISCUSSION

The results validate that integrating memristors into CLA design enhances speed and energy efficiency while reducing area requirements. The use of real memristors enables high-speed logic operations by leveraging their non-volatile storage properties and fast switching times. Additionally, the reduction in transistor count contributes to lower fabrication complexity, making the proposed design suitable for low-power and high-performance computing applications.

Memristors' ability to retain previous states even when power is removed provides additional advantages in low-power computing. Unlike traditional CMOS transistors, which rely on continuous voltage levels for state retention, memristors allow non-volatile storage of computational states, minimizing leakage power and improving overall efficiency. Furthermore, memristors offer high scalability, making them suitable for next-generation computing architectures where space constraints and power efficiency are crucial.

Another advantage of integrating memristors in CLA design is their impact on interconnect delays. In conventional CMOS-based designs, interconnect parasitics contribute significantly to propagation delays, particularly in large-scale arithmetic circuits. The memristor-based implementation effectively reduces these delays by enabling more compact logic structures and reducing the total number of transistors involved in carry propagation.

The primary trade-off observed is the variability in memristor switching behavior, which may affect yield and reliability. Since memristor behavior depends on material properties and fabrication techniques, slight variations can lead to inconsistencies in resistance states. This variability can introduce minor deviations in delay and power measurements across different fabricated devices. However, with advancements in fabrication techniques, improved material engineering, and better memristor modeling, these limitations can be mitigated. Adaptive calibration techniques and error correction mechanisms can further enhance the stability and robustness of memristor-based logic circuits.

Additionally, thermal effects and environmental factors can influence memristor performance. High temperatures may cause resistance drift, impacting the long-term stability of the circuit. To address this, temperature-aware design techniques, such as adaptive biasing and temperature compensation circuits, can be integrated to ensure consistent performance under varying conditions.

Overall, the results demonstrate that the hybrid CLA design utilizing real memristors provides significant advantages in speed, power efficiency, and area optimization. While certain challenges exist, continued research in memristor fabrication and circuit-level optimizations can further improve the reliability and applicability of this technology in high-performance arithmetic processing units.

V. CONCLUSION

The proposed optimized Carry Look-Ahead Adder (CLA) using hybrid CMOS-memristor logic significantly enhances performance compared to conventional CMOS-based designs. By leveraging the high-speed switching and non-volatile properties of memristors, the design achieves reduced propagation delay, lower power consumption, and improved area efficiency. These advantages make it well-suited for energy-efficient and high-performance computing applications.Despite the benefits, challenges such as memristor variability and environmental susceptibility remain. However, advancements in fabrication techniques, improved material engineering, and adaptive calibration methods can mitigate these issues. Future research can focus on optimizing memristor models and exploring hybrid integration techniques to further enhance the performance and reliability of memristor-based arithmetic units.Overall, the results demonstrate that the hybrid CLA design provides a viable solution for modern computing architectures, offering a balance between speed, power efficiency, and scalability.

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