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SEVEN LEVEL INVERTER IMPLEMENTATION WITH THE REDUCED SWITCHES BASED ON GRID CONNECTED PV SYSTEM

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Abstract: — Over the years, efficient renewable energy sources have become a dire need. Parallel, multilevel inverters have also been gaining traction for their applicability in solar applications as they provide transformer-less voltage control and allow even lowvoltage PV modules to be fed into the grid. But, PV integrated MLIs have low efficiencyand Harmonic Distortion. To help tackle this issue, this project proposes the implementation of a reduced switch cascaded seven-level inverter with a grid-connectedPV system. Using methods such as reducing the number of switches, RSCC andMSPWM. Reducing the number of switches enables us to reduce the switching losses ascompared to a normal cascaded MLI. However, the reduced switch topology causes voltage division, to tackle this MSPWM is implemented to obtain optimum switching angles to minimize the harmonics and RSCC helps stabilise the voltage. This paper findsthat reduced switch topology and MSPWM prove to be a better alternative for PV integrated systems, with higher efficiency and reduced harmonics.

Keywords: Seven level inverter, Photovoltaic system, Grid system, MulticarrierSinusoidal Pulse Width Modulation (MSPWM), Multilevel inverter (MLI).

I. INTRODUCTION

As a result of an increase in population, technological growth and development, the need for high quality, renewable sources of energy have increased over the years. Today there are various sources of renewable energy which are harvested such as wind energy, solar energy andso forth Converting sunlight into electricity using PV systems and connecting the same to the grid is one method to harness solar energy. But A PV panel generally has an output of 12V, which is insufficient for the grid. Hence to connect the PV system to the grid the DC current needs to be stepped up to the suitable range and inverted to AC. To achieve this, we will be components such as DC-DC Converter, MLI shows the proposed DC-DCConverter topology implemented in this paper.

There are various types of inverters such as square wave inverters, two-level inverters, multilevel inverters etc. A MLI provides the required output voltage by using various low-level DC voltages as input. As the number of levels increases, smoother the output wave and lover the harmonic distortions. However, a traditional MLI suffers from switching losses and hence reduced power quality. As the name suggests a reduced switch MLI, has fewer switches and hence the losses can be reduced and harmonics decreased by using a cascaded reduced switch MLI. The input voltage divider of the MLI is composed of three series capacitors. These DC capacitors in the MLI can cause voltage imbalance, this unbalance between the capacitors can causeharmonics in the output voltage and overvoltage across the switching devices, which isundesirable, and hence we propose controlling it using RSCC.

The MLI is controlled using pulse width modulation as a control method to obtain an accurate and required switching time. PWM holds the advantage that it has very low power lossas compared to other methods of regulating power output The controller is used to run the algorithm for MSPWM and give out the respective gate pulse signals for each switch using the GPIO pins. The gate signal from GPIO pins is fed to the gate driver circuit which usesTLP250 optocoupler to give out non inverting output in the desired voltage range to drive the MOSFETS in the inverter and RSCC. This paper give idea to implement a reduced switch MLIthat gives seven level voltage output in the range required such that it can

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be connected to the grid, with reduced total harmonic distortion and switching losses.

1.1 MOTIVATION

Traditional multi-level inverters typically require a significant number of switches, which leads to increased costs, power losses, and more complex control circuits. By reducing the number of switches, we cut down on both component costs and switching losses, enhancing the overall efficiency and affordability of the PV system. A seven-level inverter can produce a waveform that closely approximates a pure sine wave at the output. In a PV system, where the DC source voltage can fluctuate, a seven-level inverter can better utilize the various input voltage from solar panels to produce a stable AC output. This improves the energy conversion efficiency and maximizes the power harvested from the PV array.

1.2 OBJECTIVE

The main objective of this project is to implement inverter which a device or electric circuit that convert direct current to the alternating current is one of the electronic devices for generating a neat power source. The output will be seven level stepwise. They are capable to use in high voltage application with low harmonic also and easily provide the require levels needed by the high voltage drives. By achieving these objectives, the multilevel project will stabilize the quality of the output that will reduce the total internal distortion and reduce the noise this will help the green environment technology.

II. METHODOLOGY

The reduced switch MLI also produces seven output levels like the traditional H Bridge MLI but only uses eight switches as a result of which we can reduce switching losses. Fig.2 shows the circuit diagram of the proposed MLI. The input

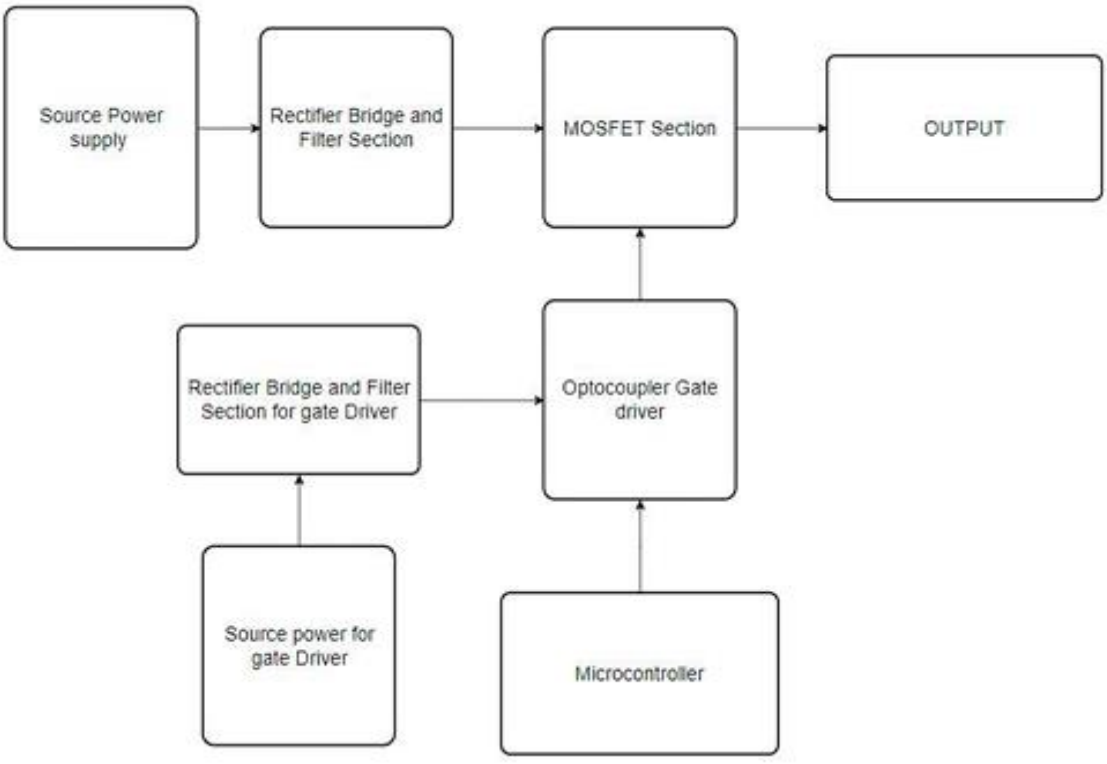

Fig: 1 Block diagram of SEVEN LEVEL INVERTER

After passing through the voltage divider the divided voltage is then supplied to the H-bridge which is made using MOSFETs, and four diodes. The voltage is then sent from the H-bridge to the output terminal which consists of four MOSFET. The MLI is controlled using pulse width modulation as a control method to obtain an accurate and required switching time. PWM holds the advantage that it has very low power loss as compared to other methods of regulating power output. The controller is used to run the algorithm for MSPWM and give out the respective gate pulse signals for

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each switch using the GPIO pins. The gate signal from GPIO pins is fed to the gate driver circuit which uses TLP250 optocoupler to give out non inverting output in the desired voltage range to drive the MOSFETS in the inverter and RSCC. This paper give idea to implement a reduced switch MLI that gives seven level voltage output in the range required such that it can be connected to the grid, with reduced total harmonic distortion and switching losses.

The primary task is to identify the hardware components which are suitable for this work. Block diagram consists of hardware components which are interconnected with each other to perform specific included power supply(0-12V) which is used as the input for the project, rectifier bridge and filter section, MOSFET section, optocoupler gate driver, gate driver and microcontroller by using this hardware components we can implement this project work.

Firstly, we are providing the DC input of 12V as the input power supply which is the step transformer of 220V-12V we are using the step-down transformer because the stepdown transformer reduces the voltage from the higher level to the lower level since multi-level inverter operates at the high voltage.

The rectifier bridge and the filter section is used to because the rectifier bridge counts the AC power source to the DC if the source power supply is AC. This is then DC is then filtered to remove any ripples to produce the pure DC this pure DC is then serves as a input to the MOSFET section. During the MOSFET section in this we use MOSFER connected based on the circuit diagram input is from the power supply and the control signal hence MOSFET is provided with the two inputs from the gate driver. The ON/OFF of the MOSFET is controlled by the microcontroller.

III. IMPLIMENTATION

3.1 Modes of operation:

Case1: For the output voltage level, Vo = ⅓ Vi, the switch Q1 is turned on for the positive half cycle. The switches Q5 and Q8 are also turned on and the energy is provided by capacitor C1 i.e. ⅓ Vi.

Case 2: For the output voltage level, Vo = ⅔Vi, the switches Q1 and Q4 are turned on. The switches Q5 and Q8 are also turned on and the energy is provided by capacitor C1 and C2 i.e. ⅔Vi.

Case 3: For the output voltage level, Vo = Vi, the switches Q1 and Q2 are turned on. The switches Q5 and Q8 are also turned on and the energy is provided by capacitor C1, C2 and C3 i.e Vi.

Case 4: For the output voltage level, Vo = -⅓ Vi, the switch Q2 is turned on for the negative half cycle. The switches Q6 and Q7 are also turned on and the energy is provided by capacitor C3 i.e. -⅓Vi.

Case 5: For the output voltage level, Vo = -⅔Vi, the switches Q2 and Q3 are turned on. The switches Q6 and Q7 are also turned on and the energy is provided by capacitor C3 and C2 i.e.- ⅔Vi.

Case 6: For the output voltage level, Vo = -Vi, the switches Q2 and Q1 are turned on. The switches Q6 and Q7 are also turned on and the energy is provided by capacitor C1, C2 and C3 i.e.- Vi.

4.1 Gate Driver operation:

The gate voltage is not sufficient for a good switch-on operation. In order to achieve a low switch-on resistance (Drain Source ON resistance), a considerably higher gate voltage must be applied, e.g. 10 V. In order to control the MOSFET with high impedance, i.e. to switch it off, the gate voltage must be permanently and significantly below the threshold voltage. The driver pulls to "low", but what does "low" mean? Clear answer, "low" should be zero Volt or at least almost zero Volt. When a logic high is given to “Drive Signal”, potential at Optocoupler pin 4 (emitter of Optocoupler transistor) is about +VCC with respect to the ground / negative terminal/point of supply – the separate/isolated power supply. This point is connected to MOSFET source. Thus, Q1 turns on. About +VCC, with respect to MOSFET source, is provided to MOSFET gate. Thus, MOSFET is driven on.
When a logic low is given to “Drive Signal”, Optocoupler pin 4 (emi er of Optocoupler transistor) is at the same potenti al as the ground / negative terminal/point of VCC – the separate/isolated power supply. So Q2 turns on and pulls MOSFET

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gate low. Thus, MOSFET is driven off. Note that the Optocoupler ground is the same ground as the ground of the MOSFET-based circuit. This driver can be used for any duty cycle – all the way from 0% to 100%. The driving frequency is limited by the speed of the Optocoupler. For high frequencies, optically isolated MOSFET drivers may be used instead of the two transistors and the Optocoupler – the optically isolated MOSFET driver will be all that's needed. Designers exclusively consider circuits that speed-up the turn-off process of the MOSFET. The reason is that the turn-on speed is usually limited by the turn-off, or reverse recovery speed of the rectifier component in the power supply. Therefore, the fastest switching action is determined by the reverse recovery characteristic of the diode, not by the strength of the gate drive circuit. In an optimum design the gate drive speed at turn-on is matched to the diode switching characteristic**.**

VI. RESULT

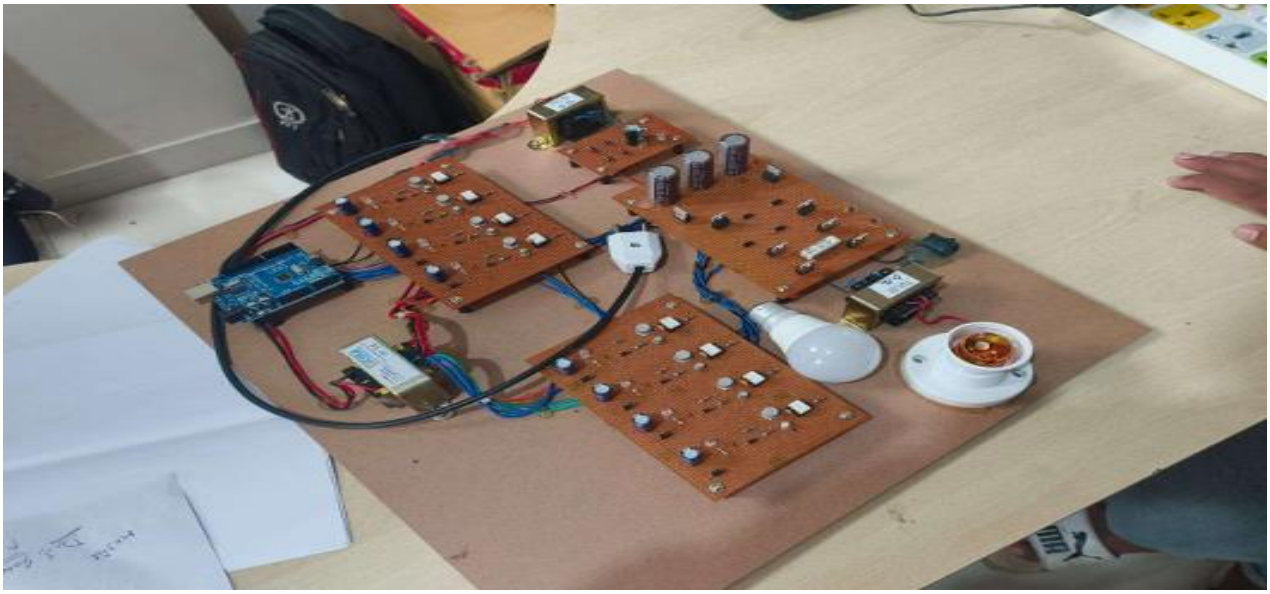

Fig 2: Prototype of model

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Fig 3: Sevel level output on the CRO

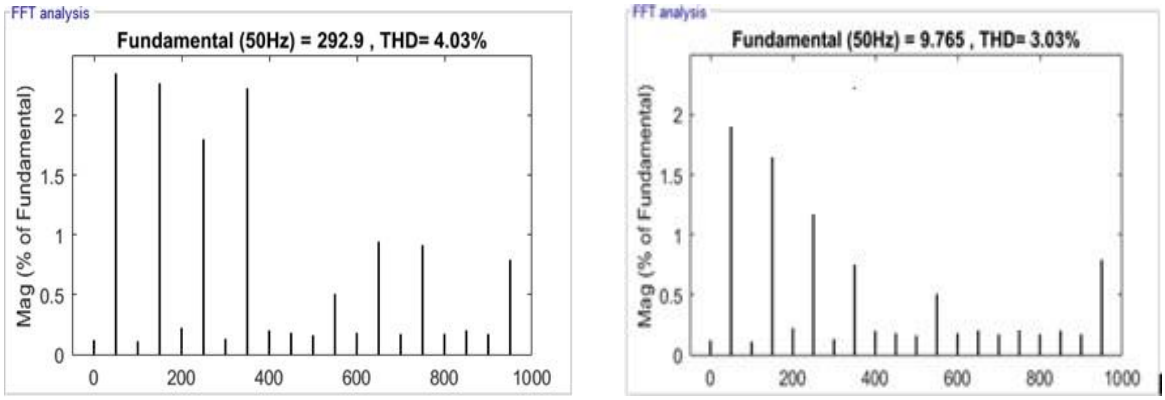

Fig 4: THD analysis of seven level inverter output voltage and output current

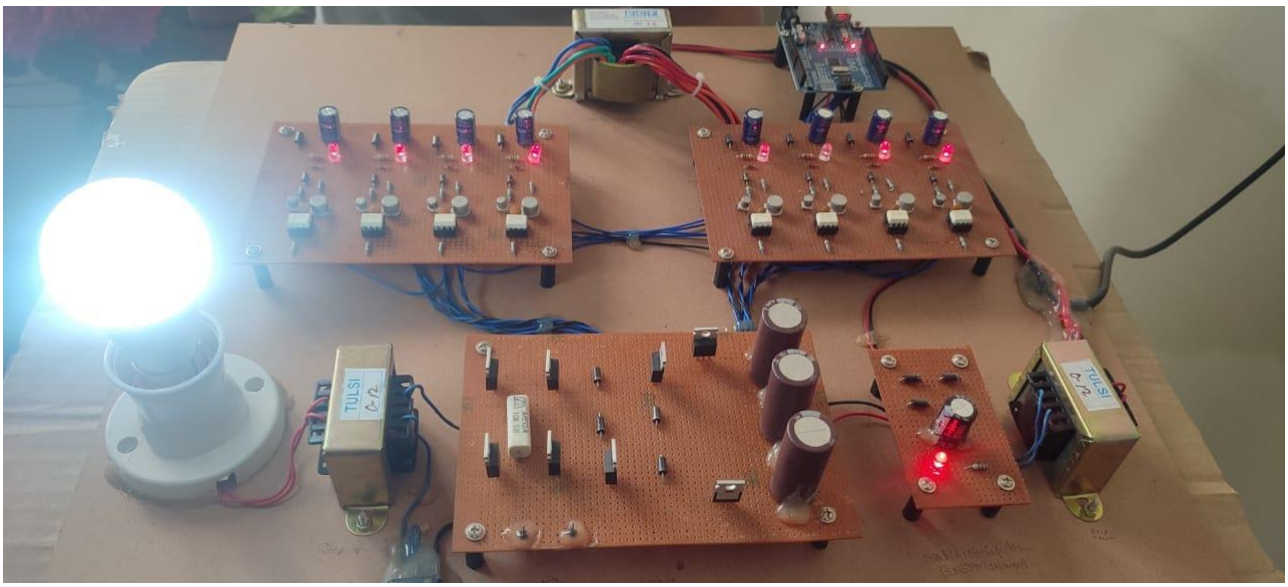

Fig 5: Inverter Working by Glowing the light

CONCLUSION

The reduced switch topology for the seven-level multilevel inverter was designed and implemented on a PV system and connected to the grid. Multicarrier sinusoidal pulse width modulation was used to provide the driving signal for the gate drivers. simulation was conducted and the results showed low Total harmonic distortion and high efficiency. The proposed system generates a seven-level output voltage with the help of eight power switches. It providesbetter performance compare other seven level inverter topologies and classical inverters. The highlights of the paper, A multilevel inverter is used in power conversion methodology for, high power applications and high voltage in today's power, transportation systems, transmission system and industrial work drives etc. Multilevel inverters are thus found to be very suitable for the voltage drive operation. Higher level inverters provide better performance as compared to lower-level inverters. Hardware, we implemented with atmega328 microcontroller. The output waveform tested in CRO in hardware project.

FUTURE SCOPE.

- While simulations validate the proposed system, real-world deployment and testing would help understand the performance under dynamic solar conditions, temperature variations, and real grid fluctuations.
- The concept can be extended to design nine-level or higher-level inverters using similar reduced switch methodologies to further reduce harmonic distortion and improve power quality.
- The inverter system can be enhanced to work in coordination with smart grid features such as real-time monitoring, fault detection, and demand-side management.

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- Future work could incorporate intelligent control strategies like fuzzy logic, neural networks, or adaptive modulation techniques to further optimize switching and reduce losses.
- It produces 2.5 times more power than regular position of the solar panel.

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