IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.471 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 14, Issue 6, June 2025

DOI: 10.17148/IJARCCE.2025.14677

Design And Verification of Low Power SRAM Memory Cells

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Abstract: As the demand for energy-efficient electronic devices continues to grow, the focus on low-power memory designs becomes paramount. Our Project presents a comprehensive study on the design and verification of low-power SRAM memory cells, addressing the critical need for energy-efficient memory solutions in contemporary electronic systems. The primary objective is to optimize SRAM cells for reduced power consumption while maintaining satisfactory performance and reliability. The basic 6T Static Random Access memory (SRAM) cell experience from relatively high static and total power loss problem, to solve this 4T SRAM cell is designed. As the technology is shrinking, a significant amount of attention is being paid on the design of high stability Static Random Access (SRAM) cells in terms of static Noise Margin (SNM) for different levels of cache memories. This project presents a qualitative design of 4T Static Random Memory Access cell in terms of Read cell current, Write time, Static Noise Margin (Read and Hold), Write Noise Margin in 45nm and 90nm CMOS technology.

Keywords: SRAM, CMOS, EEPROM, PMO, NMO, PMI.

I. INTRODUCTION

The electronic revolution has had a profound impact on the day to day lives of the people across the world. Continuous research in this field has resulted in electronic circuits and devices with greater capabilities, better efficiency, more reliability and lesser cost.

1.1Classification of Memory

Memory is the best essential element of a computer because computer can't perform simple tasks. The performance of computer mainly based on memory and CPU. Memory is internal storage media of computer that has several names such As majorly categorized into two types, Main memory and Secondary memory.

1. Primary Memory/Volatile Memory.

2. Secondary Memory/Non Volatile Memory.

1. Primary Memory/Volatile Memory:

Primary Memory also called as volatile memory because the memory can't store the data permanently. Primary memory select any part of memory when user want to save the data in memory but that may not be store permanently on that location. It also has another name ie. RAM.

Random Access Memory (RAM):
The primary storage is referred to as random access memory (RAM) due to the random selection of memory locations. It performs both read and write operations on memory. If power failures happened in systems during memory access then you will lose your data permanently. So, RAM is volatile memory. RAM categorized into SRAM, DRAM and DRDRAM.

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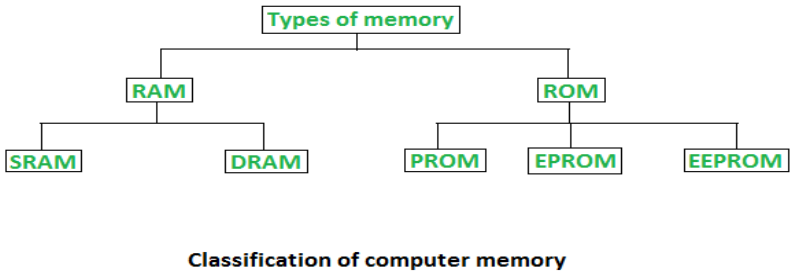

Fig 1.1: Classification of Memory

2. Secondary Memory / Non-Volatile Memory:

Secondary memory is external and permanent memory that is useful to store the external storage media such as floppy disk, magnetic disks, magnetic tapes and etc cache devices. Secondary memory deals with following types of components.

Read Only Memory (ROM):ROM is permanent memory location that offer huge types of standards to save data. But it work with read only operation. No data lose happen whenever power failure occur during the ROM memory work in computers.

ROM memory has several models such names are following.

1.PROM: Programmable Read Only Memory (PROM) maintains large storage media but can't offer the erase features in ROM. This type of RO maintains PROM chips to write data once and read many. The programs or instructions designed in PROM can't be erased by other programs.

2. EPROM: Erasable Programmable Read Only Memory designed for recover the problems of PROM and ROM. Users can delete the data of EPROM thorough pass on ultraviolet light and it erases chip is reprogrammed.

3. EEPROM: Electrically Erasable Programmable Read Only Memory similar to the EPROM but it uses electrical beam for erase the data of ROM.

4. Cache Memory: Mina memory less than the access time of CPU so, the performance will decrease through less access time. Speed mismatch will decrease through maintain cache memory. Main memory can store huge amount of data but the cache memory normally kept small and low expensive cost. All types of external media like Magnetic disks, Magnetic drives and etc store in cache memory to provide quick access tools to the users.

1.2 Types of Power Dissipation

Static power is power consumed while there is no circuit activity. For example, the power consumed by a D flip-flop when neither the clock nor the D input have active inputs (ie, all inputs are "static" because they are at fixed de levels).

Dynamic power is power consumed while the inputs are active. When inputs have ac activity, capacitances are charging and discharging and the power increases as a result. The dynamic power includes both the ac component as well as the static component.

II. LITERATURE REVIEW

1. Design and Analysis of 8× 8 SRAM Memory Array using 45 nm Technology at 100 MHz
Authors: Namgiri Snehith,E Santosh Kumar , Karumuri Srinivasa Rao
Published by:-IEEE Devices for Integrated Circuit (DevIC),2023
The development of memory and fabrication technology was pushed towards more compact design guidelines by the need for increased data storage capability. Every two years or so, the utmost achievable storage for data capacity for a single-chip semiconductor double .One Gigabyte of single chip read and write memory is currently commercially accessible and is used by many VLSI circuits for their subsystems [2]. However, as memory capacity grows, more

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processors are required, which raises power consumption. Modern digital systems must be able to store and retrieve large quantities of data quickly without consuming excessive power. A crucial design factor that affects storage capacity and consequently, the expense per bit of the memory is the number of stored information bits per unit area. Memory access time is the amount of time needed to write or retrieve data from a memory array . An essential memory array performance measure is access time, which controls memory speed. There are two kinds of memories: dynamic and static. In dynamic random-access memory, the information is stored on a capacitor and accessed via a semiconductor. The junction leaking current deteriorates the cell in formation [1]. As a result, it is unable to retain the data and must be periodically read or written to even when the cell is not being accessed. However, a latch is used in static random-access memory, so the cell data is held until the power is switched on. DRAM is frequently used for primary memory in personal and mainframe machines due to its cheap cost and high density . In microprocessors, mainframes, and engineering computers, SRAM is primarily used as cache memory. Left = Right = 20.32mm (0.8")

2. Retention Problem Free High Density 4T SRAM cell with Adaptive Body Bias in 18nm FD-SOI
Authors: Chandan Kumar, Rahul Kumar ,Anuj Grover
Published by:- 2022 35th International Conference on VLSI Design and 2022 21sInternational Conference on Embedded Systems (VLSID).
Shrinking technology is causing an increase in the transistor count on an SoC, implying that a greater amount of logic can be designed on the same area. However, SRAM bit cells do not keep pace with shrinking technology, which constraints area reduction on an SoC . To offset this limitation, many alternative bit cell topologies have been proposed . These need to be qualified for their respective bit cell Figures of Merit (FOMs) such as Static Noise Margin (SNM), Write Margin (WM), Cell Current, Retention, Leakage Current, Area, etc. There is a trade-off between some bit cell FOMs, which means that the designer may prefer an FOM and pick a corresponding bit cell, depending on the application.

3. Low Power Consumption Based 4T SRAM Cell for CMOS 130nm Technology
Authors: Anshul Goyal and Vimal Kumar Agarwal
Published by - International Conference on Computational Intelligence and C Networks CICN), 2022
The SRAM or Static RAM (Static Random Access Memory) is a semiconductor memory type which utilizes flip-flop (Bi-stable latching circuitry) to store every bit. The term static separates it from D- RAM or dynamic RAM that must occasionally be revived or refreshed. The SRAM shows information reminisces. However, it is still unpredictable in the traditional sense that the data/information gets inevitably lost when the memory isn't powered . In this paper, we propose 4T SRAM Cell which is able to reduce the power consumption and Area also. As we can see from the results session, power consumption of the 4T SRAM Cell get reduce up to 36% as compare to 6T SRAM Cell.

4. Design of Energy efficient and size reduced SRAM Cell
Authors: Sanjay G ,Suraj N K, Shruthi J and Roopa K Swamy
Published by:- IEEE- 2020
The electronic revolution has had a profound impact on the day to day lives of the people across the world. Continuous research in this field has resulted in electronic circuits and devices with greater capabilities, better efficiency, more reliability and lesser cost. The more we try to improve upon various parameters that govern the circuit's performance, the more are the challenges that we face. One of these challenges is the power requirement of the devices. The power dissipation should be kept as low as possible for two main reasons. First, in the case of portable electronic devices that operate on the battery, low power consumption would mean longer battery life. Second, more power consumption directly implies more heat dissipation; and such increase in the circuit's temperature could put its performance into jeopardy. There could be several approaches or means through which we could tackle the problem of power .

5. Design and Analysis of Area and Power Optimised SRAM Cell for High- speed Processor
Authors: Govind Prasad, Bipin chandra Mandi and Megha Jain
Published by: 2020 First International Conference on Power, Control and Computing Technologies (ICPC2T)
The SRAM is uses bistable locking equipment for securing bits [1]. A few qualities, for example, data transfer capacity control effectiveness make SRAMs perfect for the electronic machines, for example, PDAs, computerized cameras and hardware. A portion of the general employments of SRAMs are workstations, PCs, switches and other fringe types of gear, for example, CPU register records, switch cushions and hard circle supports, among others. Printers and LCD screens likewise use SRAM to spare the see of the picture printed or showed. Neural systems and adaptable hardware are developing open doors in SRAM advertise [2], [3]. The market for cell RAM is expanding at developing quickly and use and utilization of SRAM in cell gadgets is relied upon to support the market in coming time. The gadgets where SRAMs are utilized need it for either its rapid or its low power utilization [4], [5]. The SRAMs can hold rapid execution while lessening power utilization in a little bundle will offer a critical incentive in IoT applications [6], [7].

DOI: 10.17148/IJARCCE.2025.14677

There are two wide classes of SRAM based on application: Low Power (LP) is worked in low spillage forms and utilized for battery worked gadgets.

6. DESIGN OF HIGH SPEED ANDLOW POWER 4T SRAM CELL
Author: P. Pavan Kumar , Dr. R Ramana Reddy and M.Lakshmi Prasanna Rani
Published by: International Journal of Scientific and Research Publications, Volume 5, Issue 2, February 2015 1 ISSN 2250-3153
CMOS scaling has offered significant improvement in performance for the past four decades. However, as technology scaled down, standby power consumption was increased exponentially with the decrease of threshold voltage of MOSFET devices [1,2]. SRAM being one of the important sources of static power consumption demands its mere existence in most of the digital circuits. This challenge of optimizing the power consumption gives us the very need to design a new low power SRAM to enable the digital world set itself into miniature model.

7. Design of 6T, 5T and 4T SRAM Cell on Various Performance Metrics
Authors: Wazir Singh and G. Anil Kumar
Published by: 978-9-3805-4416-8/15/$31.00 @2015 IEEE
As the technology is shrinking, a significant amount of attention is being paid on the design of high stability Static Random Access (SRAM) cells in terms of static Noise Margin (SNM) for different levels of cache memories. This paper presents a qualitative design of 6T, 5T and 4T Static Random Memory Access cell in terms of Read cell current, Write time, Static Noise Margin (Read and Hold), Write Noise Margin in 65nm CMOS technology. Simulation results shows that the 6T SRAM cell exhibits 173% higher SNM than 4T SRAM cell which indicates that it is highly stable than 4T configuration.

III. PROPOSED SYSTEM

Static random-access memory is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

The term static differentiates SRAM from DRAM (dynamic random-access memory) which must be periodically refreshed. SRAM is faster and more expensive than DRAM; it is typically used for CPU cache while DRAM is used for a computer's main memory.

3.1 Lamda - Based Design Rules
A-based design rules are a set of rules that must be followed while designing the layout. It includes the dimensions of various layers that we use in creating the layout. The figure 1.2 summarizes the design rules.

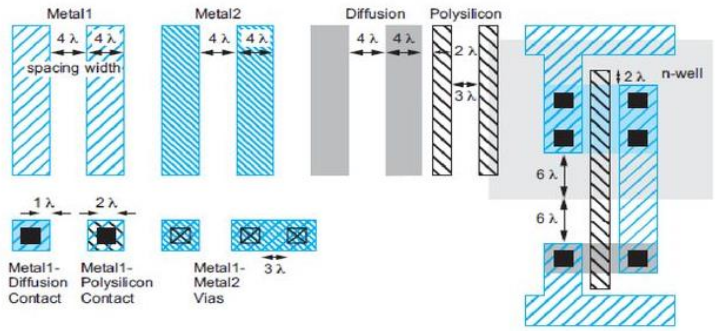

Fig 3.1.1 Lamda - Based Design Rules

3.2 4T SRAM

Static RAM is widely used in battery operated Embedded System. Where, we need to operate device at low power consumption and it's required less area as well as power efficient. Static RAM used in processors is very fast as compared to other memory storage medium as it needs less read and write timing [1].

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Low power SRAMs have turn into a significant part of many VLSI circuits because of its storage application. Rising size of on-chip memories particularly on components like microprocessors, makes SRAM's significant circuit, since its power consumption is high as compared to other circuit due to large number of cells used. Its high usage in processors makes it crucial circuit that decides the speed of processor. Also in different VLSI chips, the power dissipation has turn into a significant consideration due to the improved integration, operational speeds and the volatile enlargement of portable appliances.

With enhance in number of memory cells, additional power will be consumed still in the standby mode. The memory cells are frequently implemented by arrays of compactly packed SRAM cells for high performance, a lesser amount of leakage and power consumption optimizing the cell ratio of the cell and getting better the peripheral circuitry like precharge circuitry, write circuitry, sense amplifier etc. Cell ratio plays an significant role in stabilizing the output of the cell. The proposed cell is using a lesser amount of power supply, since the technology is scaled one. There are numerous configurations of memory cell that has been proposed

Conventional CMOS 6T SRAM cell is power competent in standby mode and has improved protection to transient noise and voltage variation than four transistor resistive load cell. That's why it is ideal over resistive load cell for high speed and low power applications [5]. Stable Data withholding remains, the main purpose when scheming any configuration of memory cell, Generally majority of the bits stored are '0'. To read a bit in the conventional 6T SRAM cell one of two bit-lines must be discharged to low apart from of written value. Due to balance in configuration the power consumption in both writing '0' and '1' are the usually same. This is also true in case of read operation. Since in cell, an irresistible majority of the write and read bits are '0', transitions always take place on bit lines in both writing '0' and reading '. Hence this causes high dynamic power consumption during read/write operation in conventional 6T SRAM cell. Our intention is to develop a SRAM cell with four transistors to decrease the cell area size with better performance and power consumption enhancement. In section II the 6T SRAM cell is presented. 4T configuration of the cell. This segment also discusses the working of the cell, about the read and write operation of the proposed cell, the leakage current of the cell and its calculation, delay at different nodes of the cell, circuitry of the cell including pre-charge, write and sense amplifier circuitry.

3.3 Cell Structure

A circuit configuration of 4T SRAM is shown in Figure 3.14. In this circuit instead of NMOS, PMOS is used as a pass transistor. Stored bit are available at nodes ST and STB. PM2 (pass transistor) is key factor through which we invoked data read and write operation at BL. (bit line) whose controlling signal is WL (word line). In inactive mode of cell (when read or write operation not perform) PM2 is OFF. When '0' stored at ST node PMO is ON and STB node pulled up to VDD. When 'I' stored at ST node NMO is ON and STB node pulled down to GND. As STB node goes "low" then PMI will be ON and ST node pulled up to GND (where transistor PMI is used as refresh circuit). Signal 'high' stored at ST node uses leakage current at input-output point BL. (BI, is pre-charge with VDD) through pass transistor PM2.

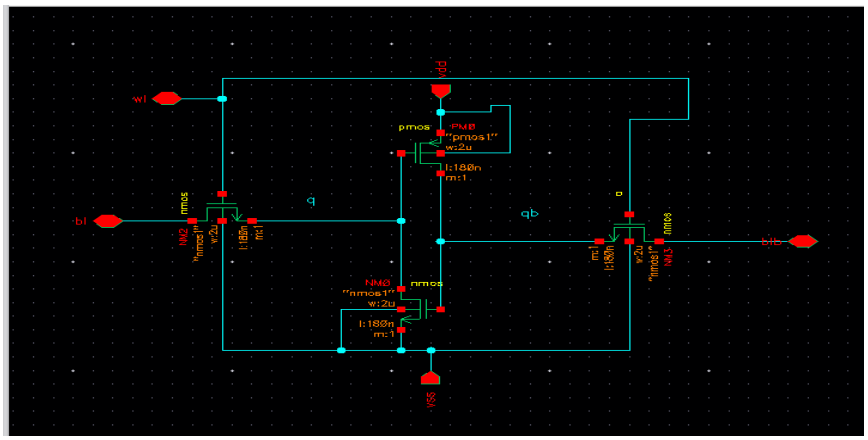

Fig 3.3.1: Schematic of 4T SRAM

3.4 Static Noise Margin (SNM)

- Definition: SNM is a measure of the stability of a memory cell, indicating how much noise the cell can tolerate without losing its stored information.

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- Importance: A higher SNM is desirable as it ensures better reliability and robustness against various factors that can introduce noise or disturbances in the memory cell.

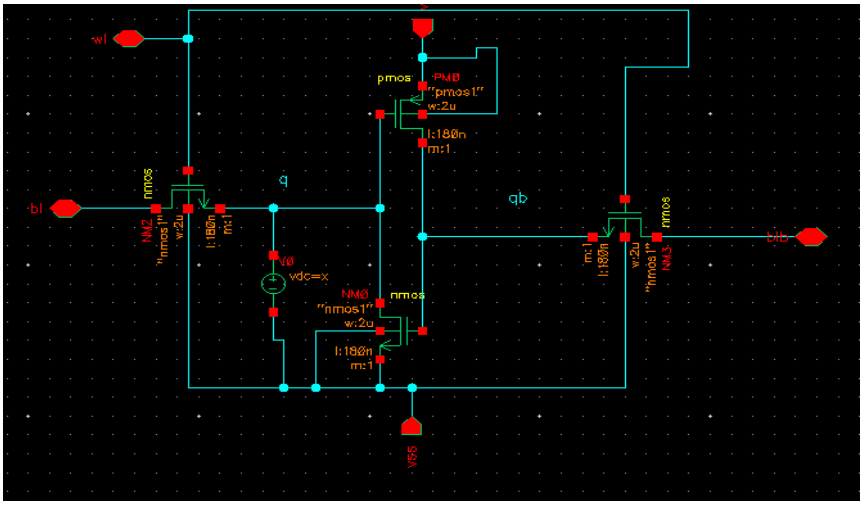

Fig 3.4.1: SNM Schematic of 4T SRAM

3.5 Sense Amplifier Circuit:

A sense amplifier is a crucial component in the operation of SRAM (Static Random Access Memory) during read operations. SRAM cells store data in a cross-coupled flip-flop configuration, and during read operations, the sense amplifier is responsible for detecting and amplifying the small signal stored in the SRAM cell to a level that can be reliably interpreted as either a '0' or '1'. Let's break down the working of a sense amplifier in the context of an SRAM read operation:

Word line Activation: The read operation starts by activating the word line associated with the SRAM cell that needs to be read. The activated word line connects the selected SRAM cell to the bit lines.

Bitline Precharging: Before the read operation, the bitlines (BL and /BL) are precharged to a certain voltage level (typically halfway between the power supply rails) to ensure a proper reference level.

1. Cell Transistor Conduction:

When the wordline is activated, it allows the SRAM cell to be connected to the bitlines. The conduction of the cell transistors affects the potential on the bitlines based on the stored data in the SRAM cell.

2. Differential Voltage on Bitlines:

The SRAM cell's stored data creates a small differential voltage between the true bitline (BL) and the complementary bitline (/BL). This differential voltage is relatively weak due to the small size of the SRAM cell transistors.

3. Sense Amplifier Activation:

The weak differential voltage on the bitlines is then sensed and amplified by the sense amplifier. The sense amplifier is designed to quickly detect and magnify this small voltage difference.

4. Positive Feedback:

The sense amplifier typically uses positive feedback to latch onto and reinforce the detected voltage difference, quickly driving one of the bitlines to a high voltage and the other to a low voltage.

5. Output Generation:

The final output of the sense amplifier is a strong differential signal that represents the stored data in the SRAM cell. This amplified signal is then used to generate the output data of the SRAM for further processing or to drive other parts of the memory hierarchy.

The sense amplifier's role is critical for achieving fast and reliable read operations in SRAM. Its ability to quickly and accurately amplify the small signals from the SRAM cell is essential for maintaining the integrity of the stored data. The use of sense amplifiers enables SRAM to have fast access times and high-speed read operations, making it suitable for applications where speed is crucial, such as cache memory in computer systems.

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3.5 Write Operation

During write operation Pass transistor PM2 is ON and subsequent operations are performed on different transistors and nodes in the proposed SRAM cell:

1) Bit-line driving: For the write operation, information (data) is set on bit-line (BL), and then word-line (WL) asserted to GND. 2) Cell flipping: This step includes two states as follows:

a) Data is zero: In this state, ST node pulled up to GND bypass transistor PM2, and therefore the Load transistor PMO will be ON, and STB node will be pulled up to VDD.

b) Data is one: In this state, ST node pulled up to VDD bypass transistor PM2, and therefore the drive transistor NM0 will be ON, and STB node will be pulled down to GND and positive feedback created by PMI and NMO.

3) Bit-line driving: At the end of write operation, cell will go to idle mode and WL and bit-line asserted to VDD and VDD, respectively.

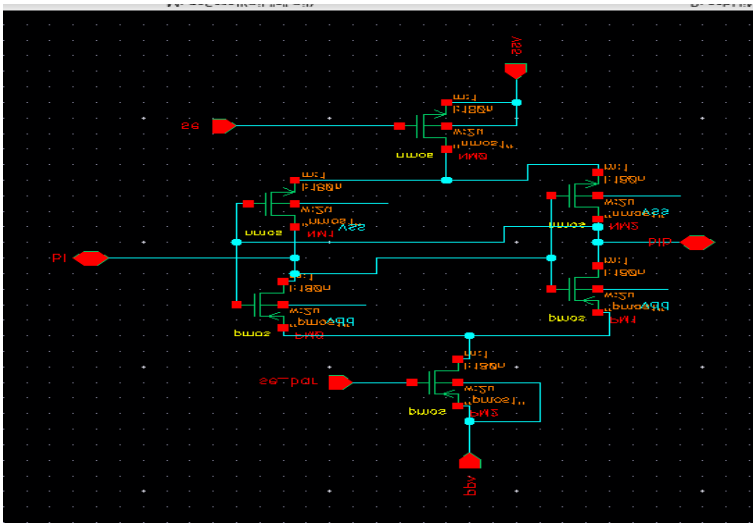

Fig 3.5.1: Schematic of 4T SRAM for write operation

3.6 Hold State Operation of 4T:

- The SRAM cell holds its state by maintaining the cross-coupled inverters in a stable configuration. The feedback loop between the inverters keeps the stored data intact.
- The transistors within the SRAM cell operate in their saturation regions to ensure a robust and stable operation.

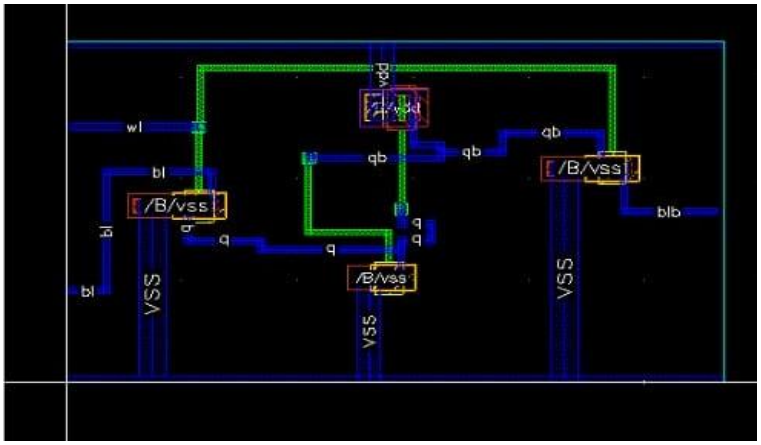

Fig 3.6.1 Layout diagram of the proposed 4T SRAM

The proposed 4T SRAM cell is dealt on the characteristics of reduced number of transistor count, area and the power. The values tabulated of the area and power dissipated is observed in 45nm technology using the Cadence tool. Cadence

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tool helps us to design our own circuit and also to verify it's working. It offers various tools to meet and improve the performance of the circuit and also to reduce the power consumption. In this design we are dealing with the reduced power and area.

Transistor Arrangement: The layout diagram shows the arrangement of the four transistors that make up the 4T SRAM cell. These transistors are typically arranged in a symmetrical layout to minimize the cell size and ensure balanced operation.

Storage Nodes: The layout includes the storage nodes, usually labeled as Q and QN, which store the complementary bit values. These nodes are connected to the storage transistors (TS1, TS2) and are essential for storing and retrieving data from the cell.

Access Transistors: The diagram also shows the two access transistors (TA1, TA2) that control the connection between the storage nodes and the bitlines (BL and BLB). These transistors enable read and write operations on the SRAM cell. Overall, the layout diagram of a 4T SRAM cell in VLSI design is a complex arrangement of transistors, storage nodes, and interconnects designed to provide reliable and efficient memory storage in integrated circuits.

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IV. RESULTS

Power Comparison of 4T SRAM Cell with 90nm and 45nm Technology

Table 4.1 Power analysis

Operation	90nm	45nm
READ	**13.5583mW**	**493.6908uW**
WRITE	**242.2072mW**	**142.2072uW**

Delay Comparison of 4T SRAM Cell with 90nm and 45nm Technology

Table 4.2 Delay time analysis

Operation	90nm	45nm
READ	**0.856ns**	**45.16ps**
WRITE	**1.8224ns**	**99.95p s**

V. CONCLUSION AND FUTURE WORK

The implementation of leaf disease detection coupled with targeted pesticide spraying presents a promising approach for sustainable agriculture. By leveraging CNN architectures for accurate disease identification, farmers can efficiently

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monitor crop health and intervene only where necessary, minimizing pesticide usage and environmental impact. However, future work should focus on enhancing the scalability and real-time deployment of these systems, integrating them seamlessly into existing agricultural practices. Additionally, advancements in sensor technology and data processing algorithms could further optimize detection accuracy and reduce false positives.

Collaborations between researchers, farmers, and industry stakeholders will be crucial in refining these systems and ensuring their practicality and effectiveness in diverse agricultural settings. Ultimately, continued innovation in this field holds the potential to revolutionize crop management practices, promoting both environmental sustainability and agricultural productivity.

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