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DESIGN AND IMPLEMENTATION OF DIGITAL PID CONTROLLER USING FPGA

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Abstract: This paper presents the design and implementation of a digital Proportional-Integral-Derivative (PID) controller using Field Programmable Gate Array (FPGA) for precise speed control of a DC motor. The proposed PID controller enhances motor speed stability by continuously generating the control signal in real time using the difference between the reference speed and the measured motor output. The digital PID controller demonstrates efficient motor speed regulation, reduces the steady-state error, and fast response time. This FPGA-based implementation offers flexibility, scalability, and high-speed operation, making it suitable for various industrial automation and embedded control applications.

Keywords: Digital pid controller, FPGA implementation, dc motor control, Verilog hdl.

I. INTRODUCTION

The Proportional–Integral–Derivative (PID) controllers are widely used in industrial control systems due to their simple structure, reliability, and effectiveness in regulating dynamic processes. They are commonly applied in motor speed control, robotics, process control, and automation systems to maintain the desired output by minimizing the error between the reference setpoint and the actual system response. Conventional PID controllers are commonly realized using analog hardware or microcontroller-based digital platforms; however, such implementations often face drawbacks including slower dynamic response, restricted parallelism, and limited adaptability for complex control applications.

DC motor speed control and temperature regulation have been extensively investigated using microcontroller-based PID controllers. Although these approaches provide satisfactory control results, they are often constrained by limited computational speed, sequential processing, and a lack of flexibility when implementing complex control algorithms. Several researchers have implemented digital PID controllers on FPGA platforms to overcome these limitations. Studies by Agarwal et al. implemented FPGA-based PID controllers using VHDL for DC motor speed control, achieving faster response and improved accuracy. Other works utilized modeling and simulation approaches to optimize controller parameters before hardware implementation, while distributed arithmetic techniques were proposed to enhance computational efficiency and reduce hardware resource usage. Additionally, FPGA-based PID control has been successfully applied to industrial applications such as refrigeration temperature control, demonstrating stability and robustness.

Despite these advancements, many existing designs rely on fixed controller parameters, limited scalability, or high hardware resource consumption. In this work, the identified limitations are overcome by designing an optimized digital PID controller implemented on an FPGA platform. The proposed method provides higher adaptability, optimized utilization of hardware resources, faster real-time performance, easier adjustment of control parameters, and better robustness across varying operating conditions. As a result, the current work provides a scalable, high-speed, and reliable control solution suitable for modern real-time control applications.

In this work, a PID controller is proposed for implementation on an FPGA platform. With the continuous advancement of digital hardware technologies, Field Programmable Gate Arrays (FPGAs) have emerged as a powerful platform for implementing digital control algorithms. FPGAs offer high-speed computation, parallel processing, reconfigurability, and deterministic timing behavior, making them highly applicable for the real-time control applications. An FPGA-based digital PID controller is capable of executing proportional, integral, and derivative computations efficiently, ensuring precise control action and stable system performance. The digital nature of the implementation allows accurate parameter tuning, reduced noise sensitivity, and repeatable performance.

In FPGA-based digital PID control systems, the control logic is implemented by using the hardware description language such as Verilog or VHDL, which enables the accurate timing control and efficient management of hardware resources.

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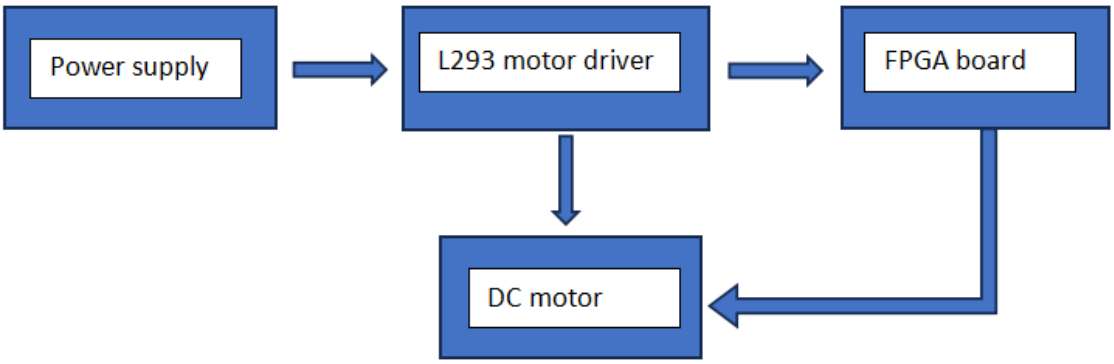
The digital implementation enables easy tuning of PID parameters, improving noise immunity, and seamless integration with peripherals such as sensors, encoders, and motor drivers.
In an FPGA-based digital PID controller can be used either fixed-point or floating-point arithmetic. Additionally, FPGAs enable direct integration of control logic with signal conditioning, sensor interfacing, and actuator driving modules on a single chip, reducing system complexity and hardware cost.
In summary, FPGA-based digital PID controllers offer a highly adaptable, scalable, and efficient solution for contemporary embedded and industrial automation applications, where rapid response, accuracy, and dependable operation are essential.

II. PROPOSED PID CONTROLLER

The block diagram illustrates an FPGA-based DC motor control system. The power module provides the necessary voltage and current to all system components, ensuring stable and reliable operation. The FPGA board acts as the main control unit, where the PID controller is implemented. L293 motor driver, which serves as an interface between the low-power FPGA signals and the high-power DC motor. Since the FPGA cannot directly drive the motor due to current and voltage limitations, the L293 driver amplifies the control signals to suitable levels. The motor driver then supplies the required voltage and current to the DC motor, enabling it to rotate at the commanded speed. The integral action in a PID controller serves to increase the low-frequency gain, which in turn reduces the steady-state error. By accumulating the error over time, the controller ensures that the system reaches the desired set-point more precisely. The derivative component provides phase lead to the control system, improving overall stability and increasing bandwidth, which results in quicker response and more effective handling of rapid dynamic variations.



Block diagram of a proposed PID controller

The power module supplies the required voltage and current to all components of the system, ensuring the stable and reliable operation. The power supply 5V is given to the controller. The motor driver, acting as an interface, converts the low-power control signals from the FPGA into suitable inputs for the motor. An H-bridge driver IC, such as the L293 motor driver, is used to handle the higher current requirements, and direction inputs from the FPGA to control motor speed, rotation direction, and ON/OFF operation, with driving power taken directly from the supply block.
At the core of the system, the FPGA board executes the PID controller written in Verilog or VHDL, continuously processing user commands or sensor feedback to achieve precise regulation.

III. DIGITAL PID CONTROLLER

The classical PID controller in continuous time is given by:

$$u(t) = Kp\, e(t) + Ki \int_0^t e(\tau)d\tau + \mathrm{Kd}\, \frac{\mathrm{de(t)}}{\mathrm{dt}}$$

Where:

- $u(t)$ is the control output,
- $e(t) = r(t) - y(t)$ is the error between reference input $r(t)$ and output $y(t)$,
- Kp is the proportional gain,
- Ki is the integral gain,
- Kd is the derivative gain.

In digital control systems, the controller output is calculated at specific discrete sampling instants denoted by nT Let:

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- $e[n] = e(nT)$
- $u[n] = u(nT)$

The discrete-time PID controller is approximated as:

$u(n) = u[n-1] + Kp(e[n] - e[n-1]) + Ki\,Te[n] + Kd(e[n] - 2e[n-1] + e[n-2])/T$

Proportional Term:

$P[n] = Kp.e[n]$

Integral Term (using trapezoidal or rectangular sum):

$II[n] = I[n-1] + Ki.T.e[n]$

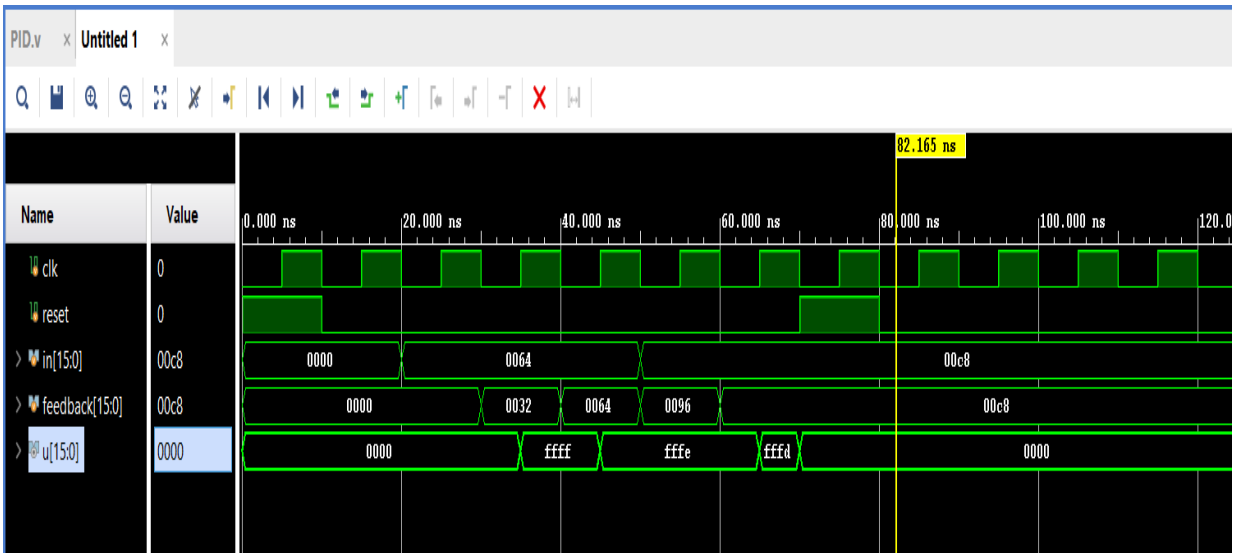
Derivative Term (finite difference approximation):

$D[n] = Kd.e[n] - e[n-1]/T$

Control Output:

$u[n] = P[n] + I[n] + D[n]$

IV. SIMULATION RESULTS OF PID CONTROLLER



The PID controller waveform simulation demonstrates how the control signal (u1) responds to changes in the setpoint (in1) and the feedback input.. Initially, the system is in the state of reset (reset = 1), which keeps all internal states, including the control signal, at zero (u1 = 0000). Once the reset is deasserted (reset = 0), a setpoint of 00C8 (decimal 200) is applied, while the feedback is initially zero. This large positive error causes the PID controller to quickly respond, as seen by the increase in u1.As feedback gradually increases to reduce the error (values like 0032, 0064, and 0096), the error becomes smaller, and the PID controller's output begins to decrease in magnitude. Notably, the u1 value transitions from FFFE to FFFA (in signed 16-bit format, these represent small negative values), indicating a shift in control direction—possibly due to derivative action responding to the rapid change in error.

At time 82.165 ns, the setpoint changes to match the feedback at 00C8 (200), making the error zero. Consequently, the control signal (u1) returns to 0000, indicating a stable state where no further corrective action is needed. This behavior confirms that the PID controller effectively adjusts its output to reduce error over time and stabilizes when the setpoint is achieved.

V. HARDWARE RESULTS

The circuit shows an FPGA-based digital PID controller realized on the **Basys-3 Artix-7** development board for controlling the speed of a DC motor. An external **12 V DC source** is used as the main supply and is stepped down through

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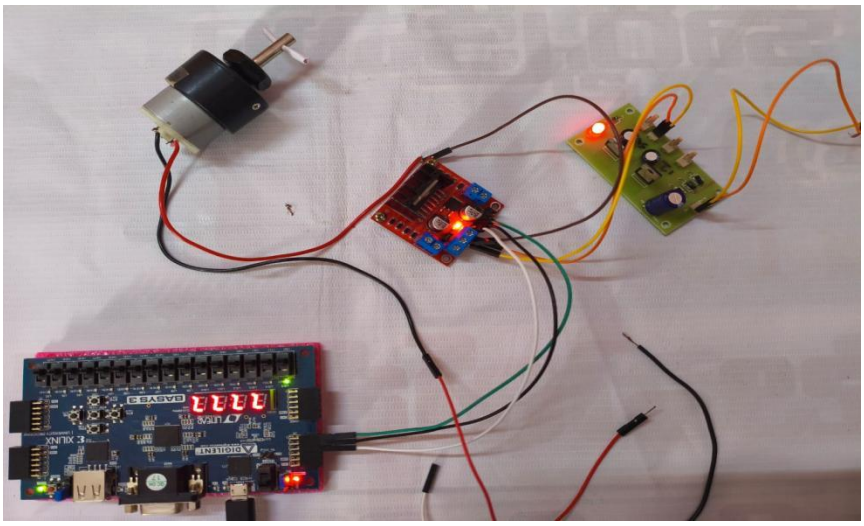
an adapter to provide a regulated **5 V** suitable for the FPGA and associated peripheral components. The regulated power supply is connected to the **VCC and GND** terminals of the motor driver. The pins on the FPGA board **Enable A, B1, and B2** are interfaced with the motor driver. The motor driver outputs are connected directly to the DC motor. The motor speed is adjusted by operating the **3-bit switches** on the FPGA board, which vary the control input accordingly.



VI. SWITCH CONFIGURATIONS

The table defines how the 3-bit switch input (SW2-SW0) selects different operating modes of the DC motor. Each switch combination corresponds to a specific action - stop, forward slow, forward fast, or reverse allowing the user to control speed and direction through simple digital inputs.

SW2	SW1	SW0	Mode	Motor Action
0	0	0	Stop	No rotation
0	0	1	Forward slow	Rotate slowly forward
0	1	1	Forward fast	Rotate faster forward
1	1	1	Reverse	Rotate reverse

VII. CONCLUSION

The FPGA-based digital PID controller presented in this work effectively delivers accurate and stable speed regulation for a DC motor. By continuously computing the proportional, integral, and derivative components of the error signal, the controller ensures fast and accurate control action. Experimental results demonstrate reduced steady-state error, improved stability, and quicker transient response compared to conventional control methods. Due to their simple architecture, adaptability, and consistent performance, PID controllers remain extensively used in various industrial control applications. Furthermore, the adoption of FPGA technology provides high computational speed, flexibility, and scalability, making the proposed approach suitable for modern embedded and industrial automation systems.

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FUTURE SCOPE

An FPGA-based digital PID controller holds significant role for future advancements in intelligent control systems. It can be extended to include adaptive tuning mechanisms using machine learning or fuzzy logic, allowing the PID gains (Kp, Ki, Kd) to adjust automatically in real time based on system behavior. The PID controllers can also be scaled to support multi-motor or multi-axis systems, such as robotic arms or autonomous vehicles, by leveraging the parallel processing capabilities of FPGAs. Additionally, integration with IoT for remote monitoring and control through wireless or serial communication protocols can make the system suitable for smart industry applications. Porting the design to FPGA-SoC platforms like Xilinx Zynq would combine hardware speed with software flexibility, enabling more complex interfaces and real-time diagnostics. Moreover, with optimization, the system can be made energy-efficient for use in battery-powered or green energy environments, making it highly relevant for future industrial and embedded automation systems.

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