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"OPTIMIZED VLSI DESIGN FOR REAL-TIME EDGE DETECTION"

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Abstract: Edge detection is a foundational operation in computer vision and embedded image processing, enabling systems to identify structural boundaries and salient features within visual data. Real-time implementation of edge detection remains challenging in software platforms due to high computational load and latency. To address this limitation, a hardware-optimized VLSI architecture implementing the Sobel operator is proposed for real-time video edge extraction. The system acquires live frames through a VGA camera, performs grayscale conversion, calculates horizontal and vertical gradients using Sobel convolution masks, and computes edge magnitude before applying thresholding. Implemented on the Artix-7 FPGA using Verilog HDL, the design leverages parallelism, pipelining, on-chip memory optimization, and low-power computation. Experimental evaluation demonstrates significant improvements in throughput, latency, and resource efficiency over traditional software-based methods. The architecture is suitable for embedded vision applications such as surveillance, robotics, and smart IoT cameras.

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Keywords: Sobel, VLSI, FPGA, Edge Detection, Verilog, Real-Time Video Processing.

I. INTRODUCTION

Edge detection aims to identify sharp intensity changes in an image, which signify meaningful transitions such as object boundaries, shape contours, and texture variations. It represents a crucial preprocessing step in high-level vision tasks including segmentation, recognition, autonomous navigation, and motion tracking. Classical algorithms such as Sobel, Prewitt, Roberts, Scharr, and Canny have been widely used for edge extraction. However, deploying these methods on CPUs or microcontrollers leads to significant processing delays, especially for video streams.

Field-Programmable Gate Arrays (FPGAs) offer a promising alternative by providing parallel computation, configurable logic, pipelines, and low-power operation, making them ideal for real-time image processing. The Sobel operator, due to its simple mask-based arithmetic and robustness to minor noise, is highly suitable for FPGA-based implementation. This work presents a complete VLSI architecture for real-time Sobel edge detection. The system comprises live video acquisition using a VGA camera, grayscale conversion, Sobel gradient computation (Gx, Gy), magnitude calculation, thresholding, buffering, and VGA-based display. All modules are designed in Verilog HDL and synthesized on an Artix-7 FPGA platform. This ensures fast, deterministic, and energy-efficient edge extraction suitable for embedded video applications.

II. METHODOLOGY

The proposed system follows a systematic hardware-centric methodology for achieving real-time video edge detection on an FPGA platform. Live video frames are first captured using a VGA camera module, which streams pixel data to the FPGA in RGB format. Since direct processing of RGB components increases computational complexity, the frames are immediately converted into grayscale using a hardware-efficient weighted approximation, thereby reducing the data width and simplifying subsequent operations. To enable 3×3 neighborhood processing required for Sobel convolution, the incoming grayscale pixel stream is passed through line buffers implemented using on-chip BRAM, which generate three parallel rows of pixels forming a sliding 3×3 window. This window is fed into two parallel Sobel convolution units that compute the horizontal (Gx) and vertical (Gy) gradients using shift-and-add operations instead of multipliers, improving speed and reducing resource usage. The gradient values are then combined using a hardware-friendly magnitude approximation |Gx| + |Gy| that avoids complex square-root calculations. A programmable threshold module

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converts the gradient magnitude into a binary edge map by classifying strong gradient transitions as edges. The processed edge pixels are stored temporarily in an output buffer to ensure synchronization with the VGA display controller. Finally, the FPGA generates appropriate HSYNC, VSYNC, and pixel clock signals to display the edge-detected video frames on a VGA monitor in real time. The entire architecture is designed using Verilog HDL, synthesized and implemented in Xilinx Vivado, utilizing a pipelined and parallelized design approach that ensures low latency, high throughput, and efficient FPGA resource utilization.

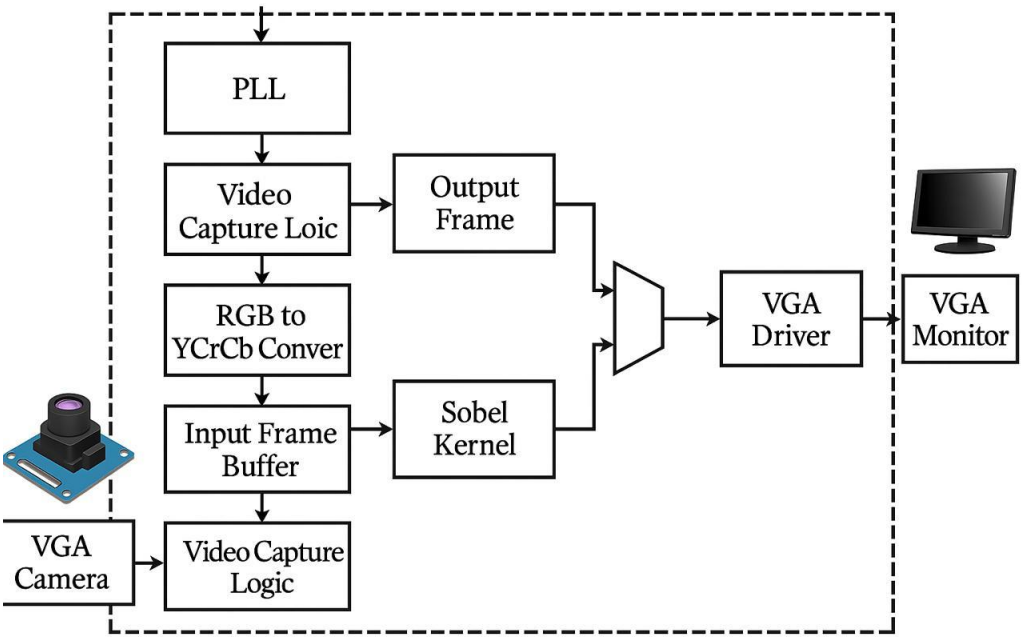

Figure 1: System Architecture

III. IMPLEMENTATION

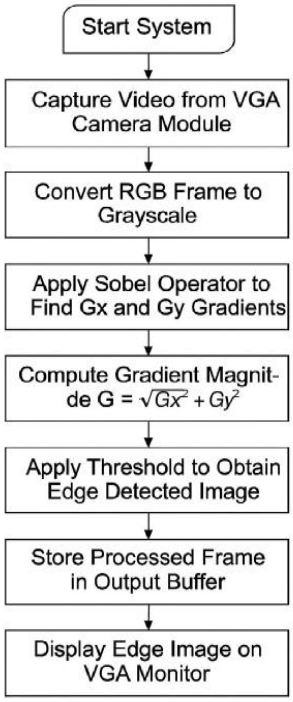

Figure 2: Implementation Steps.

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RESULT

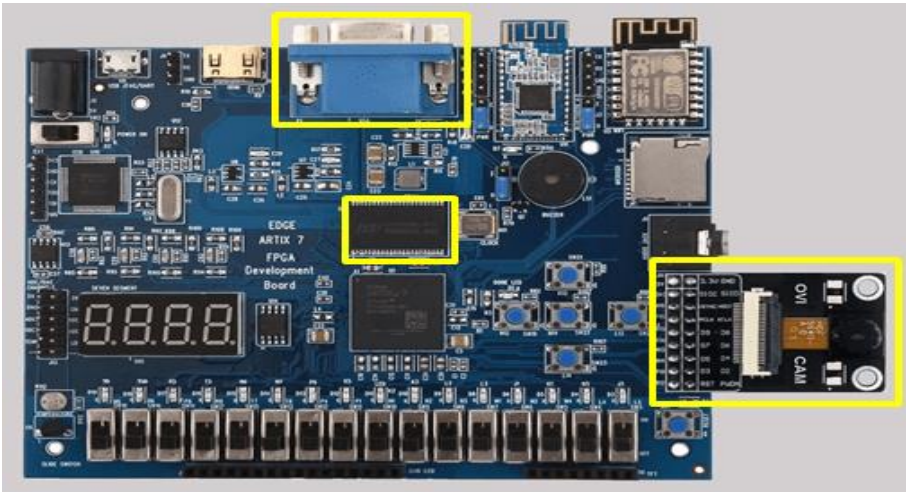

Fig: Artix 7 FPGA Board.

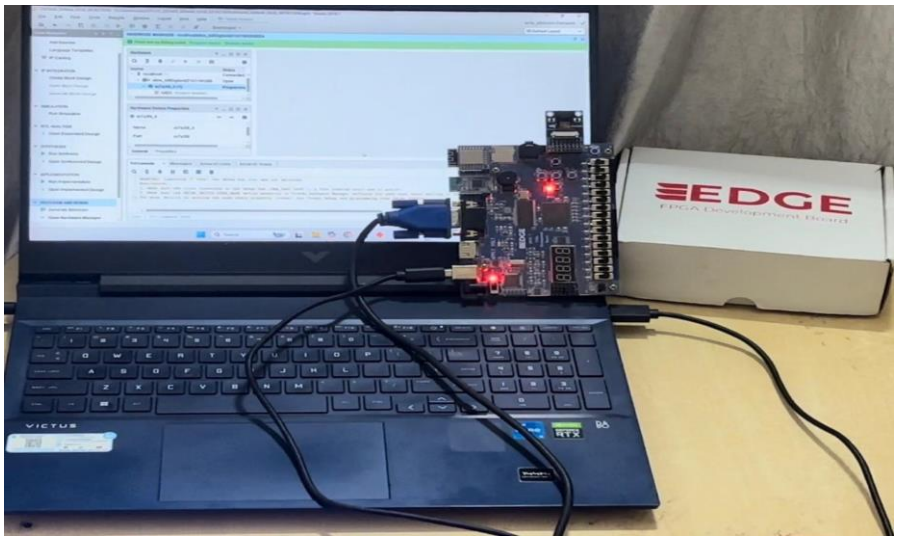

Fig: Experimental Setup

Resource	Utilization	Available	Utilization %
LUT	1109	20800	5.33
LUTRAM	3	9600	0.03
FF	952	41600	2.29
BRAM	2.50	50	5.00
IO	71	170	41.76
BUFG	7	32	21.88
MMCM	1	5	20.00

Fig: FPGA Post Synthesis Results

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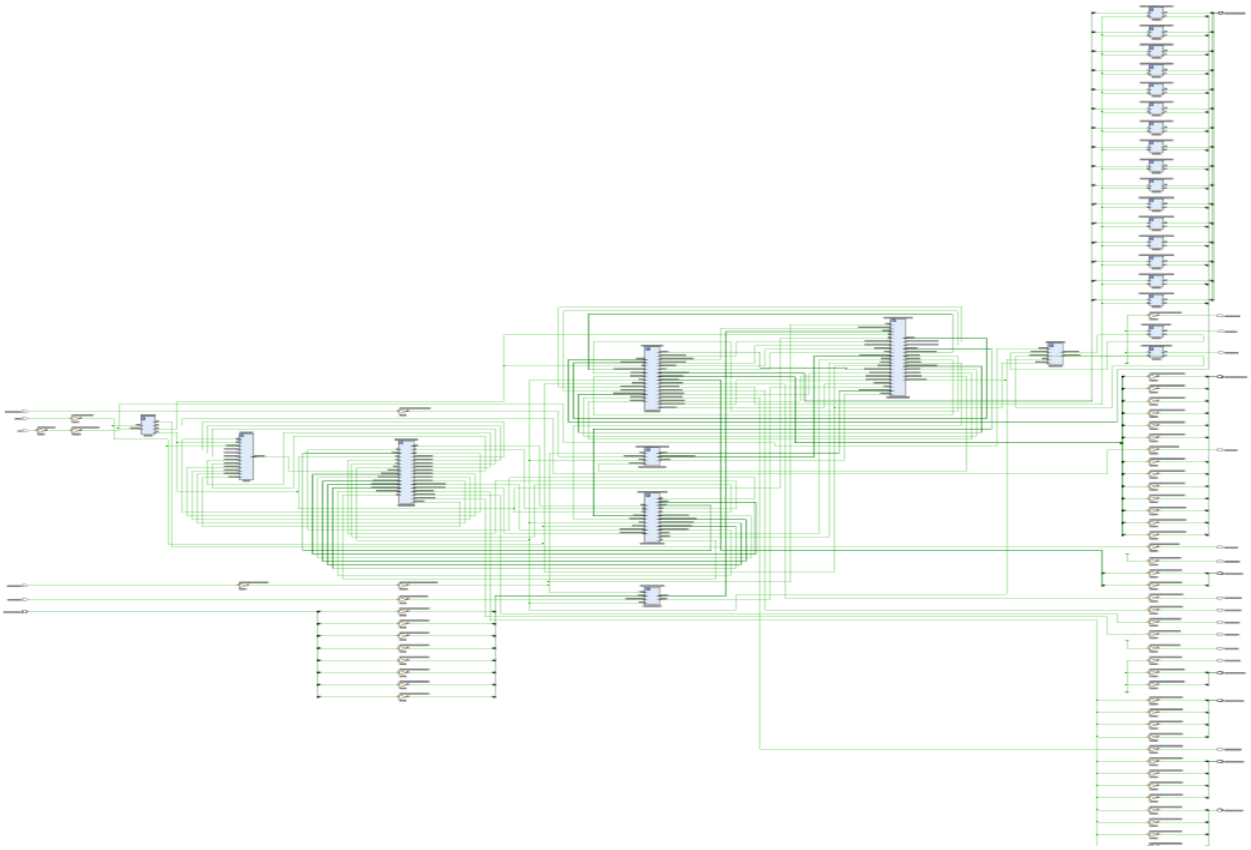

Fig: RTL Schematic of top level module.

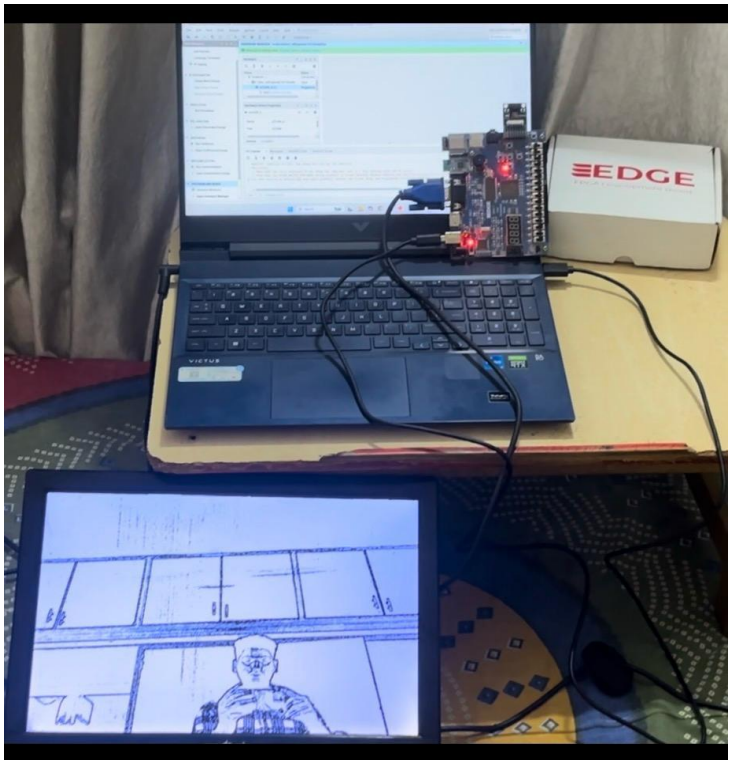

Fig: Sample Output

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IV. CONCLUSION

This work demonstrates a fully developed VLSI architecture for real-time video edge detection using the Sobel operator. The implementation on the Artix-7 FPGA validates the proposed design's efficiency in terms of speed, accuracy, and resource usage. By combining parallelism, pipelining, and optimized memory structures, the system achieves high-performance edge detection suitable for embedded vision. Future work may involve optimizing noise resistance using Gaussian smoothing or expanding the pipeline to include advanced edge detectors.

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