



Design and Analysis of a Low-Power High-Speed 32-bit ALU Using Optimized CMOS Architecture

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Abstract: With continuous scaling of CMOS technology and increasing demand for energy-efficient computing systems, the design of high-performance and low-power arithmetic circuits has become a critical challenge in Very Large-Scale Integration (VLSI). The Arithmetic Logic Unit (ALU) is one of the most frequently utilized components in microprocessors, digital signal processors, and embedded systems. Its power consumption and delay significantly influence overall system performance. This paper presents the design, implementation, and analysis of a 32-bit low-power high-speed ALU using an optimized Carry Lookahead Adder (CLA) architecture in 45nm CMOS technology. The proposed design incorporates transistor sizing optimization, clock gating, and multi-threshold CMOS techniques to minimize dynamic and leakage power. Performance evaluation is carried out in terms of propagation delay, average power consumption, and Power-Delay Product (PDP). Comparative analysis with a conventional Ripple Carry Adder (RCA)-based ALU demonstrates significant improvements in speed and energy efficiency. The proposed architecture is suitable for next-generation low-power computing applications.

Keywords: VLSI, CMOS, Low-Power Design, ALU, Carry Lookahead Adder, Power-Delay Product, 45nm Technology, Clock Gating.

I. INTRODUCTION

Advancements in semiconductor technology have enabled integration of billions of transistors onto a single chip. With shrinking technology nodes, modern electronic systems demand high computational speed while maintaining low power consumption. Portable devices, IoT nodes, and edge computing systems especially require energy-efficient architectures.

The Arithmetic Logic Unit (ALU) is a central processing component responsible for performing arithmetic and logical operations such as addition, subtraction, AND, OR, XOR, shift operations, and comparison. Since arithmetic operations are executed frequently in processor pipelines, optimizing ALU performance has a direct impact on overall system throughput and power efficiency.

However, as technology scales into deep submicron regions (45nm and below), challenges such as:

- Increased leakage currents
- Higher power density
- Short-channel effects
- Signal integrity issues

become significant.

This paper focuses on designing a 32-bit ALU optimized for low power and high-speed using CMOS technology. The major contribution includes:

1. Adoption of Carry Lookahead Adder (CLA) architecture for fast arithmetic computation.
2. Application of clock gating to reduce switching activity.
3. Implementation of transistor sizing optimization.
4. Use of Multi-Threshold CMOS (MTCMOS) to reduce leakage power.
5. Detailed performance comparison with conventional ripple-carry ALU.

II. RELATED WORK

Several architectures have been explored for ALU design in VLSI systems:

A. Ripple Carry Adder (RCA)

The Ripple Carry Adder is simple and area-efficient but suffers from linear carry propagation delay:

$$T_{delay} \propto n$$



where n is the number of bits.

B. Carry Lookahead Adder (CLA)

CLA improves speed by generating carry signals in parallel using propagate and generate functions.

$$G_i = A_i B_i$$

$$P_i = A_i \oplus B_i$$

$$C_{i+1} = G_i + P_i C_i$$

This reduces carry computation delay significantly.

C. Carry Select Adder (CSLA)

CSLA pre-computes sum outputs for both possible carry inputs but increases area.

D. Low-Power Techniques in Literature

Previous research explored:

- Dynamic voltage scaling
- Power gating
- Clock gating
- Multi-threshold devices
- Adiabatic logic

However, many designs compromise either area or speed.

This work aims to achieve a balanced trade-off among power, delay, and area.

❖ Proposed ALU Architecture

A. Overall Block Diagram

The proposed 32-bit ALU consists of:

1. 32-bit Carry Lookahead Adder
2. Logic Operation Unit
3. Multiplexer-based Output Selector
4. Control Signal Decoder

B. Functional Operations Supported

The ALU supports:

- Addition
- Subtraction
- AND
- OR
- XOR
- NOT
- Logical Shift Left/Right

Operation selection is controlled using a 4-bit control signal.

❖ Carry Lookahead Adder Design

A. Propagate and Generate Logic

For each bit:

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

Carry output:

$$C_{i+1} = G_i + P_i C_i$$

B. Group Carry Computation

To reduce complexity, the 32-bit CLA is implemented using hierarchical grouping (4-bit blocks).

Group propagate and generate:

$$P_G = P_3 P_2 P_1 P_0$$

$$G_G = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$$

This reduces carry delay from $O(n)$ to $O(\log n)$.

❖ Low-Power Optimization Techniques

A. Clock Gating

Dynamic power is given by:



$$P_{dynamic} = \alpha C_L V_{DD}^2 f$$

Where:

- α = switching activity
- C_L = load capacitance
- V_{DD} = supply voltage
- f = operating frequency

Clock gating reduces unnecessary switching activity.

B. Transistor Sizing Optimization

Transistor widths are adjusted to:

- Reduce capacitance
- Improve rise/fall times
- Maintain balanced delay

C. Multi-Threshold CMOS (MTCMOS)

High-threshold transistors are used in non-critical paths to reduce leakage: $I_{leakage} \propto e^{-V_{th}}$
This significantly lowers static power consumption.

Paper [11] compared two ALU architectures based on Ripple Carry Adder (RCA) and Sklansky parallel-prefix adder structures. The study showed that the Sklansky adder significantly reduced propagation delay and improved computational speed compared to the conventional RCA. Physical design analysis, including floor planning and routing, was also performed using Cadence tools. The results demonstrated that optimized adder selection greatly influences ALU speed and power efficiency.

Key Findings:

- Sklansky adder achieved lower delay.
- Improved speed-performance ratio.
- Suitable for high-performance processor applications.

Research in [12] focused on designing a 32-bit CMOS-based ALU for ASIC implementation. The architecture integrated arithmetic operations such as addition, subtraction, increment, and buffering along with logical operations including AND, OR, XOR, and XNOR. The authors emphasized energy-efficient CMOS design methodologies to reduce power consumption while maintaining high computational speed.

Key Findings:

- Energy-efficient 32-bit ALU implementation.
- Reduced power consumption through CMOS optimization.
- Suitable for embedded and portable application

The authors [13] proposed a 32-bit ALU using Feedback Switch Logic (FSL) and compared it with conventional static CMOS implementation at 90 nm technology. FSL reduced switching capacitance and enhanced circuit speed. Experimental results showed a delay reduction of approximately 14% while maintaining acceptable power consumption.

Key Findings:

- 14% reduction in propagation delay.
- Faster switching behaviour than static CMOS.
- Effective for high-speed ALU applications.

Study in paper [14] analyzed a 32-bit ALU designed using CMOS and Transmission Gate (TG) logic styles at 45 nm and 32 nm technologies. Performance metrics such as average power consumption, propagation delay, and power-delay product (PDP) were evaluated. The TG-based implementation demonstrated improvements in power efficiency and speed compared to conventional CMOS circuits.

Key Findings:

- Lower power-delay product.
- Reduced transistor count.
- Enhanced speed at deep submicron technologies.

The study in [15] investigated Gate Diffusion Input (GDI) techniques as an alternative to traditional CMOS logic. GDI significantly reduced transistor count, resulting in lower switching power and reduced propagation delay. The authors concluded that GDI-based ALUs provide superior power efficiency and compact design compared to conventional CMOS implementations.

**Key Findings:**

- Reduced power dissipation.
- Lower propagation delay.
- Smaller silicon area.

This research [16] compared Complementary Pass Logic (CPL), Double Pass Logic (DPL), and Dual Value Logic (DVL) approaches for ALU implementation. The DVL technique achieved the best energy efficiency, while DPL offered improved performance under low-voltage operation.

Key Findings:

- DVL provides minimum power consumption.
- DPL improves speed under low supply voltage.
- CPL reduces chip area.

The authors [17] evaluated various logic styles including CMOS, GDI, Modified GDI (MGDI), Transmission Gate Logic (TGL), and Pass Transistor Logic (PTL). The study compared transistor count, power dissipation, and delay. Results indicated that GDI and MGDI techniques offer significant improvements in power efficiency while maintaining high speed.

Key Findings:

- GDI and MGDI outperform conventional CMOS in power efficiency.
- Reduced transistor count.
- Improved delay characteristics.

Recent research [18] has focused on architectural optimization techniques such as clock gating, data gating, and power gating. These methods reduce dynamic and leakage power consumption without substantially affecting performance. Studies report dynamic power reductions ranging from 45% to 66%.

Key Findings:

- Significant reduction in dynamic power.
- Effective for battery-operated systems.
- Maintains acceptable computational speed.

Research Gap Identified

From the reviewed literature, the following gaps are identified:

1. Most designs focus on either power reduction or speed enhancement, but not both simultaneously.
2. Several low-power techniques increase propagation delay.
3. Advanced logic styles reduce transistor count but may suffer from voltage degradation.
4. Few studies combine optimized CMOS architecture with efficient adder structures in a full 32-bit ALU.
5. Limited work exists on achieving low power, high speed, and low area simultaneously in deep submicron technologies.

III. CMOS IMPLEMENTATION DETAILS

- Technology: 45nm CMOS
- Supply Voltage: 1V
- Frequency: 500 MHz
- Simulation Tool: Cadence Virtuoso
- Layout Style: Standard Cell Based
- Design constraints: Minimize fan-out, Avoid long interconnects, Optimize critical path

Critical path identified: Carry propagation path through CLA logic.

Performance Evaluation**A. Simulation Setup**

Input vectors applied for all possible arithmetic operations. Worst-case delay measured from input change to output stabilization.

B. Measured Parameters

1. Average Power Consumption
2. Propagation Delay
3. Power-Delay Product (PDP)
4. Area (Gate Count)



C. Results

Table 1: Result Comparison

Parameter	RCA-based ALU	Proposed CLA ALU
Power	2.85 mW	2.12 mW
Delay	3.6 ns	1.85 ns
PDP	10.26 pJ	3.92 pJ
Area	100%	112%

IV. RESULTS AND DISCUSSION

A. Speed Improvement

Delay reduction $\approx 48\%$ and Parallel carry generation significantly reduces computation time.

B. Power Reduction

Power reduced $\approx 25\%$ and Clock gating and MTCMOS contribute to static and dynamic power reduction.

C. Area Trade-off

Area increased slightly due to complex carry logic, but performance gains justify overhead.

Table 2: Comparative Analysis with Existing Architectures

Architecture	Speed	Power	Area	Complexity
RCA	Low	Low	Low	Simple
CSLA	High	Medium	High	Moderate
Proposed CLA	Very High	Low	Medium	Moderate

The proposed design provides the best balance of speed and power.

D. Applications

The proposed ALU architecture is suitable for:

- Microprocessors
- RISC-V cores
- DSP architectures
- IoT edge devices
- AI accelerators
- Low-power embedded systems

E. Scalability and Future Scope

Future enhancements include:

1. Implementation in 7nm FinFET technology
2. Integration with RISC-V processor pipeline
3. Approximate computing for AI workloads
4. FPGA prototyping
5. Voltage scaling techniques

V. CONCLUSION

This paper presented the design and analysis of a low-power, high-speed 32-bit ALU using Carry Lookahead architecture in 45nm CMOS technology. By incorporating clock gating, transistor sizing optimization, and multi-threshold CMOS techniques, significant improvements in delay and energy efficiency were achieved. Compared to conventional ripple carry-based ALU design, the proposed architecture reduced delay by nearly 48% and improved Power-Delay Product substantially. The design demonstrates suitability for high-performance and energy-efficient VLSI systems.

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