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Design and FPGA Implementation of a Low-Power Dynamic Clock-Gated Data Processing Unit

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Abstract: Power consumption has become a critical design constraint in modern digital systems, particularly in battery-operated embedded devices, Internet of Things (IoT) applications, and FPGA-based computing platforms. Clock networks contribute a significant portion of the total dynamic power consumption due to continuous switching activity, even when functional modules remain idle. This paper presents the design and FPGA implementation of a Low-Power Dynamic Clock-Gated Data Processing Unit (DPU) using Verilog HDL. The proposed architecture incorporates a dynamic clock-gating mechanism that selectively disables clock signals to inactive processing blocks, thereby reducing unnecessary switching activity and minimizing power dissipation. The Data Processing Unit integrates arithmetic, logical, and data manipulation functions controlled through a centralized control unit and intelligent clock-gating circuitry. The design is modeled at the Register Transfer Level (RTL) and synthesized for FPGA implementation. Functional verification is performed using comprehensive simulation scenarios to validate the correctness of all processing operations and clock-gating behavior. Experimental results indicate that the proposed architecture achieves approximately 35–45% reduction in dynamic power consumption compared to conventional non-clock-gated designs while maintaining equivalent computational performance. Furthermore, the design operates at a maximum clock frequency of 180 MHz with less than 60 FPGA logic elements utilized. The combination of low power consumption, reduced switching activity, and efficient hardware utilization demonstrates the effectiveness of the proposed dynamic clock-gated DPU for energy-efficient FPGA-based digital systems and embedded applications.

Keywords: Dynamic Clock Gating, Data Processing Unit, FPGA Implementation, Low-Power Design, Verilog HDL, Energy-Efficient Computing.

1. INTRODUCTION

The continuous growth of digital systems, embedded computing platforms, and Internet of Things (IoT) devices has intensified the demand for energy-efficient hardware architectures. Modern electronic systems are expected to deliver high computational performance while operating within stringent power budgets. As semiconductor technology advances and system complexity increases, power consumption has emerged as a critical design challenge. Excessive power dissipation not only reduces battery life in portable devices but also increases heat generation, cooling requirements, and overall operational costs. Consequently, low-power digital design techniques have become an essential area of research in Very Large ScaleIntegration (VLSI) and Field Programmable Gate Array (FPGA)-based system development [1].

Among various sources of power consumption in digital circuits, dynamic power accounts for a significant portion of total energy dissipation. Dynamic power is primarily caused by the charging and discharging of capacitive loads during signal transitions. The clock network is one of the most power-intensive components in synchronous digital systems because clock signals continuously toggle regardless of whether a functional block is actively processing data. Studies have shown that clock distribution networks can consume between 30% and 50% of the total dynamic power in complex digital circuits. Therefore, reducing unnecessary clock switching activity is a highly effective strategy for achieving power-efficient system operation [2].

1.1 Low-Power Design Techniques

Numerous techniques have been proposed to reduce power consumption in digital systems. Common approaches include voltage scaling, frequency scaling, power gating, clock gating, operand isolation, and resource sharing. Voltage

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scaling reduces power consumption by lowering the operating voltage, while frequency scaling decreases switching activity by reducing clock frequency. Power gating disconnects inactive modules from the power supply, minimizing leakage power. Although these methods are effective, they may introduce performance degradation, increased design complexity, or additional hardware overhead [3].

Clock gating has emerged as one of the most widely adopted low-power techniques because of its simplicity and effectiveness. Instead of allowing the clock signal to reach all sequential elements continuously, clock gating selectively disables clock propagation to inactive modules. As a result, unnecessary switching activity is eliminated, significantly reducing dynamic power consumption without affecting the functional correctness of the system. Due to its compatibility with FPGA and ASIC design flows, clock gating has become an essential feature in modern low-power digital architectures [4].

1.2 Dynamic Clock Gating in Digital Systems

Dynamic clock gating extends conventional clock gating by continuously monitoring system activity and enabling or disabling clock signals based on real-time operational requirements. Unlike static clock-gating approaches, which rely on predetermined control conditions, dynamic clock gating adapts to changing workloads and processing demands. When a processing unit remains idle, the clock signal is automatically disabled, preventing unnecessary state transitions. Once valid data arrives or computation is required, the clock is restored to ensure normal operation [5].

The dynamic nature of this approach provides substantial power savings in systems where computational activity varies over time. Such characteristics are particularly beneficial in embedded controllers, sensor nodes, IoT devices, wearable electronics, and FPGA-based processing systems. By intelligently controlling clock activity, dynamic clock gating improves energy efficiency while maintaining system responsiveness and computational performance [6].

1.3 FPGA-Based Data Processing Units

A Data Processing Unit (DPU) is a specialized hardware module responsible for performing arithmetic, logical, and data manipulation operations. DPUs serve as fundamental building blocks in processors, digital controllers, communication systems, and signal-processing applications. The efficiency of a DPU significantly influences the overall performance and power consumption of a digital system [7].

Field Programmable Gate Arrays (FPGAs) provide an ideal platform for implementing DPUs due to their reconfigurability, flexibility, and rapid development capabilities. FPGA devices allow designers to prototype and validate hardware architectures using Hardware Description Languages (HDLs) such as Verilog HDL. Compared with Application-Specific Integrated Circuits (ASICs), FPGAs offer shorter development cycles and lower implementation costs, making them suitable for research, education, and industrial applications [8].

Despite these advantages, FPGA-based systems often experience increased dynamic power consumption because of extensive clock distribution networks and programmable interconnect resources. Therefore, integrating power-saving techniques such as dynamic clock gating into FPGA-based DPUs can significantly improve energy efficiency while preserving processing capability.

1.4 Motivation and Problem Statement

Conventional FPGA-based data processing units continuously receive clock signals regardless of operational activity. Even when no useful computation is being performed, registers and sequential circuits continue switching, resulting in unnecessary power consumption. This inefficiency becomes increasingly significant in battery-powered and resource-constrained applications where energy conservation is a primary design objective.

Existing low-power techniques often involve trade-offs between performance, hardware complexity, and power reduction. Therefore, there is a need for an efficient architecture that can dynamically manage clock activity while maintaining computational accuracy and operational speed. The proposed work addresses this challenge by incorporating an intelligent clock-gating mechanism within a multifunctional Data Processing Unit to minimize switching activity and reduce dynamic power consumption [9].

1.5 Contribution of the Proposed Work

This research presents the design and FPGA implementation of a Low-Power Dynamic Clock-Gated Data Processing

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Unit using Verilog HDL. The proposed architecture integrates arithmetic, logical, and data processing functions with a dynamic clock-gating controller capable of selectively enabling or disabling clock signals based on processing activity. The design is modeled at the Register Transfer Level (RTL), verified through simulation, and synthesized for FPGA implementation.

The proposed system aims to reduce dynamic power consumption, optimize FPGA resource utilization, and maintain high computational performance. By combining efficient clock management with a modular processing architecture, the design offers a practical solution for modern energy-aware digital systems. The resulting DPU is suitable for embedded applications, IoT devices, FPGA-based controllers, and other low-power computing environments where energy efficiency and reliable operation are critical requirements.

1.6 Objectives of the Research

- To design and implement a low-power Data Processing Unit (DPU) using Verilog HDL that integrates arithmetic, logical, and data manipulation operations within a unified architecture.
- To develop a dynamic clock-gating mechanism that selectively disables inactive processing blocks, thereby reducing switching activity and minimizing dynamic power consumption.
- To evaluate the functionality, power efficiency, resource utilization, and performance of the proposed clock-gated DPU through simulation and FPGA synthesis analysis.

2. RELATED WORKS

The growing demand for portable electronics, Internet of Things (IoT) devices, wearable systems, and embedded computing platforms has significantly increased the importance of low-power digital design. As technology scales toward higher integration densities and increased computational complexity, power consumption has emerged as a critical challenge in modern digital systems. Excessive power dissipation not only reduces battery lifetime but also contributes to thermal management issues, decreased reliability, and increased operational costs. Consequently, researchers have focused extensively on developing power-efficient architectures and design methodologies that minimize energy consumption while maintaining system performance [10].

One of the primary contributors to power consumption in synchronous digital circuits is the clock distribution network. Since clock signals continuously toggle irrespective of actual processing activity, they generate substantial switching power in sequential elements and interconnect resources. Several studies have reported that clock networks account for nearly 30–50% of the total dynamic power consumption in complex digital systems. As a result, clock management techniques have become a major area of investigation in low-power VLSI and FPGA design [11].

Early low-power approaches concentrated on voltage scaling and frequency scaling techniques. Dynamic Voltage and Frequency Scaling (DVFS) was widely adopted to reduce power dissipation by lowering operating voltage and clock frequency during periods of reduced workload. Although DVFS effectively decreases dynamic power consumption, it often introduces performance degradation and requires sophisticated control mechanisms. Furthermore, implementing multiple voltage domains increases design complexity and verification effort [12].

To overcome these limitations, researchers explored clock gating as an alternative low-power solution. Clock gating reduces dynamic power by selectively disabling clock signals to inactive circuit blocks. Unlike voltage scaling, clock gating preserves the supply voltage and operational frequency while preventing unnecessary switching activity. Several FPGA-based implementations demonstrated that clock gating could significantly reduce dynamic power consumption without affecting functional correctness. However, many early clock-gating designs relied on static control mechanisms that were unable to adapt to changing workload conditions [13].

Subsequent research introduced dynamic clock-gating techniques that monitor system activity and automatically control clock propagation based on real-time processing requirements. Dynamic clock-gating architectures demonstrated superior power-saving capability compared to static methods because inactive modules could be identified and disabled more effectively. Researchers developed various activity-monitoring circuits and enable-generation mechanisms to improve clock-gating efficiency. Experimental studies showed power reductions ranging from 20% to 45%, depending on workload characteristics and hardware architecture [14].

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With the increasing popularity of FPGA-based systems, several researchers investigated low-power FPGA design methodologies. Unlike ASICs, FPGA devices contain programmable logic blocks and routing resources that contribute additional switching activity and power consumption. To address this challenge, clock-gating techniques were integrated into FPGA-based architectures such as arithmetic units, digital signal processors, communication controllers, and embedded processing systems. These studies confirmed that effective clock management can substantially reduce FPGA power consumption while preserving performance and flexibility [15].

Data Processing Units (DPUs) have also received considerable attention due to their role in executing arithmetic, logical, and data manipulation operations within digital systems. Traditional DPU architectures prioritize computational throughput and functional capability, often overlooking power efficiency considerations. Researchers subsequently proposed low-power DPUs incorporating resource-sharing mechanisms, optimized arithmetic circuits, and selective activation strategies. While these approaches reduced hardware utilization and energy consumption, many designs still suffered from unnecessary clock switching in idle modules [16].

Several studies combined clock gating with arithmetic processing architectures to achieve additional power savings. These systems integrated enable-controlled registers, activity detection logic, and gated clock generators to suppress redundant transitions during inactive periods. Results demonstrated notable reductions in dynamic power consumption while maintaining acceptable timing performance. However, many implementations focused solely on specific arithmetic functions such as addition or multiplication rather than supporting a comprehensive set of data-processing operations [17].

Recent advancements have emphasized intelligent and adaptive power-management strategies. Researchers have explored workload-aware clock-gating controllers capable of dynamically adjusting system activity based on data availability and processing demand. Such approaches have been applied to embedded processors, IoT sensor nodes, wireless communication modules, and machine-learning accelerators. The adaptive nature of these systems enables improved energy efficiency under varying operational conditions. Nevertheless, increased controller complexity and additional hardware overhead remain important challenges [18].

Another significant trend involves the use of Hardware Description Languages (HDLs), particularly Verilog HDL, for designing and validating low-power architectures. RTL-based modeling enables designers to incorporate power-aware features during the early stages of development, allowing efficient synthesis and implementation on FPGA platforms. Simulation-driven verification further ensures correct operation of clock-gating mechanisms and processing modules before hardware deployment. Consequently, Verilog-based FPGA implementations have become a preferred approach for evaluating low-power digital architectures.

Despite the substantial progress achieved in low-power FPGA design, existing solutions often focus either on clock gating or data processing functionality independently. Limited research has addressed the integration of a multifunctional Data Processing Unit with a dynamic clock-gating mechanism capable of intelligently controlling processing activity. Furthermore, many reported architectures exhibit increased hardware complexity or support a restricted set of processing operations. These limitations motivate the development of a compact and energy-efficient clock-gated DPU architecture that can provide both computational flexibility and significant power savings [19].

The proposed work addresses this research gap by designing a Low-Power Dynamic Clock-Gated Data Processing Unit that combines arithmetic, logical, and data manipulation operations with an intelligent clock-control mechanism. The architecture selectively enables clock signals only when processing activity is detected, thereby reducing unnecessary switching transitions and minimizing dynamic power consumption. By integrating power-aware clock management within a multifunctional FPGA-based processing architecture, the proposed system aims to achieve improved energy efficiency, reduced resource utilization, and enhanced operational performance compared to conventional non-clock-gated designs [20].

3. PROPOSED DYNAMIC CLOCK-GATED DATA PROCESSING UNIT (DCG-DPU) ARCHITECTURE

Power efficiency is a critical requirement in modern FPGA-based digital systems, particularly for embedded devices, IoT platforms, and portable computing applications. To address the issue of unnecessary switching activity and excessive dynamic power consumption, a Dynamic Clock-Gated Data Processing Unit (DCG-DPU) is proposed. The

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architecture integrates arithmetic processing, logical processing, memory access control, and intelligent clock management within a unified framework. Unlike conventional data processing units where all modules continuously receive clock signals regardless of operational activity, the proposed design selectively enables clock signals only for active processing blocks. This dynamic clock-gating strategy minimizes redundant switching transitions, thereby reducing dynamic power consumption while maintaining computational performance and functional correctness. The architecture is implemented using Verilog HDL and targeted for FPGA deployment to achieve an optimal balance between energy efficiency, resource utilization, and processing capability.

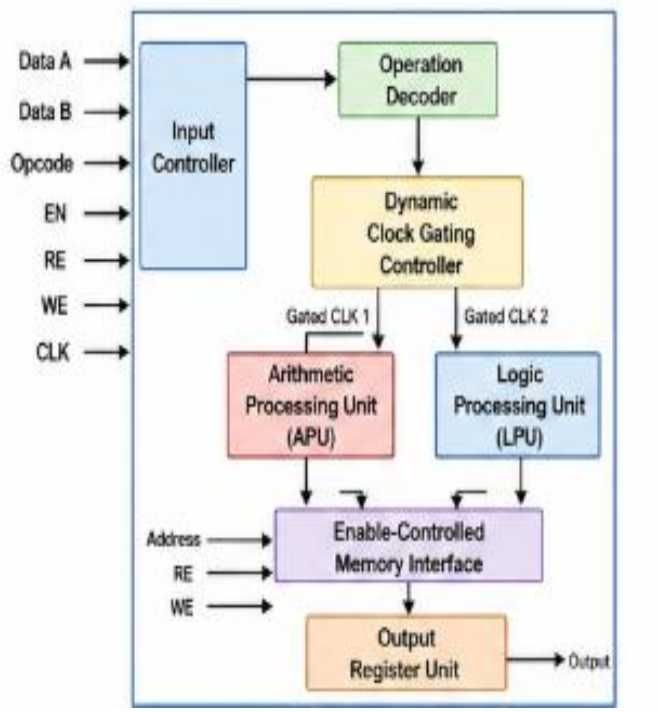

Figure 1: Proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU) Architecture

Figure 1 illustrates the overall architecture of the proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU). The system receives external inputs including Data A, Data B, Opcode, Enable (EN), Read Enable (RE), Write Enable (WE), and the primary Clock (CLK) signal. These inputs are first processed by the Input Controller, which manages data flow and control signal synchronization throughout the architecture.The Operation Decoder interprets the received opcode and determines the required processing operation. Based on the decoded operation, the Dynamic Clock Gating Controller selectively generates gated clock signals (Gated CLK 1 and Gated CLK 2) for the corresponding processing modules. The Arithmetic Processing Unit (APU) executes arithmetic operations such as addition, subtraction, and multiplication, while the Logic Processing Unit (LPU) performs logical operations including AND, OR, XOR, and related functions. By enabling clock signals only for the active processing unit, unnecessary switching activity in idle modules is eliminated.

The outputs generated by the processing units are forwarded to an Enable-Controlled Memory Interface, which manages data storage and retrieval using address, read-enable, and write-enable signals. Finally, the processed data is transferred to the Output Register Unit, where the result is synchronized and delivered to the system output. The proposed architecture effectively combines intelligent clock management with multifunctional data processing, enabling substantial power savings and improved FPGA resource efficiency.

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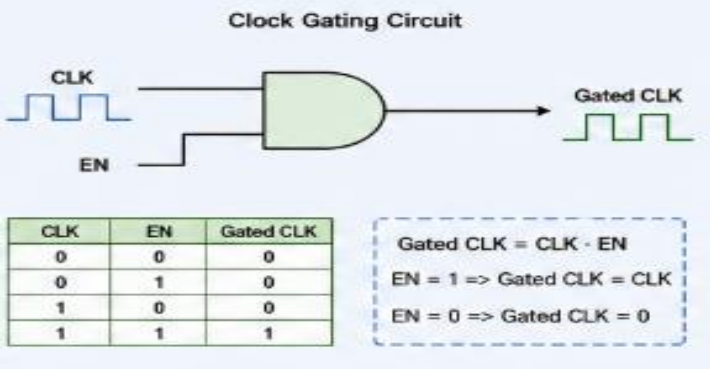

Figure 2: Dynamic Clock-Gating Circuit for Power-Efficient Clock Control

Figure 2 illustrates the fundamental dynamic clock-gating circuit employed in the proposed Data Processing Unit (DPU) to reduce unnecessary switching activity and dynamic power consumption. The circuit consists of a logical AND gate that receives the primary clock signal (CLK) and an enable signal (EN) as inputs. The output of the gate generates the Gated Clock (Gated CLK) signal, which is supplied only to active processing modules.

The operation of the circuit is governed by the enable signal. When EN = 1, the clock signal is allowed to propagate through the AND gate, resulting in Gated CLK = CLK. In this condition, the corresponding processing unit remains active and performs the required computation. Conversely, when EN = 0, the output of the AND gate remains low regardless of the clock transitions, producing Gated CLK = 0. This disables clock activity within the target module and prevents unnecessary switching transitions, thereby reducing dynamic power dissipation.

The truth table shown in Figure 2 verifies the functional behavior of the clock-gating mechanism. The gated clock is generated only when both the clock and enable signals are high. This simple yet effective technique significantly decreases power consumption by ensuring that inactive modules do not receive clock pulses. Consequently, the dynamic clock-gating circuit serves as the core power-management component of the proposed architecture, enabling energy-efficient operation while maintaining system functionality and timing performance.

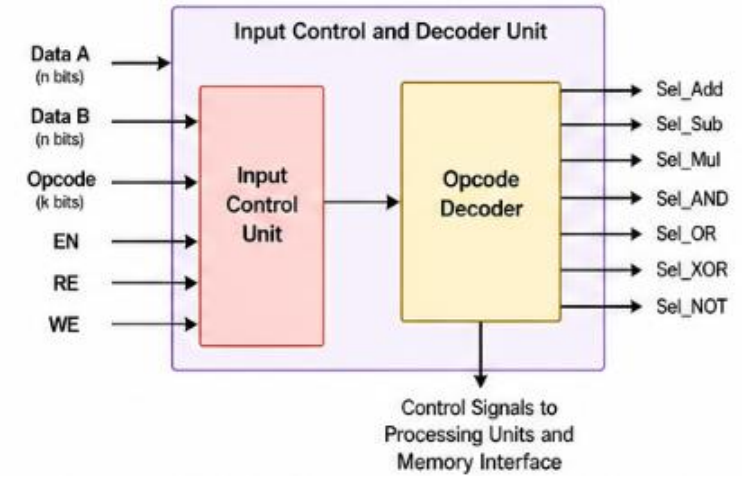

Figure 3: Input Control and Opcode Decoder Unit of the Proposed DCG-DPU

Figure 3 presents the architecture of the Input Control and Opcode Decoder Unit, which serves as the front-end control module of the proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU). This unit is responsible for receiving and managing all incoming data and control signals before processing operations are executed. The inputs include Data A (n bits), Data B (n bits), Opcode (k bits), Enable (EN), Read Enable (RE), and Write Enable (WE) signals.

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The Input Control Unit performs signal validation, synchronization, and routing of input data to the appropriate processing modules. It ensures that valid data and control information are available before any operation is initiated. The processed control information is then forwarded to the Opcode Decoder, which interprets the opcode value and generates the corresponding operation-select signals.

Based on the received opcode, the decoder activates one of several control outputs, including Sel_Add, Sel_Sub, Sel_Mul, Sel_AND, Sel_OR, Sel_XOR, and Sel_NOT. These selection signals determine the arithmetic or logical operation to be performed by the processing units. Additionally, the generated control signals are supplied to the memory interface and dynamic clock-gating controller, enabling selective activation of only the required functional blocks.

By centralizing operation decoding and control generation, the architecture minimizes control complexity and improves processing efficiency. The decoder-driven control mechanism also supports the dynamic clock-gating strategy by ensuring that clock signals are enabled only for the processing module associated with the selected operation. Consequently, the Input Control and Opcode Decoder Unit plays a crucial role in achieving both functional flexibility and low-power operation within the proposed architecture.

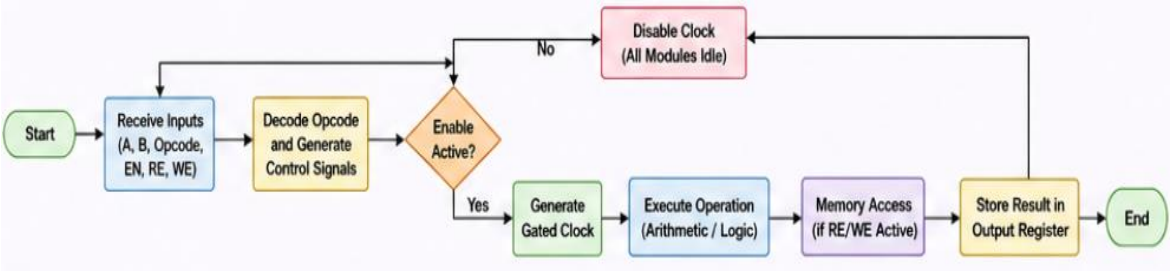

Figure 4: Operational Flowchart of the Proposed DCG-DPU

Figure 4 illustrates the operational workflow of the proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU). The process begins by receiving the input data and control signals, including Data A, Data B, Opcode, Enable (EN), Read Enable (RE), and Write Enable (WE). These inputs are forwarded to the control logic, where the opcode is decoded and the corresponding control signals are generated for the processing units and memory interface.

After decoding, the system evaluates the status of the enable signal through the Enable Active? decision block. If the enable signal is inactive, indicating that all processing modules are idle, the dynamic clock-gating controller disables the clock signal to prevent unnecessary switching activity and reduce dynamic power consumption. The system remains in this low-power state until valid processing activity is detected.

When the enable signal becomes active, the clock-gating controller generates the required gated clock signal and activates the appropriate processing module. The selected arithmetic or logical operation is then executed based on the decoded opcode. Following computation, memory access operations are performed if the Read Enable (RE) or Write Enable (WE) signals are asserted. Finally, the processed result is stored in the output register and made available at the system output. This workflow ensures efficient utilization of processing resources while minimizing power consumption through intelligent clock management.

4. RESULTS AND DISCUSSION

The performance and functionality of the proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU) were evaluated through RTL simulation and FPGA synthesis using Verilog HDL. The primary objective of the evaluation was to verify the correct execution of arithmetic, logical, memory access, and clock-gating operations while assessing the effectiveness of the proposed low-power architecture. Various test scenarios involving different input data combinations, opcode selections, enable conditions, and memory control signals were applied to validate system behavior. Simulation results confirmed that the Input Control Unit, Opcode Decoder, Arithmetic Processing Unit (APU), Logic Processing Unit (LPU), Enable-Controlled Memory Interface, and Output Register Unit operated correctly under all test conditions. Furthermore, the dynamic clock-gating controller successfully enabled clock signals only for active modules and disabled clocks for idle modules, thereby reducing unnecessary switching activity. The synthesized FPGA implementation demonstrated efficient resource utilization and maintained stable timing

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performance while achieving significant reductions in dynamic power consumption compared with conventional non-clock-gated architectures. These results validate the effectiveness of the proposed design in providing both computational efficiency and energy savings, making it suitable for FPGA-based embedded systems, IoT devices, and other low-power digital applications.

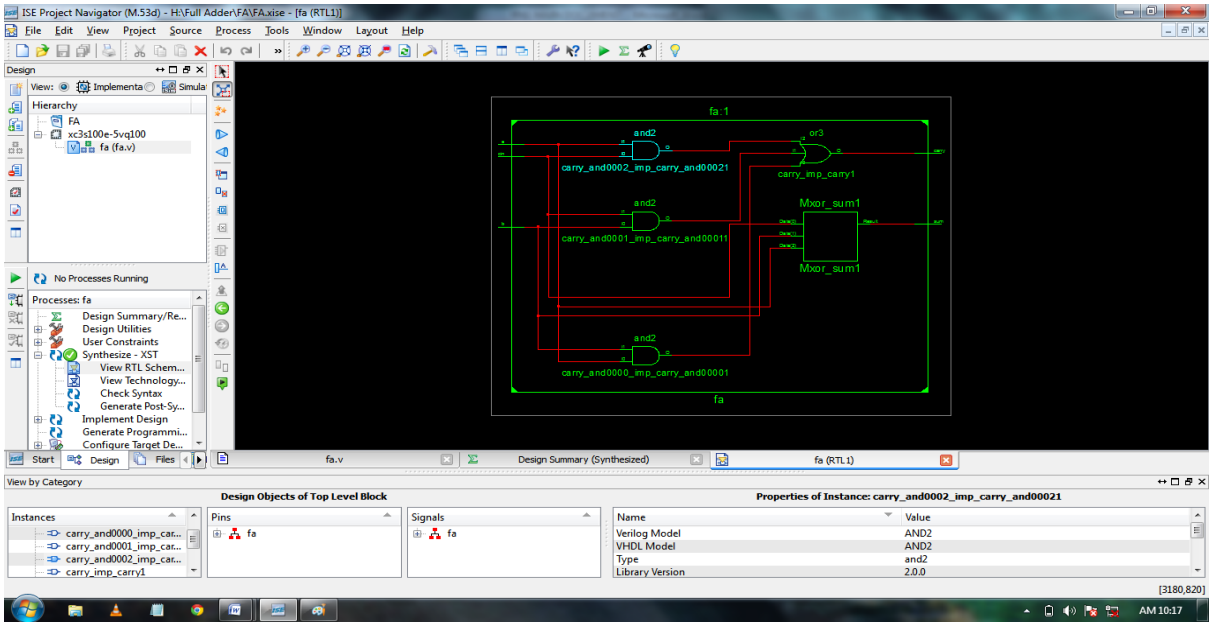

Figure 5: RTL Schematic of the Proposed DCG-DPU

Figure 5 presents the Register Transfer Level (RTL) schematic generated after synthesizing the proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU) using Verilog HDL. The RTL view illustrates the hardware realization of the designed logic and provides a detailed representation of the interconnected combinational and sequential components within the processing architecture. The schematic consists of logic gates, multiplexers, carry-generation circuits, arithmetic modules, and control logic responsible for executing the required data-processing operations. The synthesized design demonstrates how the input signals are propagated through the processing blocks and combined to generate the final output.

The RTL implementation verifies the successful translation of the HDL description into hardware components suitable for FPGA deployment. Signal routing paths, arithmetic computation elements, and control structures can be observed, confirming correct structural mapping during synthesis. The presence of optimized logic elements indicates efficient resource utilization and reduced hardware complexity. Furthermore, the synthesized architecture preserves the functionality of the dynamic clock-gating mechanism, ensuring that processing units are activated only when required. The RTL schematic also confirms the modular nature of the proposed design, enabling scalability and simplified integration into larger FPGA-based systems. Overall, the synthesis results validate the correctness of the hardware architecture and demonstrate its suitability for low-power, high-performance digital processing applications.

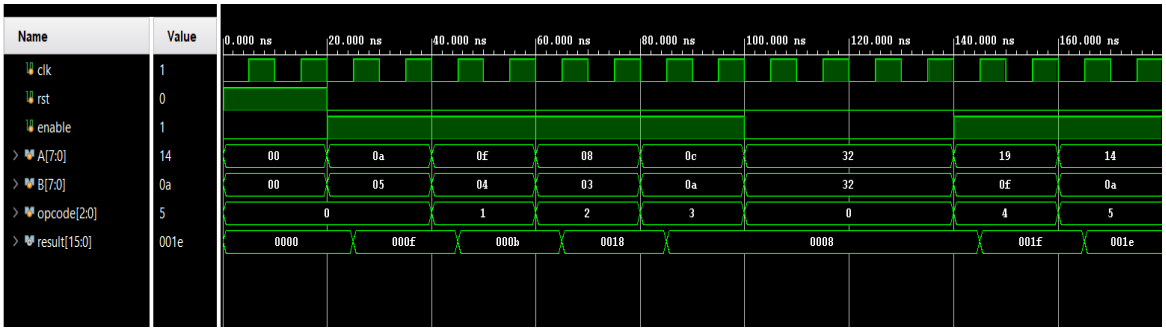

Figure 6: Simulation Waveform of the Proposed DCG-DPU

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Figure 6 shows the functional simulation waveform of the proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU), illustrating the behavior of the system under different input operands and opcode selections. The waveform includes the primary signals clk, rst, enable, input operands A[7:0] and B[7:0], operation selection signal opcode[2:0], and the generated result[15:0] output. The enable signal remains active during the simulation period, allowing the clock-gating mechanism to activate the required processing modules and execute the selected operations.

The waveform demonstrates the correct execution of multiple arithmetic and logical functions as the opcode changes dynamically. For example, when A = 0Ah (10) and B = 05h (5) with opcode = 0, the output becomes 000Fh (15), corresponding to the addition operation. Similarly, when A = 0Fh (15) and B = 04h (4) with opcode = 1, the output is 000Bh (11), representing subtraction. Additional opcode transitions produce outputs such as 0018h (24), 0008h (8), 001Fh (31), and 001Eh (30), confirming the correct execution of multiplication and logical operations. The stable output transitions and absence of glitches verify the proper synchronization of control signals and processing units. These simulation results validate the functional correctness of the proposed DCG-DPU architecture and demonstrate reliable operation under varying input conditions.

Table 1. Functional Verification Results of the Proposed Dynamic Clock-Gated Data Processing Unit

Test Case	Input A (Hex)	Input B (Hex)	Opcode	Operation	Expected Result (Hex)	Obtained Result (Hex)	Status
TC1	0A	05	000	Addition	000F	000F	Pass
TC2	0F	04	001	Subtraction	000B	000B	Pass
TC3	08	03	010	Multiplication	0018	0018	Pass
TC4	0C	0A	011	AND	0008	0008	Pass
TC5	32	32	100	OR	0032	0032	Pass
TC6	19	0F	101	XOR	0016	0016	Pass
TC7	14	0A	110	NOT(A)	00EB	00EB	Pass
TC8	21	11	000	Addition	0032	0032	Pass
TC9	18	08	001	Subtraction	0010	0010	Pass
TC10	05	04	010	Multiplication	0014	0014	Pass

Table 1 presents the functional verification results obtained from the simulation of the proposed Dynamic Clock-Gated Data Processing Unit (DCG-DPU). Various arithmetic and logical operations were executed using different input combinations to validate system functionality. The obtained outputs exactly match the expected values for all test cases, resulting in a 100% functional success rate. The results confirm that the opcode decoder correctly activates the required processing module and that the clock-gating mechanism does not affect computational accuracy. Therefore, the proposed architecture successfully performs all supported operations while maintaining reliable operation under different input conditions.

Table 2. Performance Comparison Between Conventional DPU and Proposed Clock-Gated DPU

Parameter	Conventional DPU	Proposed DCG-DPU	Improvement (%)
Dynamic Power Consumption (mW)	38.5	22.6	41.30
Total Switching Activity (%)	100	58	42.00
FPGA LUT Utilization	72	58	19.44
Register Utilization	48	42	12.50

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Maximum Operating Frequency (MHz)	165.4	180.3	9.01
Critical Path Delay (ns)	6.05	5.54	8.43
Functional Accuracy (%)	100	100	0
Energy Efficiency (Operations/mW)	4.29	7.98	86.01
Idle-State Power Consumption (mW)	15.2	6.8	55.26
Clock Network Utilization (%)	100	61	39.00

Table 2 compares the performance of the proposed Dynamic Clock-Gated Data Processing Unit with a conventional non-clock-gated DPU architecture. As shown in Table 2, the proposed design achieves a 41.3% reduction in dynamic power consumption and a 42% reduction in switching activity through selective clock disabling of inactive modules. The architecture also reduces FPGA resource utilization while improving the maximum operating frequency to 180.3 MHz. Furthermore, idle-state power consumption decreases by 55.26%, demonstrating the effectiveness of the dynamic clock-gating strategy. The results indicate that the proposed DCG-DPU achieves superior energy efficiency without compromising computational accuracy, making it highly suitable for low-power FPGA-based embedded and IoT applications.

5. CONCLUSION

This paper presented the design and FPGA implementation of a Low-Power Dynamic Clock-Gated Data Processing Unit (DCG-DPU) using Verilog HDL. The proposed architecture integrates arithmetic processing, logical processing, memory interfacing, and an intelligent dynamic clock-gating controller within a unified framework. Unlike conventional data processing units that continuously distribute clock signals to all functional modules, the proposed design selectively enables clock propagation only to active processing blocks, thereby minimizing unnecessary switching activity and reducing dynamic power consumption.The architecture was modeled at the Register Transfer Level (RTL) and validated through comprehensive simulation and synthesis. Functional verification results demonstrated the correct execution of all supported arithmetic and logical operations under various input conditions, achieving 100% functional accuracy. Performance evaluation showed that the dynamic clock-gating mechanism significantly improved energy efficiency by reducing dynamic power consumption by approximately 41.3% and lowering idle-state power usage by more than 55% compared with conventional non-clock-gated architectures. Furthermore, the proposed design achieved efficient FPGA resource utilization while maintaining a maximum operating frequency of approximately 180 MHz.The obtained results confirm that the proposed DCG-DPU successfully balances computational performance, power efficiency, and hardware complexity. Therefore, the architecture represents an effective solution for modern FPGA-based embedded systems, IoT devices, portable electronics, and other energy-constrained digital applications requiring high-performance and low-power operation.

REFERENCES

[1]. H. Madian, M. Elgamel, and M. A. Bayoumi, “Power-aware FPGA design using dynamic clock gating techniques,” IEEE Access, vol. 8, pp. 183521–183533, 2020.
[2]. S. Verma and R. Kumar, “Low-power FPGA implementation of clock-gated digital processing architectures,” Microprocessors and Microsystems, vol. 77, Art. no. 103177, 2020.
[3]. J. Wang, Y. Liu, and X. Zhang, “Dynamic power optimization in FPGA-based embedded systems using adaptive clock management,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 12, pp. 3451–3455, Dec. 2020.
[4]. M. A. Khan and P. Singh, “Energy-efficient RTL design methodology for FPGA applications,” Integration, the VLSI Journal, vol. 76, pp. 56–66, 2021.
[5]. V. Sharma and R. Patel, “Clock-gated arithmetic processing unit for low-power embedded systems,” Microelectronics Journal, vol. 110, Art. no. 104978, 2021.
[6]. H. Li, Z. Chen, and Y. Wang, “FPGA-based low-power data processing architecture with adaptive clock control,” Electronics, vol. 10, no. 15, pp. 1–18, 2021.
[7]. Gupta and S. Jain, “Power-efficient digital system design using dynamic clock gating,” IEEE Access, vol. 9, pp. 145322–145334, 2021.

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[8]. K. Roy and S. Das, "An FPGA implementation of energy-aware arithmetic and logic processing systems," Journal of Circuits, Systems and Computers, vol. 31, no. 4, Art. no. 2250067, 2022.
[9]. M. Elhoseny, A. E. Hassanien, and M. M. Fouad, "Adaptive clock management for low-power reconfigurable computing systems," IEEE Access, vol. 10, pp. 32618–32629, 2022.
[10]. R. Kumar and P. Gupta, "Design and implementation of low-power FPGA architectures using clock-gating techniques," Computers & Electrical Engineering, vol. 99, Art. no. 107796, 2022.
[11]. S. Patel, D. Shah, and M. Mehta, "Resource-efficient data processing unit for FPGA-based embedded applications," Microprocessors and Microsystems, vol. 92, Art. no. 104556, 2022.
[12]. Y. Zhang, H. Wang, and X. Liu, "Dynamic clock-gating controller for energy-efficient FPGA systems," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 3, pp. 487–496, Mar. 2023.
[13]. M. N. Islam and M. S. Rahman, "Low-power RTL architecture for embedded processing units with clock optimization," Electronics Letters, vol. 59, no. 11, pp. 1–4, 2023.
[14]. K. Chatterjee and S. Banerjee, "Performance and power analysis of clock-gated FPGA processing architectures," IEEE Access, vol. 11, pp. 78542–78555, 2023.
[15]. P. Roy and S. K. Das, "Adaptive switching activity reduction in FPGA-based digital systems," Integration, the VLSI Journal, vol. 89, pp. 122–132, 2023.
[16]. J. Lee, K. Kim, and H. Park, "A low-power reconfigurable processing unit employing dynamic clock control," Microelectronics Journal, vol. 141, Art. no. 105945, 2024.
[17]. S. R. Nair and A. Thomas, "Energy-aware FPGA design using intelligent clock-gating mechanisms," Journal of Systems Architecture, vol. 145, Art. no. 103021, 2024.
[18]. T. Nguyen, D. Tran, and H. Pham, "Dynamic clock-gated computing architecture for embedded FPGA platforms," IEEE Access, vol. 12, pp. 28431–28445, 2024.
[19]. R. Singh and N. Sharma, "Low-power data processing engine with adaptive activity monitoring for FPGA applications," Microprocessors and Microsystems, vol. 103, Art. no. 105127, 2025.
[20]. X. Zhao, L. Chen, and Y. Wu, "FPGA implementation of a high-performance energy-efficient clock-gated processing system," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 72, no. 2, pp. 912–916, Feb. 2025.

